NOVATEK
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Data Sheet

NT39125

One-chip Driver IC with internal GRAM
for 262k colors 240 RGB x 432 dot TFT LCD

Version 0.0.12

REVISION HISTORY

Date	Contents	Version
04/17/2007	- Preliminary Version 0.0.0	Ver. 0.0.0
04/24/2007	- Add AC characteristic spec (7.7) - Add application example (8.3) - Add Chip overview (9.1) - Update pad coordinates (9.3) - Add Gamma Function description (5.9) - Add Gamma adjustment registers (6.2.21~6.2.26)	Ver. 0.0.1
05/02/2007	- Modify 6bits RGB-interface data format (5.2.2.1) - Modify adjustment register of GVDD.(6.2.8) - Modify adjustment register of VGH 2nd level output timing. (6.2.9) - Modify min. value of write cycle time in CPU mode. (7.7.1 & 7.7.2)	Ver. 0.0.2
05/17/2007	- Remove VCI1 regulator & reference descriptions. (All pages) - Add VR regulator for the power supply of step-up circuit1. (All pages) - Remove AVDDO, VGHO, VGLO, VCLO pins. (4.3) - Modify display data format. (5.2.1) - Add capacitor connecting pin "VREF" for internal reference voltage. (4.4) - Modify the application circuit. (8.2 & 8.3)	Ver. 0.0.3
06/01/2007	- Remove "RCM0, RL, TB, SHUT, IDM, REV" test pins. (4.5) - Rename power supply pins such as VCI, IOVCC and VDD. (All pages) - Modify register definition of RB1h, RB2h, RB3h. (6.2.3, 6.2.4, 6.2.5) - Modify register definition of RC1h. (6.2.9)	Ver. 0.0.4
06/11/2007	- Modify 18-Bit Parallel Interface for data ram write (5.2.1.3) - Remove RDRED, RDGREEN, RDBLUE commands. (6.1) - Rename Gamma adjusting registers.(all pages)	Ver 0.0.5
06/15/2007	- Modify RB1h, RB2h, RB3h commands. (6.2) - Modify CPU-9bits write data ram format. (5.2.1) - Add Command RD4h, RDFh. (6.2)	Ver 0.0.6
06/20/2007	- Modify the LUT default values. (5.2.8) - Modify the definition of ISCI[3:0]. (6.2.7) - Rename pin 521 as "GEXT". (All pages) - Rename VR regulator adjusting register as VRA[3:0]. (6.2.9)	Ver 0.0.7
06/26/2007	- Remove DCM[1:0] bits. (6.2.9) - Re-define ISCI[3:0] setting. (6.2.7) - Add GAM_R_SEL bit. (6.2.28) - Add description of 4 preset gamma curve. (6.9.3)	Ver 0.0.8
07/03/2007	- Add TEST_GVDD bit. (6.2.29) - Modify RC2h, RC3h, RC4h commands. (6.2)	Ver 0.0.9
08/07/2007	- Remove NVP_F and NV_DF1 bit. (6.2.19) - Modify MTP program sequence. (6.4) - Add Chip information (9)	Ver 0.0.10
10/30/2007	- Modify figure error. (3) - Add gamma voltage (5.9.3) - Add gamma curve detail explain (6.1.18) - Add display resolusion control command (6.2.7) - Modify VR default output voltage (6.2.10) - Add the step voltage and the voltage range (6.2.15)	Ver 0.0.11
11/23/2007	- Modify application example (8.2, 8.3)	Ver 0.0.12

1 DESCRIPTION

NT39125 is a single chip low power CMOS LCD controller/driver for color TFT-LCD displays of 432 gates and 240xRGB columns. It has a 1.86M-bit (240 x 18bit x 432) display RAM and a full set of control functions. NT39125 offers 9 kinds microprocessor interfaces: 8080-system (8-bit, 9-bit, 16-bit, 18-bit), 6800-system (8-bit, 9-bit, 16-bit, 18-bit), serial interface. It also supply 6-bit, 16-bit, 18-bit RGB interface for driving video signal directly from controller.

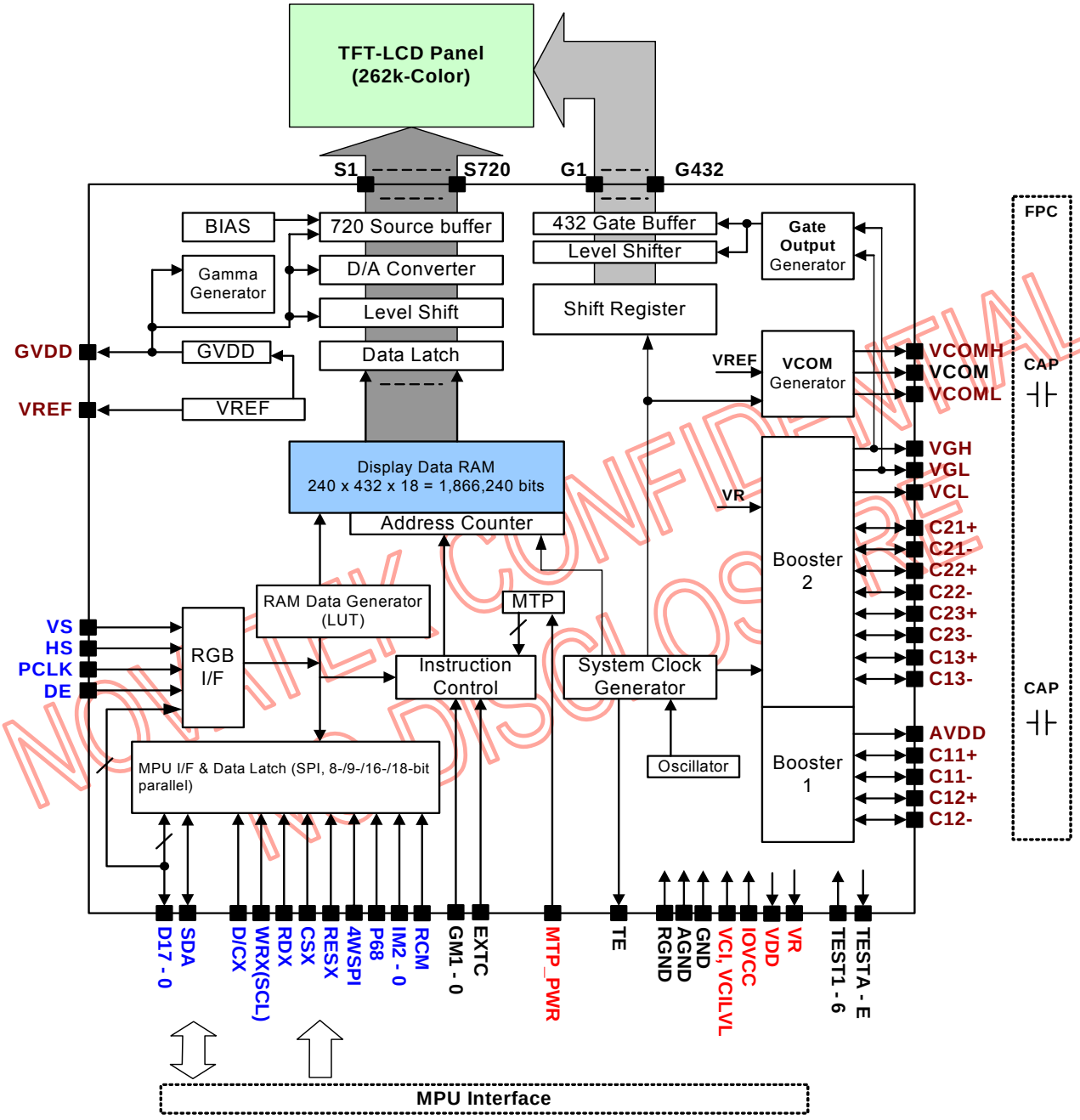
2 FEATURES

◆ Single chip AM-TFT-LCD Controller/ driver with Display RAM.
◆ Display resolution :
- 240*RGB (H) *432(V)
- 240*RGB (H) *400(V)
- 240*RGB (H) *320(V)
◆ Display data RAM (frame memory): 240 x 432 x 18-bit = 1,866,240bit
◆ Output:
- 720ch source outputs (240xRGB)
- 432 gate outputs
- Common electrode output
◆ Display mode (Color mode)
  - Full color mode (Idle mode off): 262k-colors
  - Reduce color mode (Idle mode on): 8-colors (3-bit binary mode)
◆ Interface mode (Color modes on the display host interface):
  - 12-bit/Pixel: RGB= (444) using the 1866k-bit frame memory
  - 16-bit/Pixel: RGB= (565) using the 1866k-bit frame memory
  - 18-bit/Pixel: RGB= (666) using the 1866k-bit frame memory
◆ Interface:
  - 3-pin / 4-pin serial interface
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 8080-series MCU
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 6800-series MCU
  - 6-bit, 16-bit, 18-bit RGB interface with graphic controller
◆ Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
◆ On chip
  - DC/DC converter
  - Adjusted VCOM generation
  - Separate RGB gamma control
  - Oscillator for display clock generation
  - Timing generation
  - Factory default value (VCOM offset voltage, , etc) are stored on the display module
  - 4 preset gamma curve selectable
◆ NV Memory (4-times on each function)
  - 7-bits for User ID2
  - 8-bits for User ID2
  - 7-bits for VCOM adjustment
◆ Driving Algorithm
  - 2 level gate drive with common electrode modulation drive
  - Line inversion, frame inversion
◆ Supply voltage range
  - Analog supply voltage range for VCI to AGND: 2.50V – 3.10V
  - I/O supply voltage range for IOVCC to GND: 1.65V – 3.10V
  - Internal Digital supply voltage range for VDD to GND: 1. 50V – 2.00V
◆ Output voltage levels
  - Source output voltage range for GVDD to AGND: 3.425V – 5.000V

- Power supply for driver circuit range for AVDD to AGND: 4.5V – 6.0V
- Common electrode output High voltage range for VCOMH to AGND: 2.5V – 5.0V
- Common electrode output Low voltage range for VCOML to AGND: -2.5V – 0.0V
- Positive Gate output voltage range for VGH to AGND: +10.0V to +15.0V
- Negative Gate output voltage range for VGL to AGND: -12.5V to – 4.5V

◆ Lower power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Optimized layout for COG assembly
- Operate Temperature range: -40℃ to +85℃

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1 Power Supply Pins

Table 4.1.1 Power Supply Pins

Symbol	Name	Description
VCI, VCILVL	Analog voltage	Power supply for analog system
IOVCC	Logic voltage	Power supply for I/O system
VR	Analog voltage	Power supply for step-up circuit 2
VDD	Logic voltage	Power supply for internal digital system
AGND	Analog GND	System ground for Analog system
GND	Logic GND	System Ground for I/O system and internal digital system
RGND	Logic GND	System ground for internal GRAM
MTP_PWR	MTP voltage	Power supply for MTP programming power

4.2 Interface Logic Pins

Table 4.2.1: Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>GM1, GM0</td><td>I</td><td>-Display resolution select
-For the resolution selectable, please connect these pins to the FPC.
<table>
<tr><th>GM1,GM0</th><th>Bus width selection</th></tr>
<tr><td>00</td><td>240*RGB (H) *432(V)</td></tr>
<tr><td>01</td><td>240*RGB (H) *400(V)</td></tr>
<tr><td>10</td><td>240*RGB (H) *320(V)</td></tr>
<tr><td>11</td><td>Setting disabled</td></tr>
</table></td></tr>
<tr><td>IM2, IM1, IM0</td><td>I</td><td>-MCU Parallel interface bus and Serial interface select
<table>
<tr><th>IM2,IM1,IM0</th><th>Bus width selection</th></tr>
<tr><td>000</td><td>Parallel 18-bit interface mode (D[17:0])</td></tr>
<tr><td>001</td><td>Parallel 9-bit interface mode (D[17:9])</td></tr>
<tr><td>010</td><td>Parallel 16-bit interface mode (D[17:10], D[8:1])</td></tr>
<tr><td>011</td><td>Parallel 8-bit interface mode (D[17:10])</td></tr>
<tr><td>100</td><td>Serial interface</td></tr>
<tr><td>101</td><td>Serial interface</td></tr>
<tr><td>110</td><td>Setting disabled</td></tr>
<tr><td>111</td><td>Setting disabled</td></tr>
</table></td></tr>
<tr><td>P68</td><td>I</td><td>-8080 /6800 MCU Interface mode select
-P68=’1’, select 6800-MCU parallel interface
-P68=’0’, select 8080-MCU parallel interface
-If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>4WSPI</td><td>I</td><td>-4-line or 3-line Serial interface select.
-4WSPI=’1’: 4-line Serial interface
-4WSPI=’0’: 3-line Serial interface
-This pin has internal pull-down resistor.
-If not used, please open this pin</td></tr>
<tr><td>RCM</td><td>I</td><td>-RGB or MCU interface mode selection pin.
-RCM=’1’, select RGB + SPI interface
-RCM=’0’, select MCU parallel or serial interface</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>CSX (SCEX)</td><td>I</td><td>-Chip select input pin (“Low” enable).
-This pin can be permanently fixed “Low” in MCU interface mode only.</td></tr>
<tr><td>D/CX</td><td>I</td><td>- Display data / Command selection pin in parallel interface</td></tr>
</table>

		-D/CX='1': Display Data -D/CX='0': Command -If not used, please connect this pin to GND or IOVCC
RDX (E)	I	-Read enable in 8080-system interface. -Read/ Write operation enable pin in 6800-parallel interface. -If not used, please connect this pin to GND or IOVCC
WRX (R/WX) (SCL)	I	-Write enable in 8080-system interface. -Read write selection in 6800-parallel interface. -In serial I/F, this is used as clock pin for serial interface. -If not used, please connect this pin to GND or IOVCC
D[17:0]	I/O	-Data bus in 8080-system interface. -Data bus in RGB interface. -If not used, please connect this pin to GND or IOVCC
SDA	I/O	-Data input/output signal in serial interface. -If not used, please connect this pin to GND or IOVCC
PCLK	I	-Pixel clock signal in RGB I/F mode. -If not used, please connect this pin to GND or IOVCC
VS	I	-Vertical sync. Signal in RGB I/F mode. -If not used, please connect this pin to GND or IOVCC
HS	I	-Horizontal sync. Signal in RGB I/F mode. -If not used, please connect this pin to GND or IOVCC
DE	I	-Data enable signal in RGB I/F mode. -If not used, please connect this pin to GND or IOVCC
TE	O	-Frame head pulse signal, which is used when writing data to the internal RAM. -If not used, please open this pin

4.3 Booster Circuit Pins

Table 4.4.1: Booster Circuit Pins

Symbol	I/O	Description
AVDD	Power	-Power supply for the source driver, VCOM drive and step-up circuit 2. -Output of step-up circuit 1 -Connect a capacitor for stabilization.
VGH	Power	-Liquid crystal drive power supply. -Output of step-up circuit 2 -Connect a capacitor for stabilization.
VGL	Power	-Liquid crystal drive power supply. -Output of step-up circuit 2 -Connect a capacitor for stabilization.
VCL	Power	-VCOML power supply. -Output of step-up circuit 2 -Connect a capacitor for stabilization.
C11+/-, C12+/-	C	-Capacitor connection pin for step-up circuit 1.
C13+/-, C21+/-, C22+/-, C23+/-	C	-Capacitor connection pin for step-up circuit 2.

4.4 Driver Pins

Table 4.5.1: Driver Output Pins

Symbol	I/O	Description
S1 to S720	O	Source driver output pins.
G1 to G432	O	Gate driver output pins.
VCOM	O	A power supply for the TFT common electrode.
VCOMH	O	Positive voltage output of VCOM -Connect a capacitor for stabilization.
VCOML	O	Negative voltage output of VCOM -Connect a capacitor for stabilization.
GVDD	O	A standard level for grayscale voltage generator -Connect a capacitor for stabilization.
VREF	O	Reference voltage for power block. -Connect a capacitor for stabilization.

4.5 TEST Pins

Symbol	I/O	Description
EXTC	I	-TEST pin, please connect this pin to IOVCC.
SMX	I	-TEST pin, please connect this pin to GND.
SMY	I	-TEST pin, please connect this pin to GND.
SRGB	I	-TEST pin, please connect this pin to GND.
TEST1~6	I	-These pin has internal pull-down resistor. -TEST pin, please open these pin.
TESTA~E	O	-TEST pin, please open these pin.
DUMMYR1-10	-	DUMMYR1 and DUMMYR10, DUMMYR2 and DUMMYR9, DUMMYR3 and DUMMYR4, DUMMYR5 and DUMMYR8, and DUMMYR6 and DUMMYR7 are short-circuited within the chip for COG contact resistance measurement. -If not used, please open this pin
VGLDMY1~3	-	-TEST pin, please open these pin.
GEXT	-	-TEST pin, please open these pin.
AGNDDUM1~5	O	These pins and the “AGND” pin are short-circuited within the chip. - Use them to fix the electrical potentials
GNDDUM1~29	O	These pins and the “GND” pin are short-circuited within the chip. - Use them to fix the electrical potentials
GND2	-	Reserved pins for the possibility of MIPI function implementing. -Please connect these pins to system ground.
VCI2	-	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
IOVCC2	-	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
CLKP	I	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
CLKN	I	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
DATAP	I/O	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
DATAN	I/O	Reserved pins for the possibility of MIPI function implementing. -Please open these pin.
IOVCCDUM1~2	O	These pins and the “IOVCC” pin are short-circuited within the chip. - Use them to fix the electrical potentials
DUMMY1~24	-	These pins are dummy (not have any function inside)

5 FUNCTION DESCRIPTION

5.1 MPU Interface

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting P68 and IM2-0 pins as show in ***Table 5.1.1*** and ***Table 5.1.2.***

Table 5.1.1 Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read back selection
0	0	0	0	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
0	0	0	1	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	0	1	0	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	0	1	1	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	X	Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter
0	1	1	X	Setting disabled	-
1	0	0	0	6800 MCU 18-bit Parallel	E strobe (18-bit read data and 8-bit read parameter)
1	0	0	1	6800 MCU 9-bit Parallel	E strobe (9-bit read data and 8-bit read parameter)
1	0	1	0	6800 MCU 16-bit Parallel	E strobe (16-bit read data and 8-bit read parameter)
1	0	1	1	6800 MCU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	X	Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter
1	1	1	X	Setting disabled	-

Table 5.1.2 Pin Connection according to the Interface Type

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Data bus selection
0	0	0	0	8080 MCU 18-bit Parallel	RDX	WRX	D/CX	D[17:0]: 18-bit Data
0	0	0	1	8080 MCU 9-bit Parallel	RDX	WRX	D/CX	D[8:0]: Unused, D[17:9] : 9-bit Data
0	0	1	0	8080 MCU 16-bit Parallel	RDX	WRX	D/CX	D9,D0: Unused, D[17:10],D[8:1]: 16-bit Data
0	0	1	1	8080 MCU 8-bit Parallel	RDX	WRX	D/CX	D[9:0]: Unused, D[17:10] : 8-bit Data
0	1	0	X	Serial interface	-	SCL	-	D[17:0]: Unused, Din+Dout: SDA
0	1	1	X	Setting disabled	-	-	-	-
1	0	0	0	6800 MCU 18-bit Parallel	E	WRX	RS	D[17:0]: 18-bit Data
1	0	0	1	6800 MCU 9-bit Parallel	E	WRX	RS	D[8:0]: Unused, D[17:9] : 9-bit Data
1	0	1	0	6800 MCU 16-bit Parallel	E	WRX	RS	D9,D0: Unused, D[17:10],D[8:1]: 16-bit Data
1	0	1	1	6800 MCU 8-bit Parallel	E	WRX	RS	D[9:0]: Unused, D[17:10] : 8-bit Data
1	1	0	X	Serial interface	-	SCL	-	D[17:0]: Unused, Din+Dout: SDA
1	1	1	X	Setting disabled	-	-	-	-

5.1.2 General Protocol

For programming of the LCD driver, the general supported protocol is shown in ***Fig. 5.1.1***

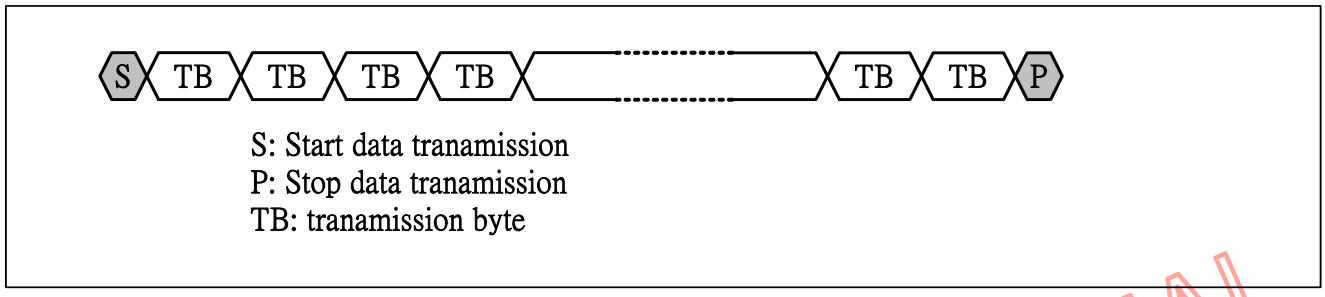


Fig. 5.1.1 Programming protocol

If data write or parameter write is interrupted by any other command, data write command or parameter write command should be done again to write the remained data or parameter.

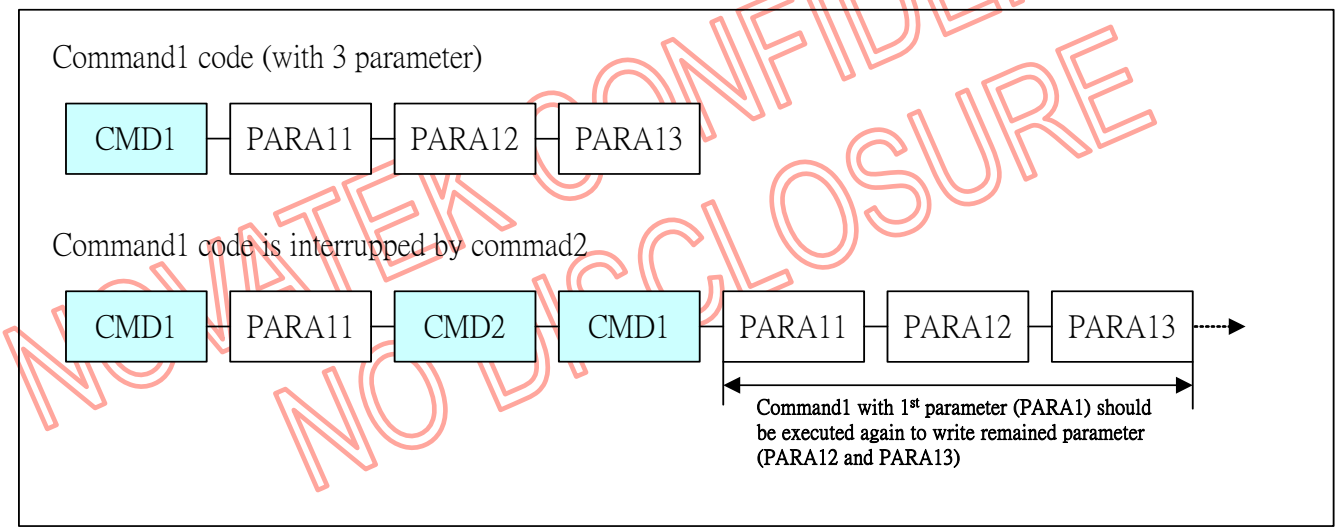


Fig. 5.1.2 Write interrupted sequence

5.1.3 80-Series Parallel Interface (P68 = "0")

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface or 12-wires 9-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (GND). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 8080-series parallel interface are given in ***Table 5.1.3.***

Table 5.1.3 Parallel Interface Function (80-series, P68="Low")

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	0	0	0	18-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
					1	↑	1	Read 18-bit display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	0	1	9-bit Parallel	0	1	↑	Write 8-bit command (D17 to D10)
					1	1	↑	Write 9-bit display data (D17 to D9) or 8-bit parameter (D17 to D10)
					1	↑	1	Read 9-bit display data (D17 to D9)
					1	↑	1	Read 8-bit parameter or status (D17 to D10)
0	0	1	0	16-bit Parallel	0	1	↑	Write 8-bit command (D8 to D1)
					1	1	↑	Write 16-bit display data (D17 to D10, D8 to D1) or 8-bit parameter (D8 to D1)
					1	↑	1	Read 16-bit display data (D17 to D10, D8 to D1)
					1	↑	1	Read 8-bit parameter or status (D8 to D1)
0	0	1	1	8-bit Parallel	0	1	↑	Write 8-bit command (D17 to D10)
					1	1	↑	Write 8-bit display data (D17 to D10) or 8-bit parameter (D17 to D10)
					1	↑	1	Read 8-bit display data (D17 to D10)
					1	↑	1	Read 8-bit parameter or status (D17 to D10)

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

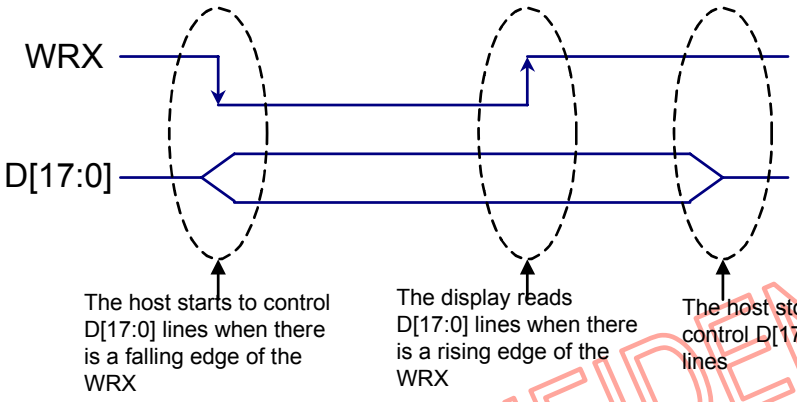


Fig. 5.1.3 8080-Series WRX Protocol

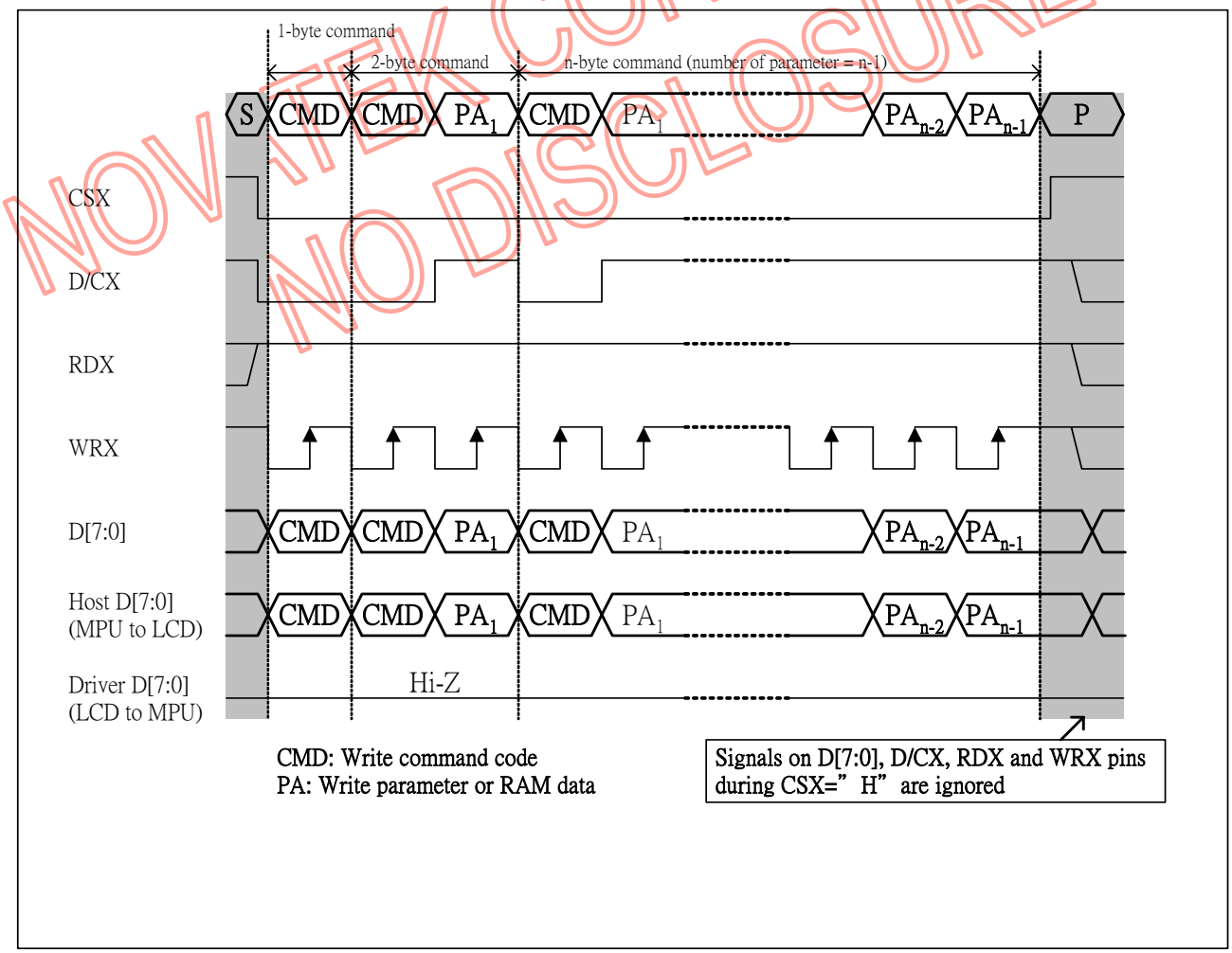


Fig. 5.1.4 80-Series parallel bus protocol, write to register or display RAM

Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

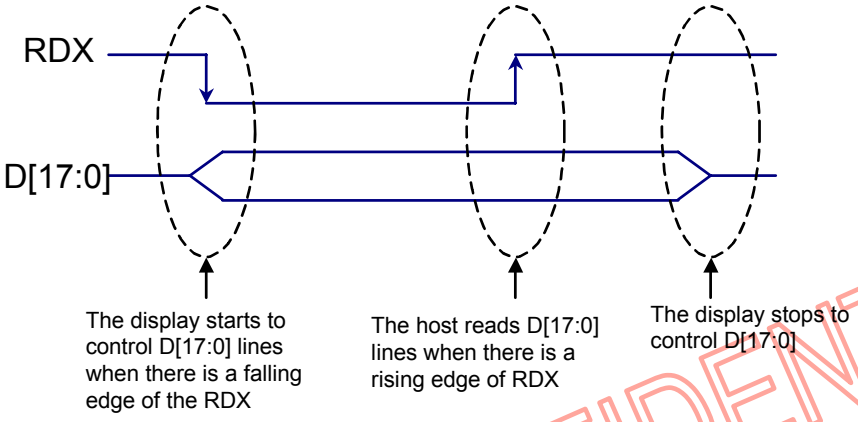


Fig. 5.1.5 8080-Series RDX Protocol

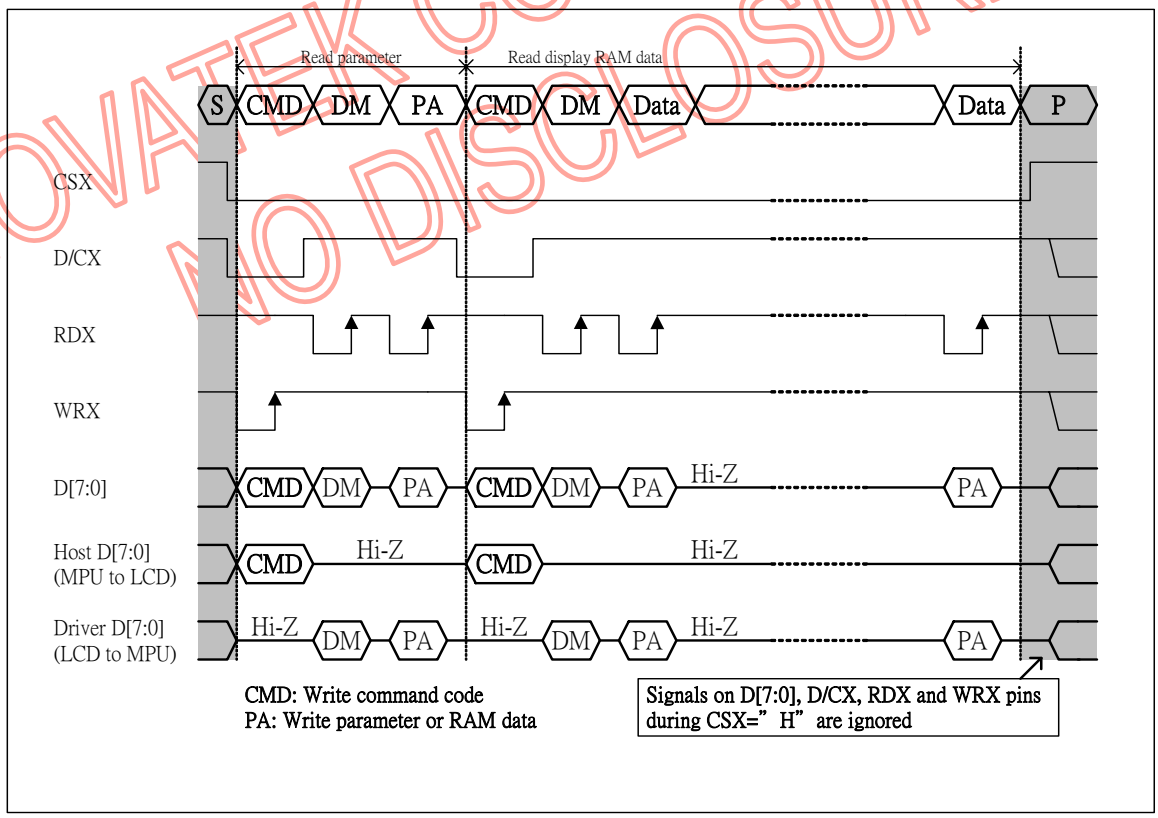


Fig. 5.1.6 80-Series parallel bus protocol, read from register

5.1.4 68-Series Parallel Interface (P68 = "1")

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface or 12-wires 9-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. The E is the parallel data Read/Write. The R/WX is the Read/Write flag and D[17:0] is parallel data.

The NT39125 reads the data at the falling edge of E signal when R/WX='1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (IOVCC). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in ***Table 5.1.4***

Table 5.1.4 Parallel Interface Function (68-series, P68="High")

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	0	0	0	18-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
					1	1	↓	Read 18-bit display data (D17 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	0	0	1	9-bit Parallel	0	0	↓	Write 8-bit command (D17 to D10)
					1	0	↓	Write 9-bit display data (D17 to D9) or 8-bit parameter (D17 to D10)
					1	1	↓	Read 9-bit display data (D17 to D9)
					1	1	↓	Read 8-bit parameter or status (D17 to D10)
1	0	1	0	16-bit Parallel	0	0	↓	Write 8-bit command (D8 to D1)
					1	0	↓	Write 16-bit display data (D17 to D10, D8 to D1) or 8-bit parameter (D8 to D1)
					1	1	↓	Read 16-bit display data (D17 to D10, D8 to D1)
					1	1	↓	Read 8-bit parameter or status (D8 to D1)
1	0	1	1	8-bit Parallel	0	0	↓	Write 8-bit command (D17 to D10)
					1	0	↓	Write 8-bit display data (D17 to D10) or 8-bit parameter (D17 to D10)
					1	1	↓	Read 8-bit display data (D17 to D10)
					1	1	↓	Read 8-bit parameter or status (D17 to D10)

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

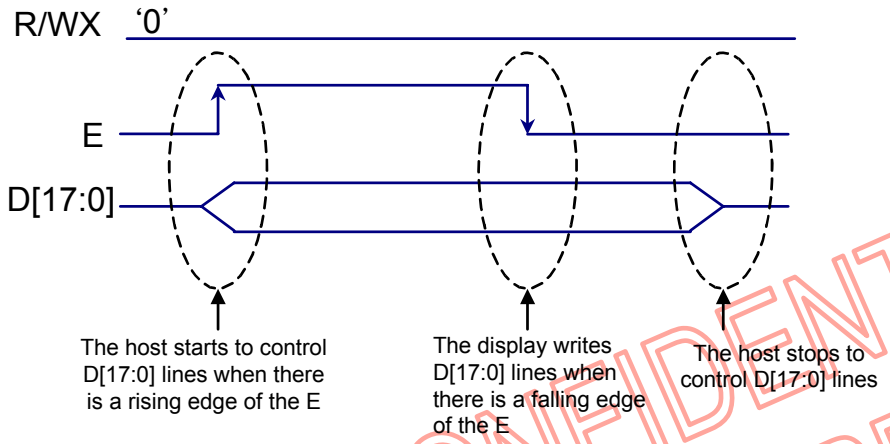


Fig. 5.1.7 6800-Series Write Protocol

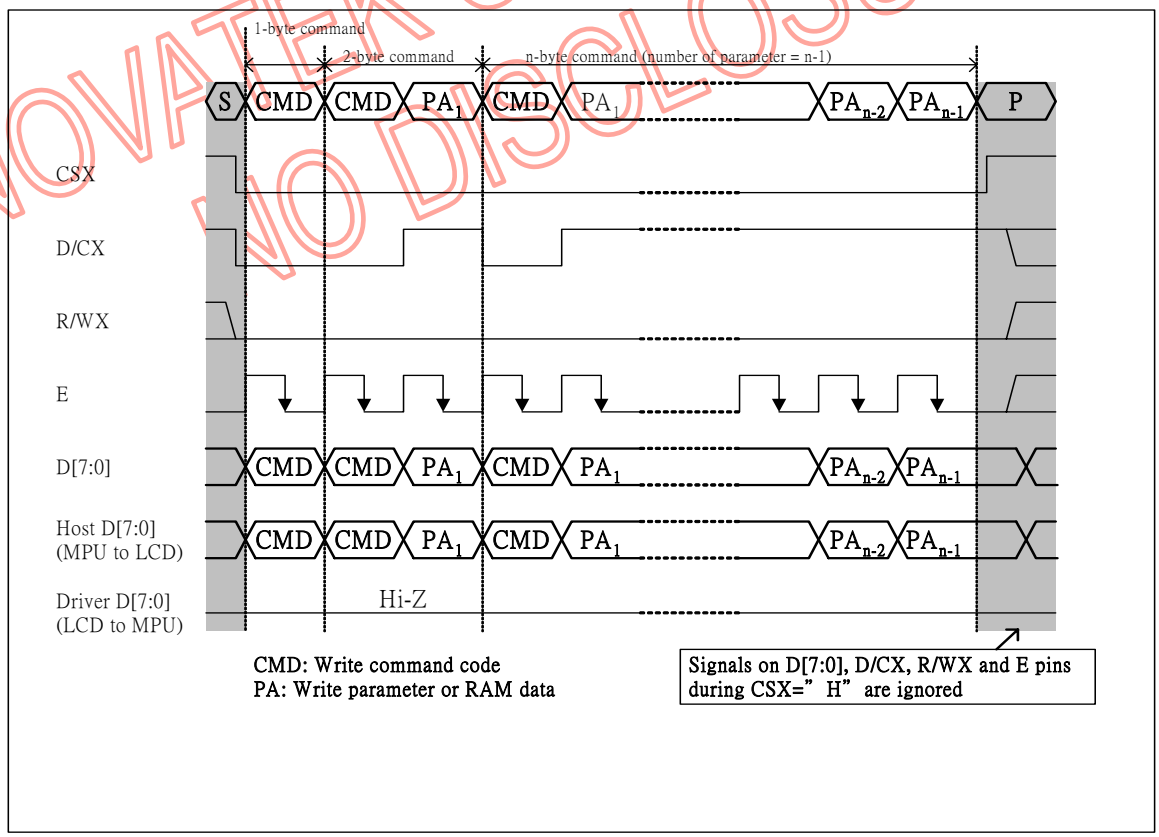


Fig. 5.1.8 68-Series parallel bus protocol, write to register or display RAM

Read cycle sequence

The write cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

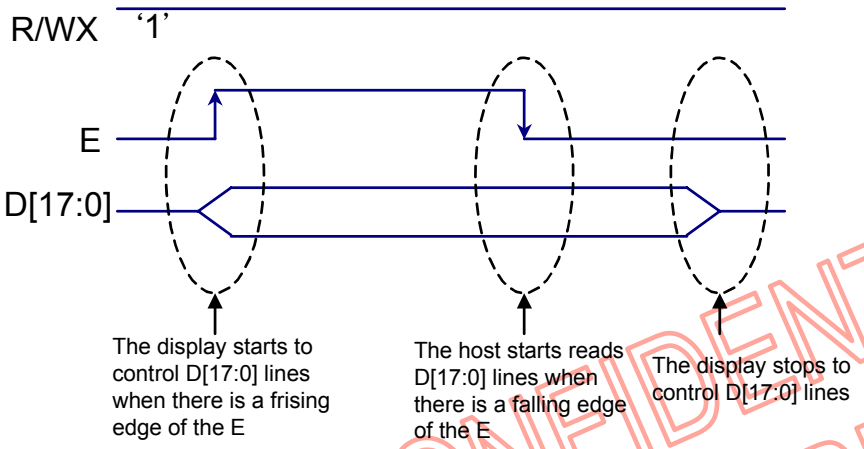


Fig. 5.1.9 6800-Series Read Protocol

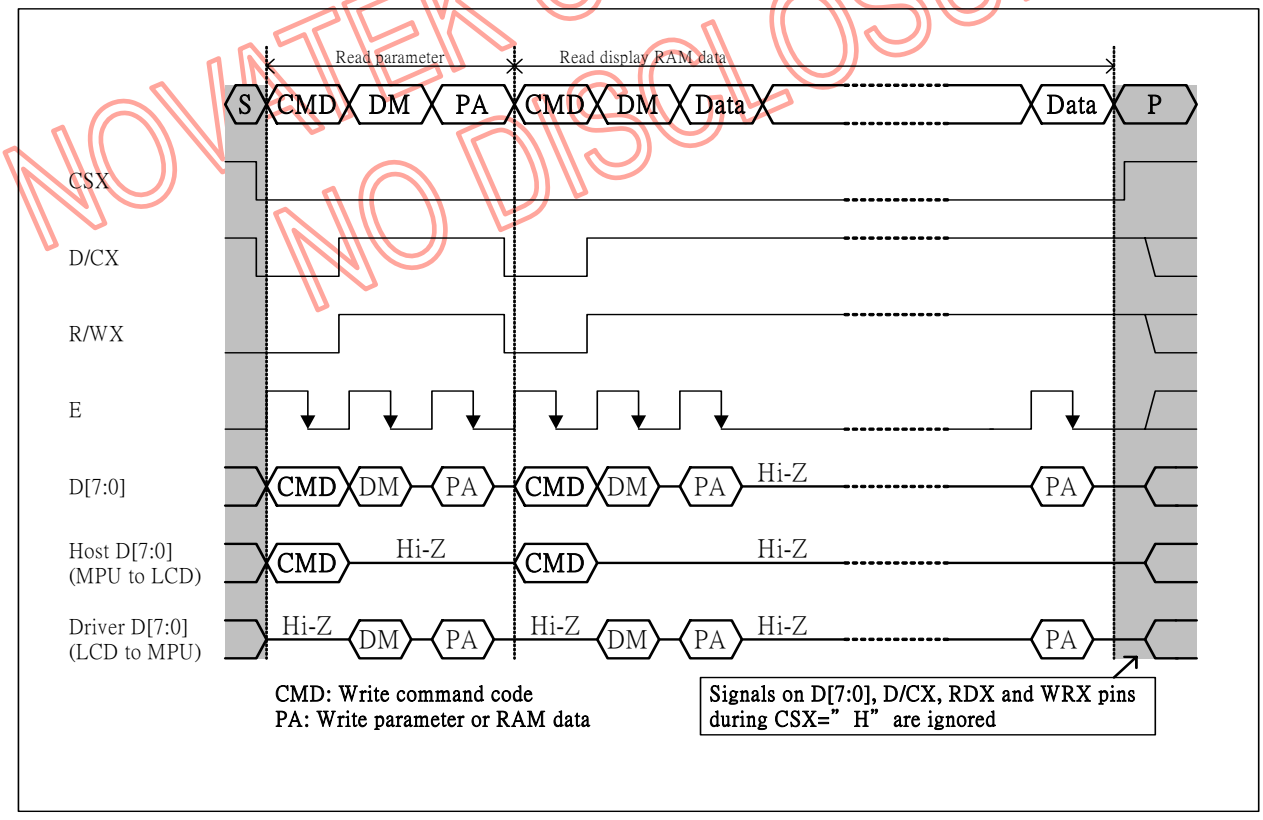


Fig. 5.1.10 68-Series parallel bus protocol, write to register or display RAM

5.1.5 Serial Interface

The selection of this interface is done by P68, IM2, IM1 and IM0.

The serial interface is a 3-pin or 4-pin bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: SCEX (chip enable), SCL (serial clock) and SDA (serial data input/output) and 4-pin serial use: SCEX (chip enable), D/CX (data / command select), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

5.1.5.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT39125. 3-Pin serial data packet contains a control bit D/CX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit D/CX is transferred by D/CX pin. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the NT39125. The MSB is transmitted first. The serial interface is initialized when SCEX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on SCEX enables the serial interface and indicates the start of data transmission.

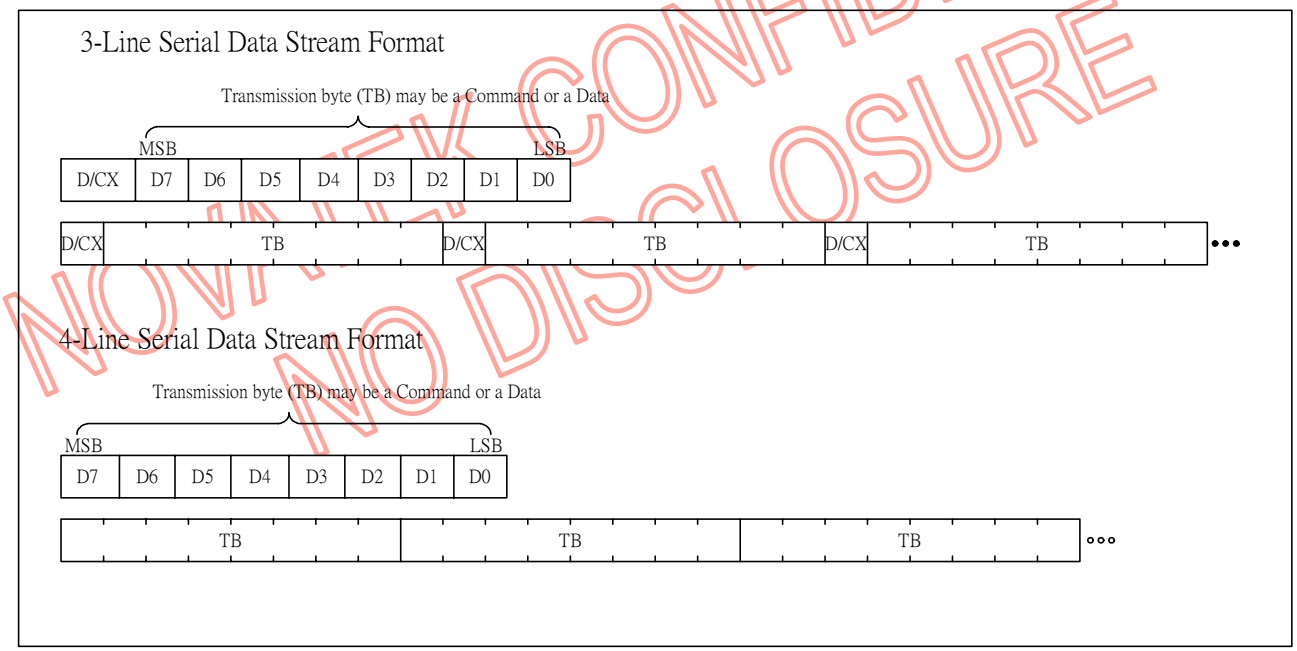


Fig. 5.1.11 Serial data stream, write mode

When SCEX is high, SCL clock is ignored. During the high time of SCEX the serial interface is initialized. At the falling SCEX edge, SCL can be high or low (see ***Fig 5.1.12***). SDA is sampled at the rising edge of SCL. D/CX indicates, whether the byte is command code (D/CX=0) or parameter/RAM data (D/CX=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCLK edge (4-line serial interface). If SCEX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

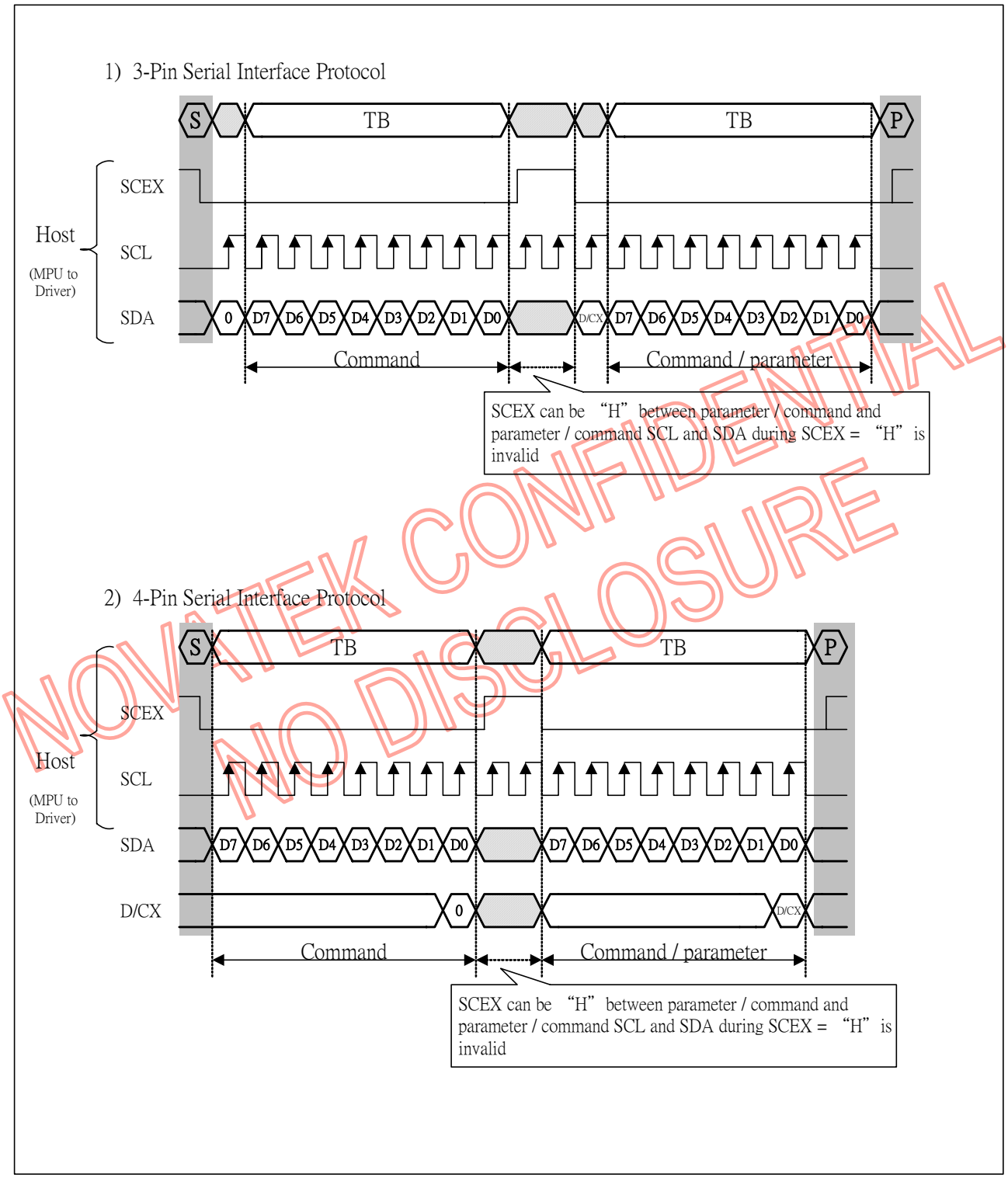


Fig. 5.1.12 Serial bus protocol, write to register with control bit in transmission

5.1.5.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT39125. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that SCEX is required to go high before a new command is send (see ***Fig. 5.1.13*** and ***Fig. 5.1.14***). The NT39125 samples the SDA (input data) at the rising edges, but shifts SDA (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling SCL edge of the last bit (see ***Fig. 5.1.13*** and ***Fig. 5.1.14***).

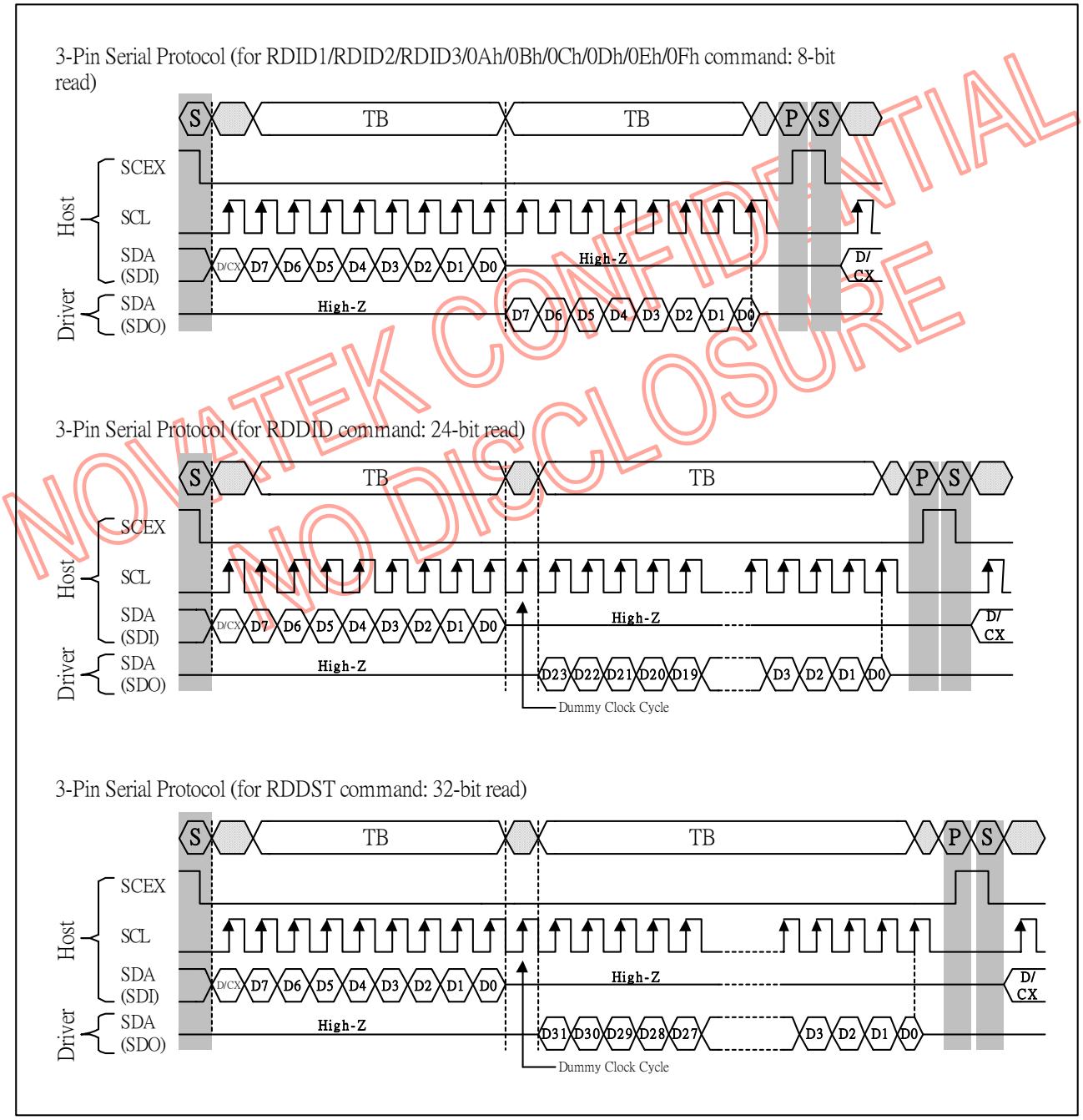


Fig. 5.1.13 Serial bus protocol, read mode (3-Pin serial interface case)

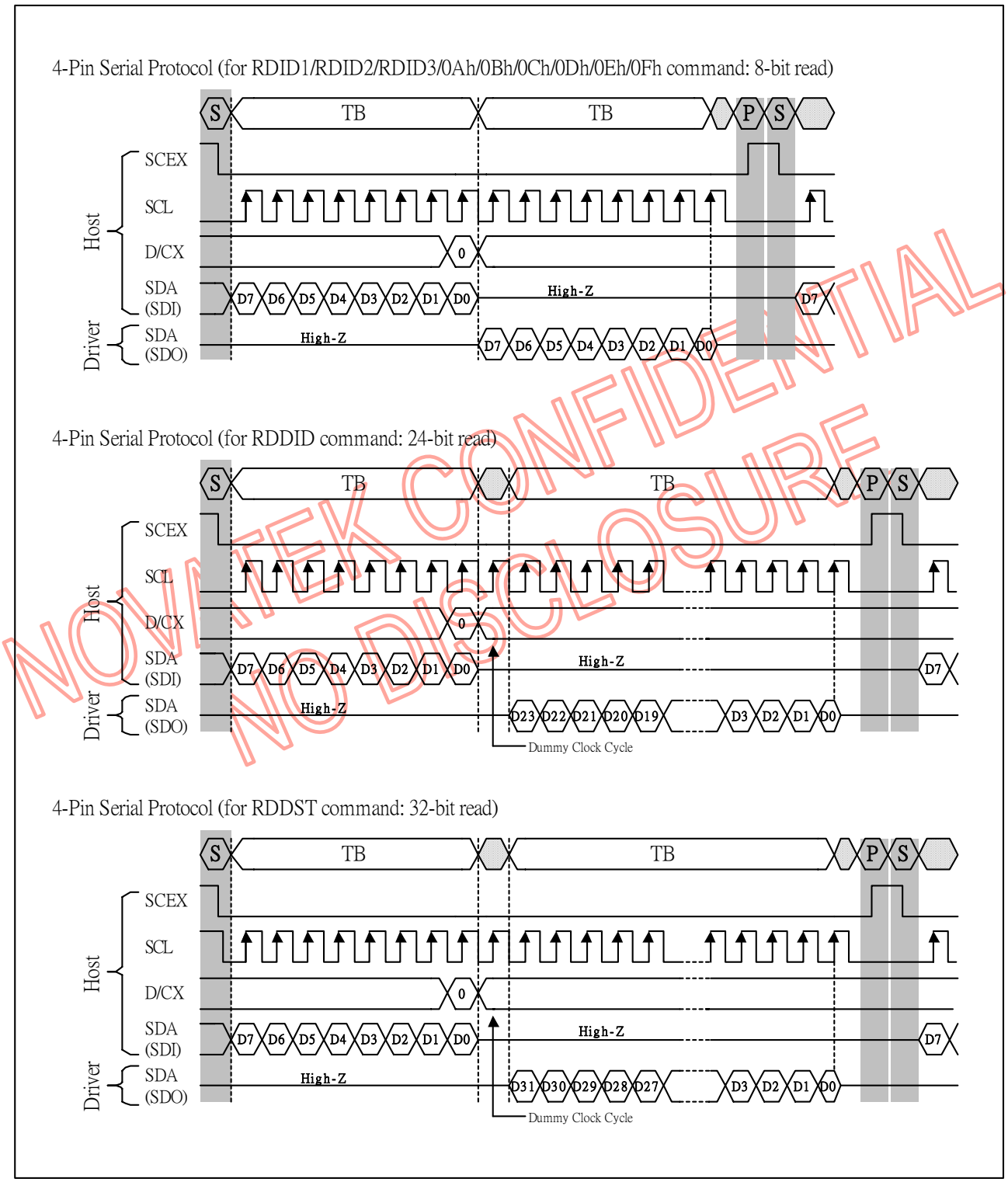


Fig. 5.1.14 Serial bus protocol, read mode (4-Pin serial interface case)

5.1.6 Interface Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT39125 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

5.1.6.1 PARALLEL INTERFACE PAUSE

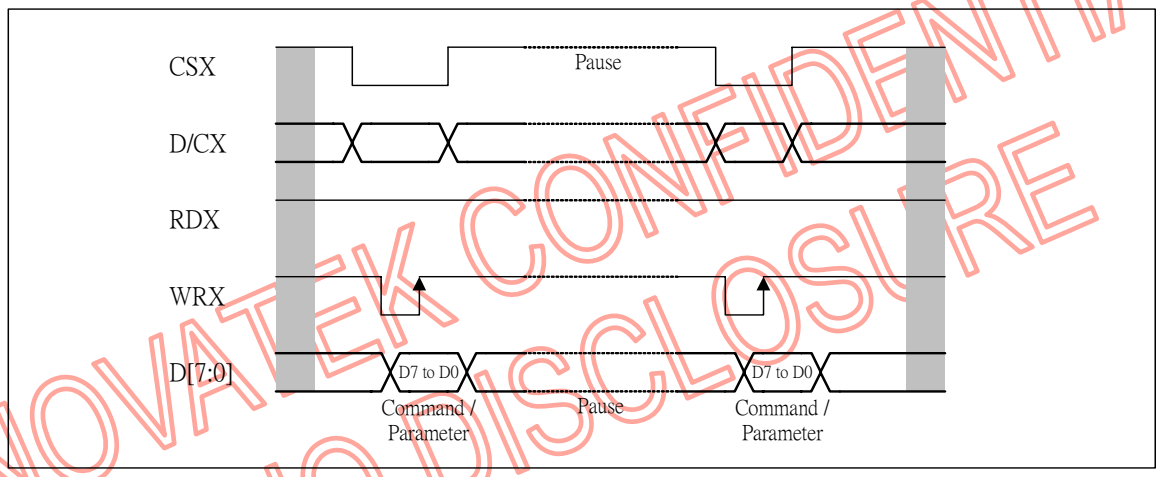


Fig. 5.1.15 Parallel bus protocol, write mode – paused by CSX

5.1.6.2 SERIAL INTERFACE PAUSE

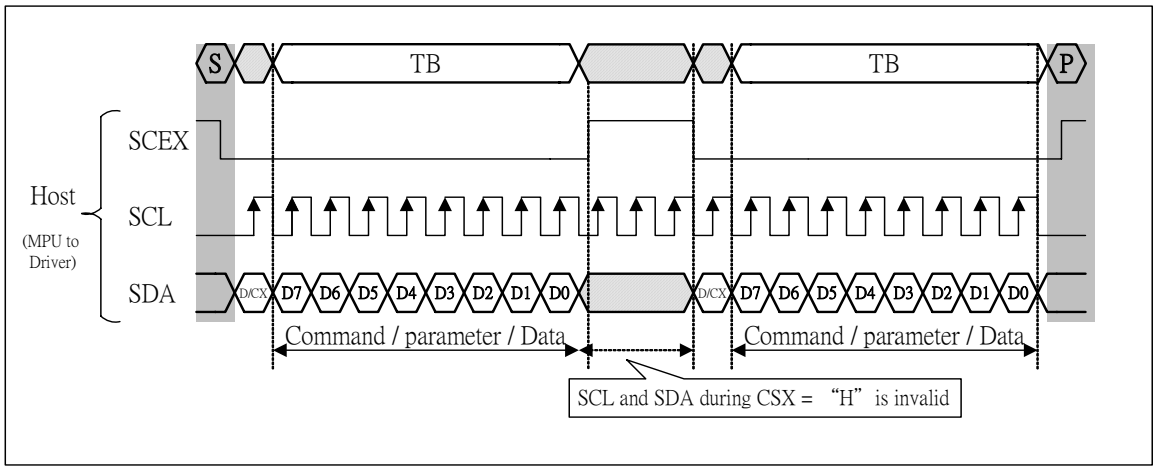


Fig. 5.1.16 Serial bus protocol, write mode – paused by SCEX (3-Pin serial case)

5.1.7 Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT39125 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (SCEX) is next activated after RESX have been High state. See the following example (See ***Fig. 5.1.17***)

If there is a break in data transmission by SCEX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT39125 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (SCEX) is next activated. See the following example (See ***Fig. 5.1.18***)

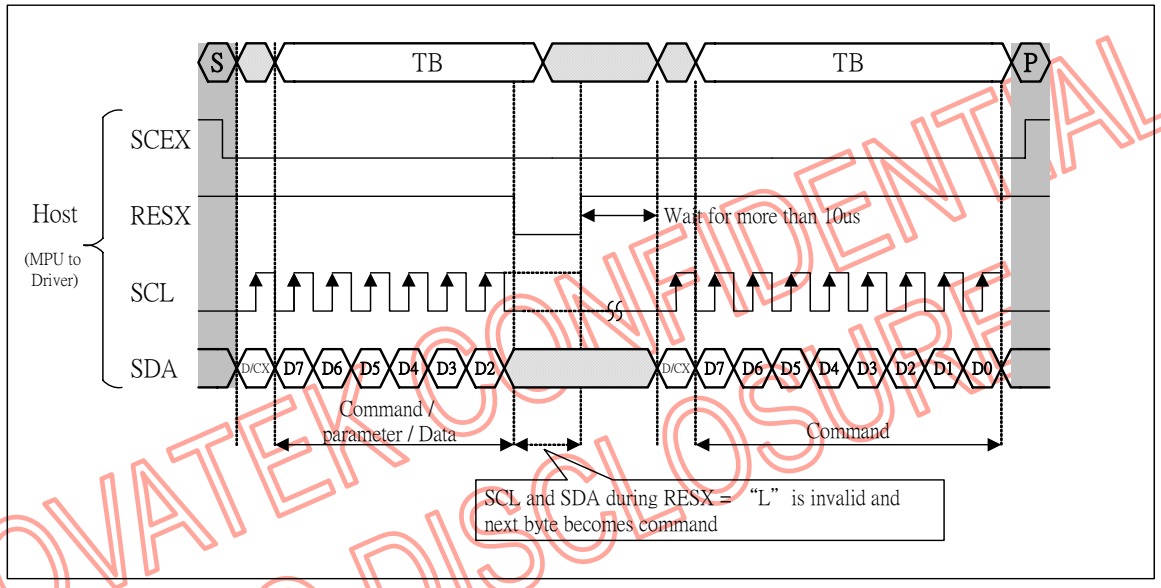


Fig. 5.1.17 Serial bus protocol, write mode – interrupted by RESX

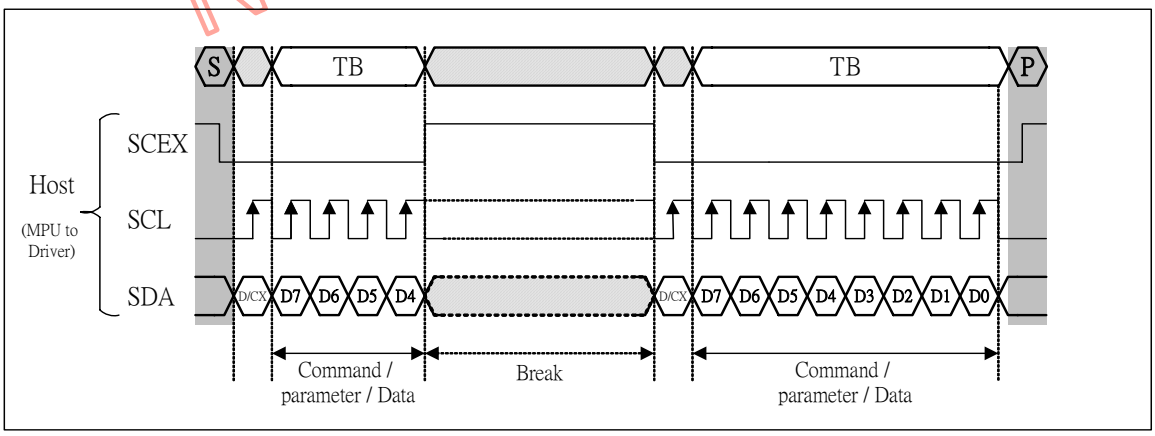


Fig. 5.1.18 Serial bus protocol, write mode – interrupted by SCEX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in ***Fig. 5.1.19***.

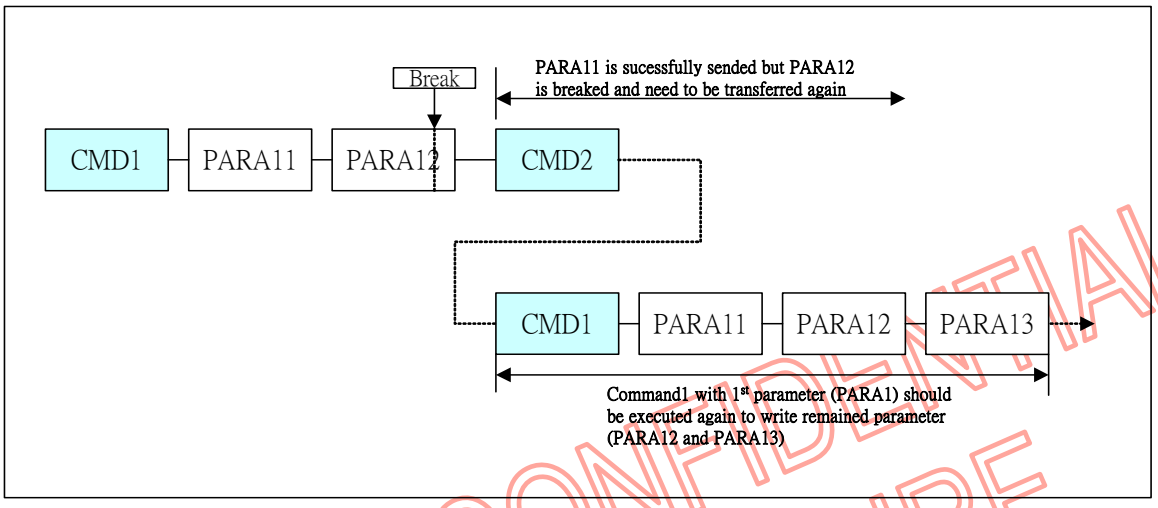


Fig. 5.1.19 Write interrupt recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

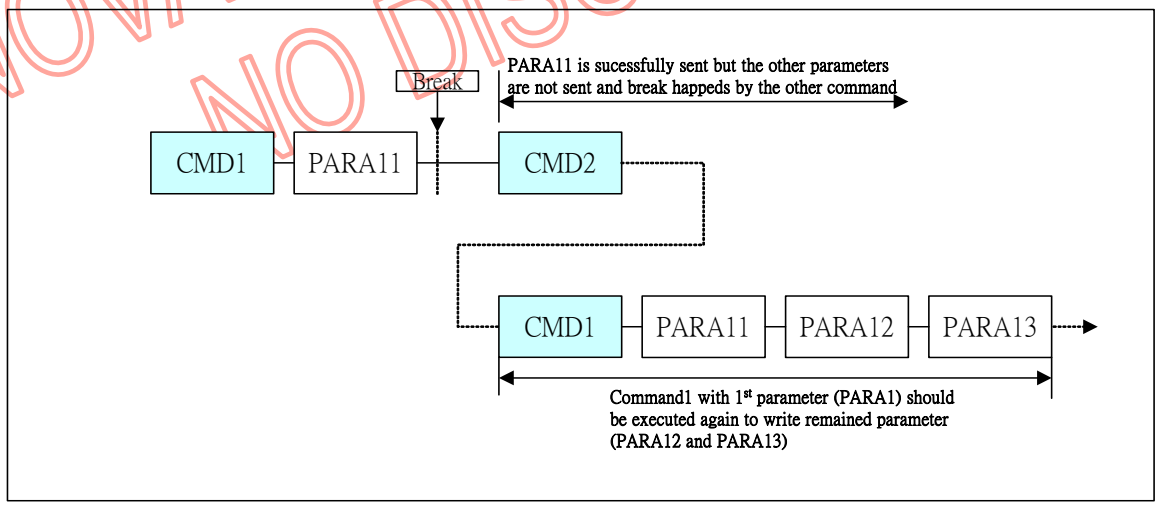


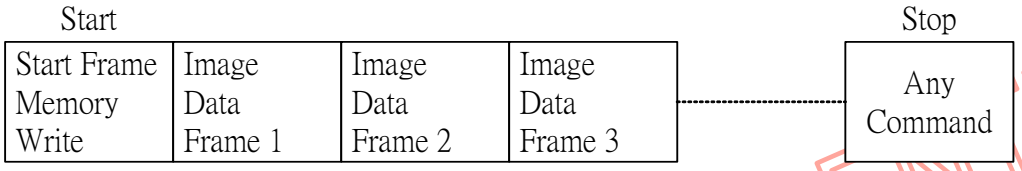
Fig. 5.1.20 Write interrupt recovery (both serial and parallel interface)

5.1.8 Display Module Data Transfer Modes

The Module has 3 color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

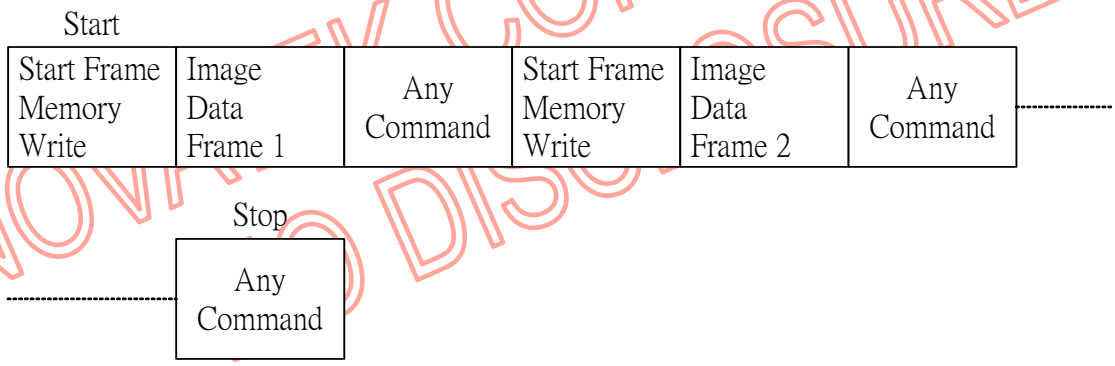
5.1.8.1 METHOD 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



5.1.8.2 METHOD 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

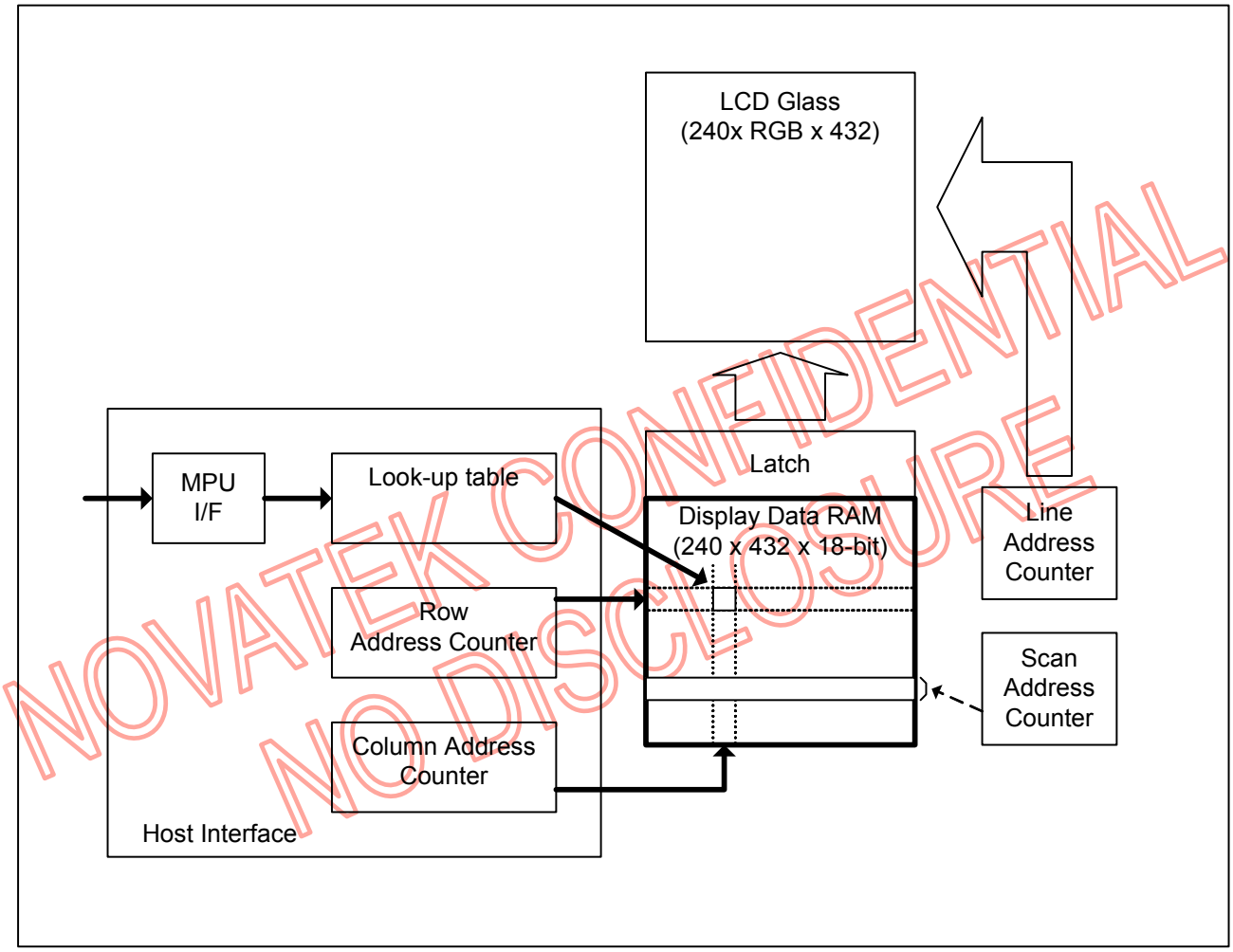
1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

2) The Frame Memory can contain numbers of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 DISPLAY DATA RAM (DDRAM)

The NT39125 has an integrated 240x432x18-bit graphic type static RAM. This 1.86M-bit memory allows to store on-chip a 240xRGBx432 image with an 18-bit resolution (262k-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



5.2.1 Display Data Formats

5.2.1.1 3-PINS SERIAL INTERFACE FOR DATA RAM WRITE (IM2, IM1, IM0=”10X”, 4WSPI = ‘0’)

Different display data formats are available for four colors depth supported by the LCM listed below.

-4k colors, RGB 4,4,4-bits input

-65k colors, RGB 5,6,5-bits input

-262k colors, RGB 6,6,6-bits input

Table 5.2.1.1.1 3-pins SPI write data for RGB 4-4-4-bits input

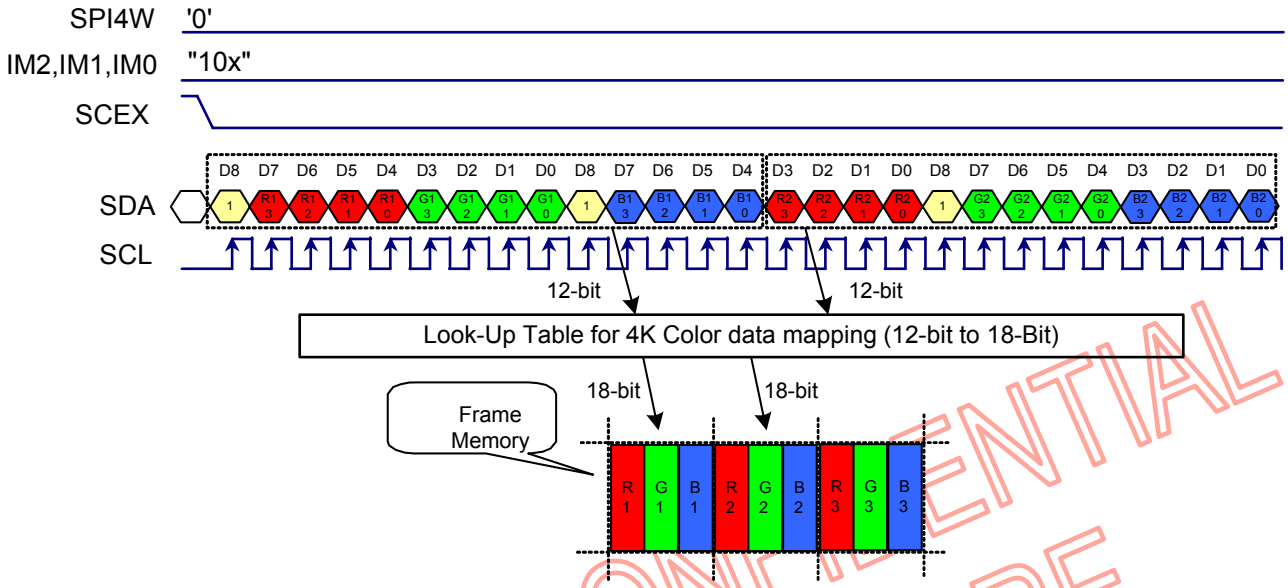


Table 5.2.1.1.2 3-pins SPI write data for RGB 5-6-5-bits input

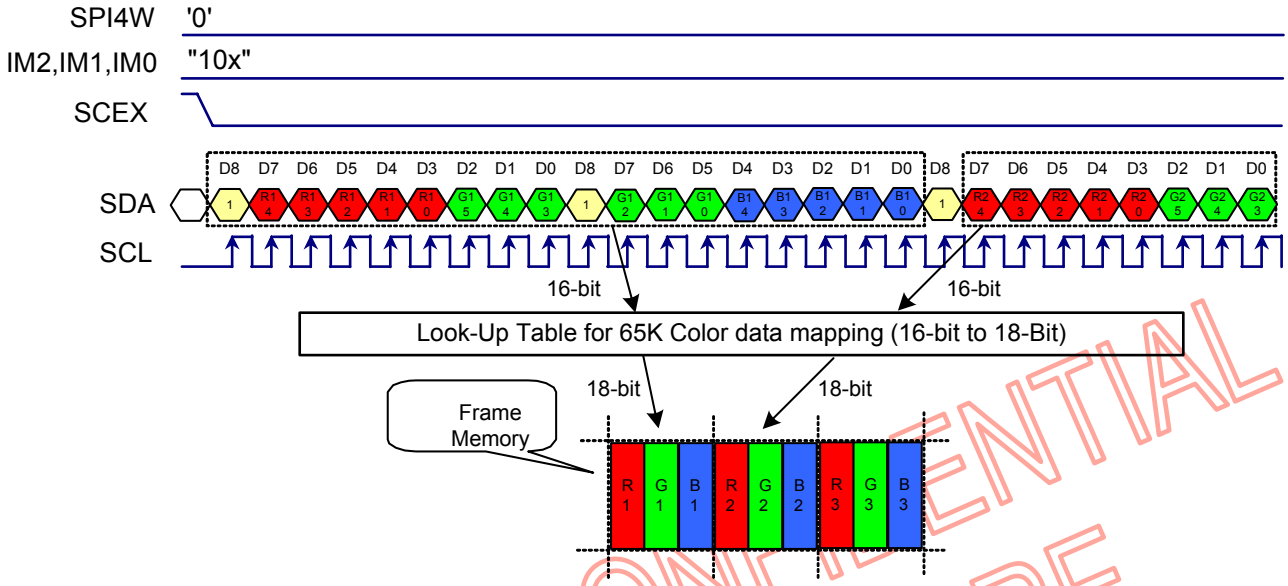
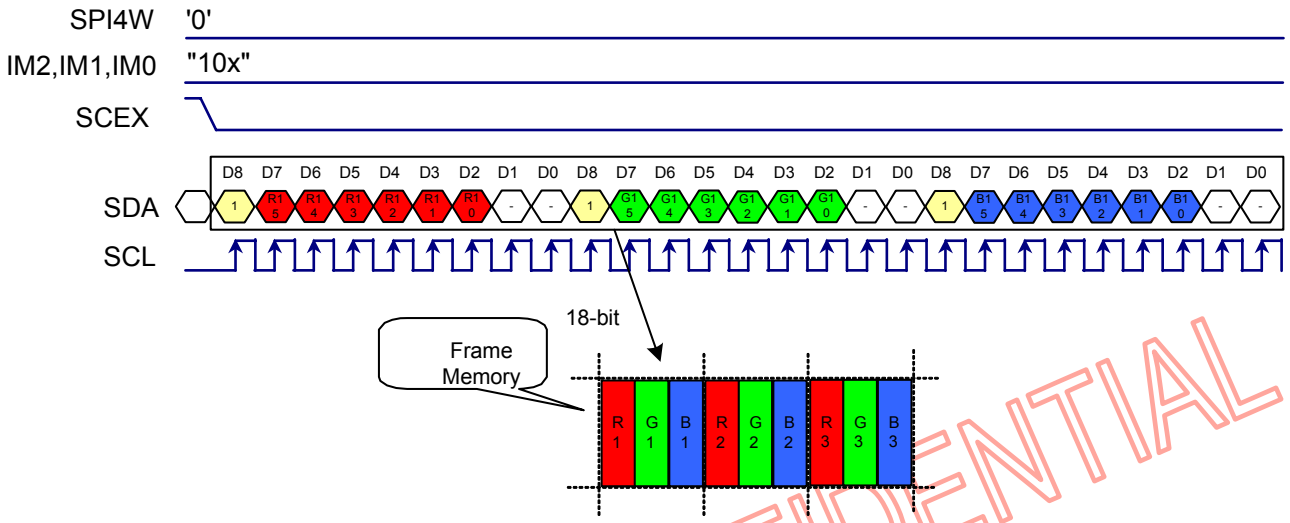


Table 5.2.1.1.3 3-pins SPI write data for RGB 6-6-6-bits input



5.2.1.2 4-PINS SERIAL INTERFACE FOR DATA RAM WRITE(IM2, IM1, IM0="10X", 4WSPI = '1')

Different display data formats are available for four colors depth supported by the LCM listed below.

-4k colors, RGB 4,4,4-bits input

-65k colors, RGB 5,6,5-bits input

-262k colors, RGB 6,6,6-bits input

Table 5.2.1.2.1 4-pins SPI write data for RGB 4-4-4-bits input

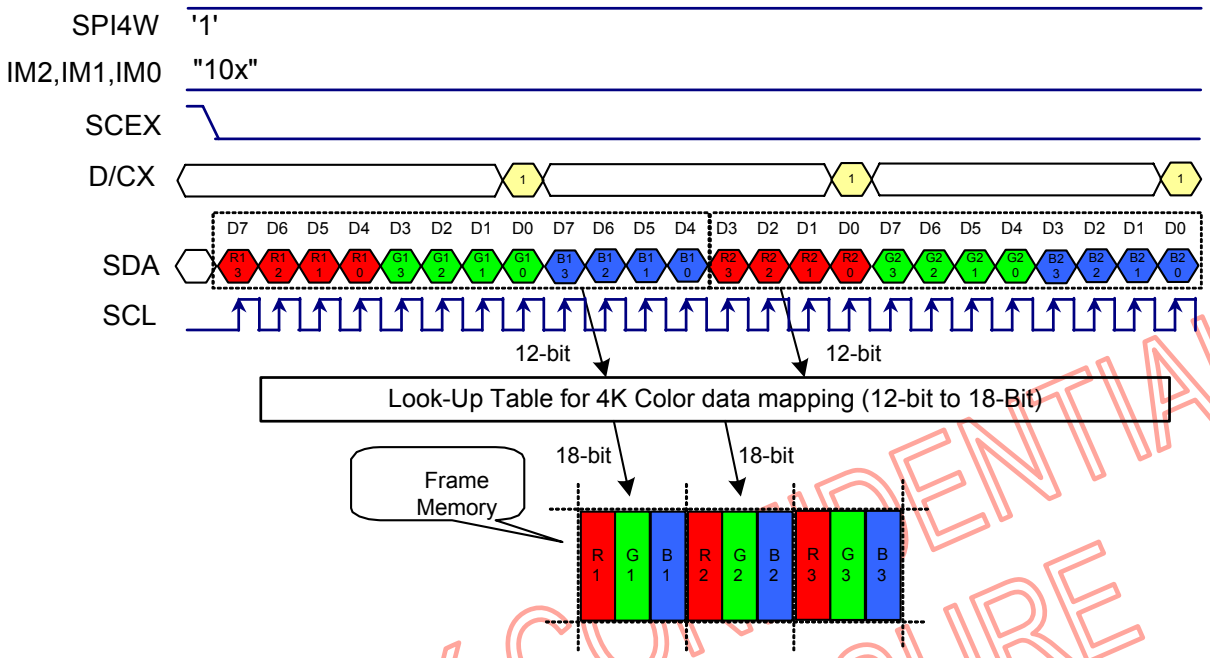


Table 5.2.1.2.2 4-pins SPI write data for RGB 5-6-5-bits input

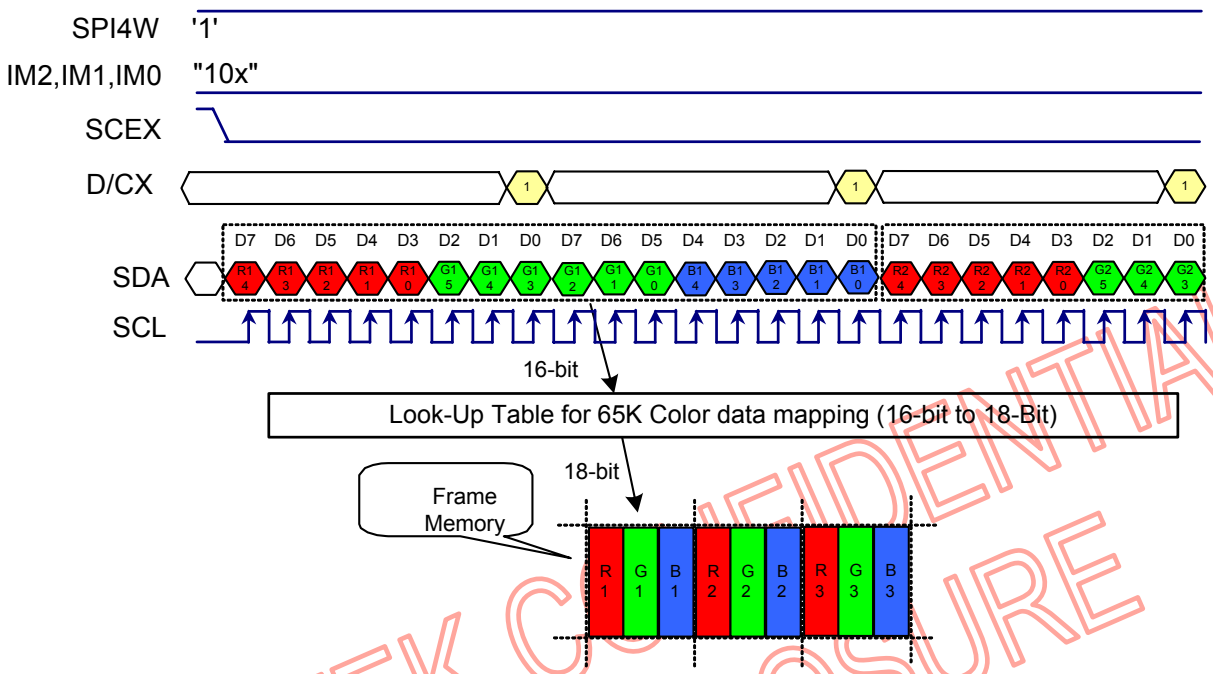
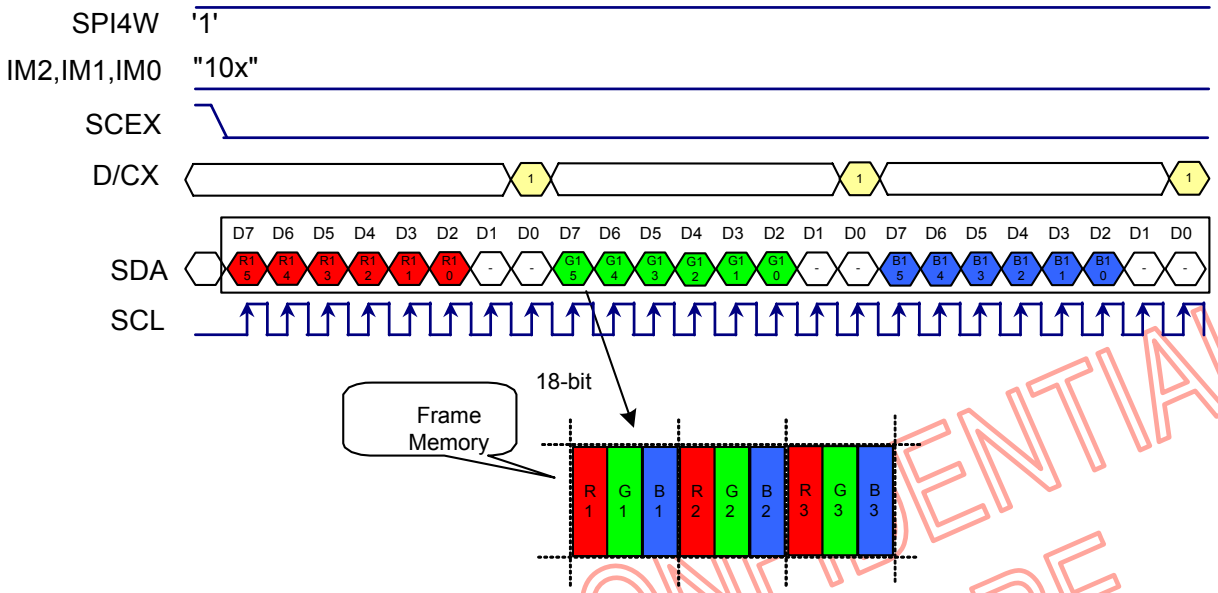


Table 5.2.1.2.3 4-pins SPI write data for RGB 6-6-6-bits input



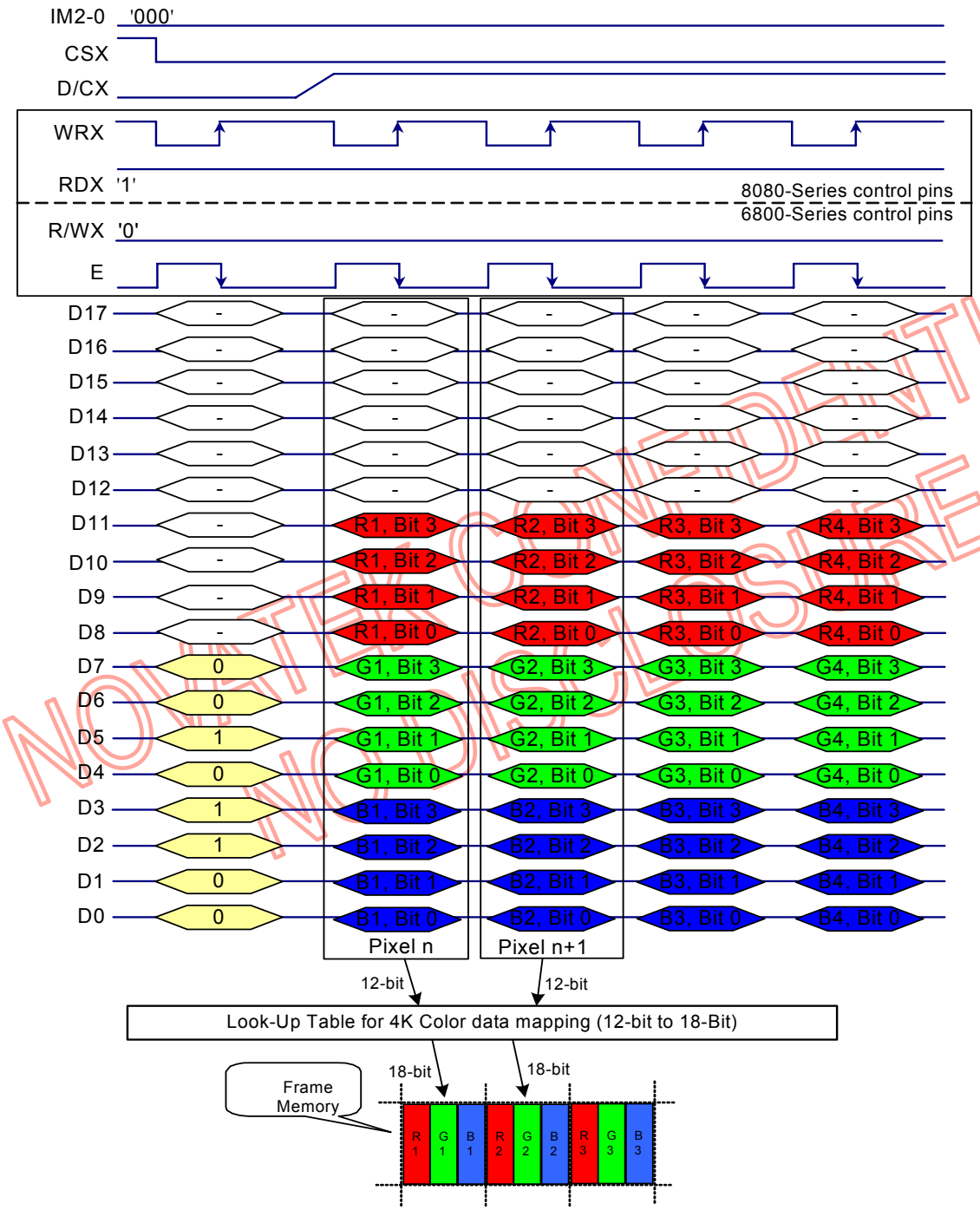
5.2.1.3 18-BIT PARALLEL INTERFACE FOR DATA RAM WRITE (IM2, IM1, IM0= “000”)

Different display data formats are available for four colors depth supported by the NT39125 listed below.
-4k colors, RGB 4,4,4-bits input
-65k colors, RGB 5,6,5-bits input
-262k colors, RGB 6,6,6-bits input

Table 5.2.1.3.1 18-Bits Parallel Interface Set Table

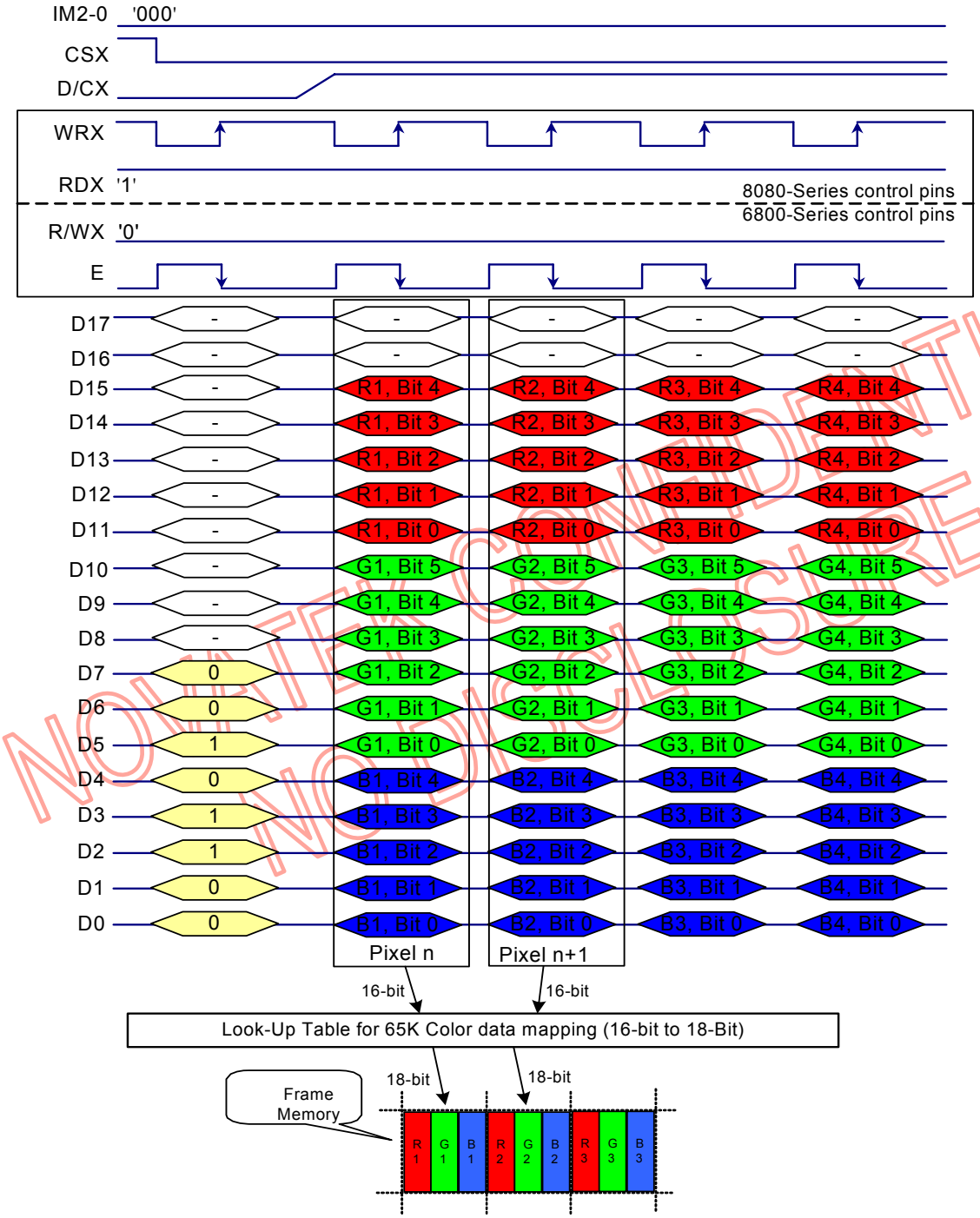
Register	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4096-Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.2.1.3.2 Write 18-bit data for RGB 4-4-4-bits input



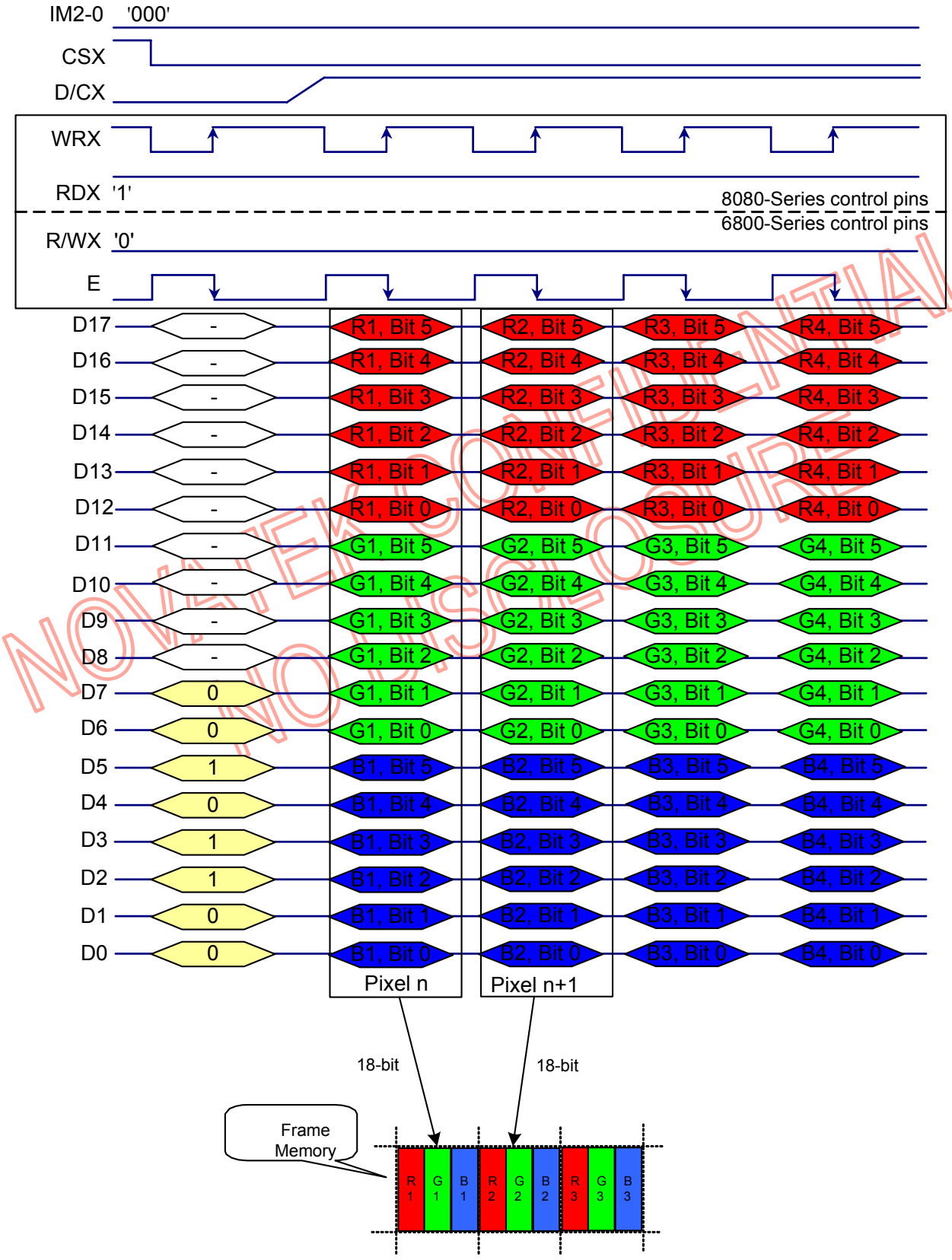
Note: '-' = Don't care - Can be set to '0' or '1'

Table 5.2.1.3.3 Write 18-bit data for RGB 5-6-5-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

Table 5.2.1.3.4 Write 18-bit data for RGB 6-6-6-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

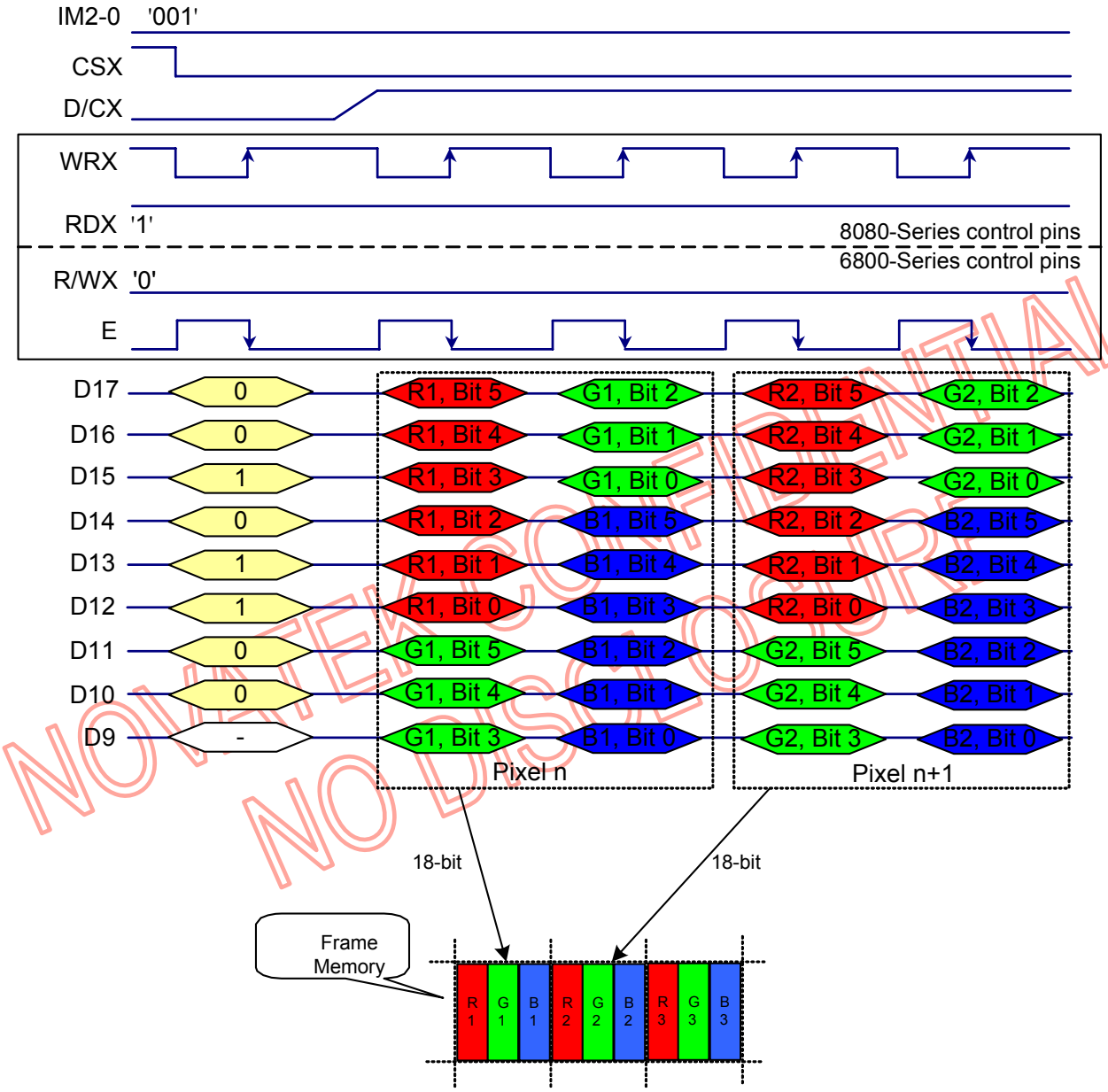
5.2.1.4 9-BIT PARALLEL INTERFACE FOR DATA RAM WRITE (IM2, IM1, IM0="001")

Different display data formats are available for four colors depth supported by the NT39125 listed below.
-4k colors, RGB 4,4,4-bits input
-65k colors, RGB 5,6,5-bits input
-262k colors, RGB 6,6,6-bits input

Table 5.2.1.4.1 9-Bits Parallel Interface Set Table

Register	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	0	0	1	0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	2Ch
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.2.1.4.2 Write 9-bit data for RGB 6-6-6-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

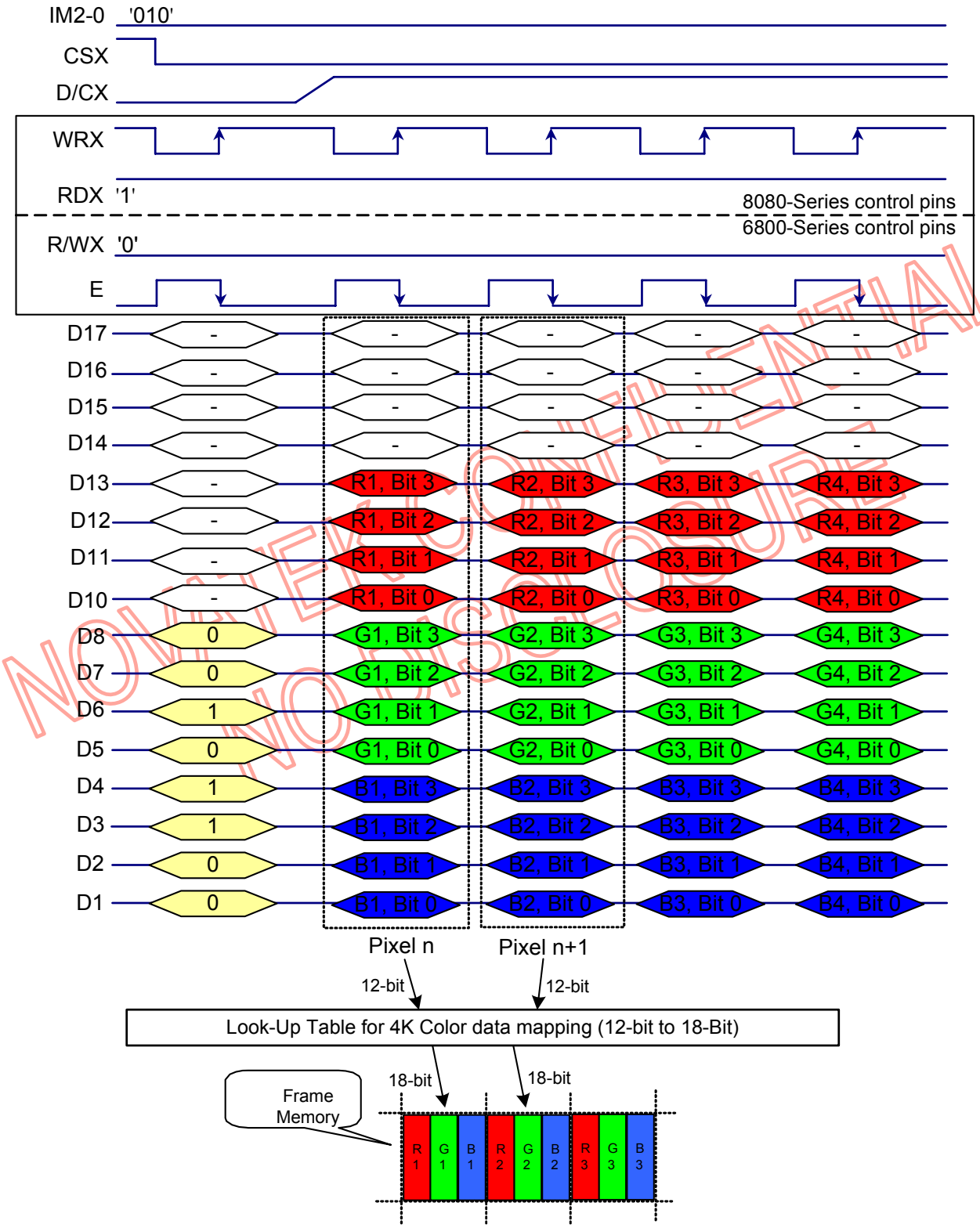
5.2.1.5 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE (IM2, IM1, IM0="010")

Different display data formats are available for four colors depth supported by the NT39125 listed below.
-4k colors, RGB 4,4,4-bits input
-65k colors, RGB 5,6,5-bits input
-262k colors, RGB 6,6,6-bits input

Table 5.2.1.5.1 16-Bits Parallel Interface Set Table

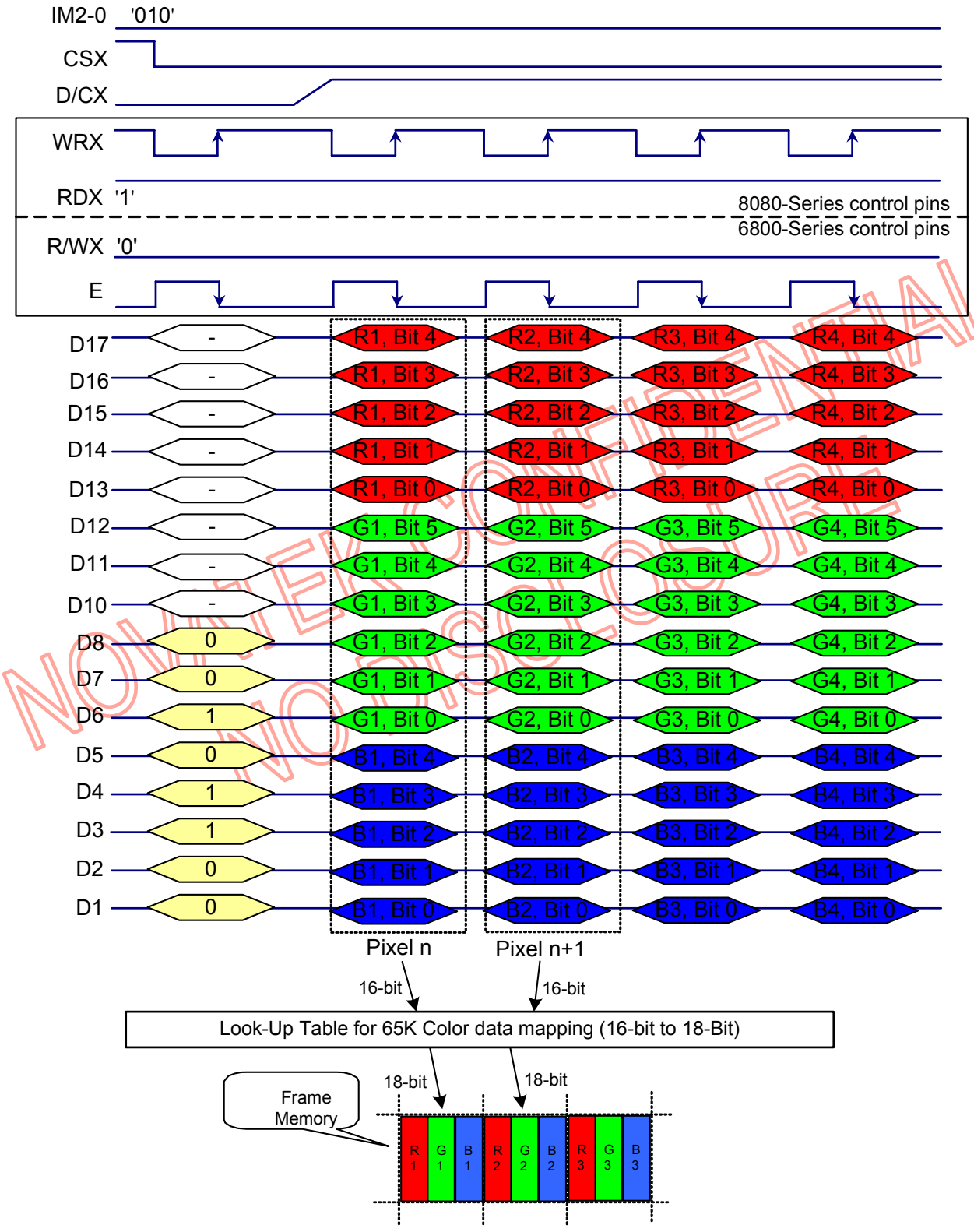
Register	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	x	2Ch
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4096-Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	(1-pixels/
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	3bytes)

Table 5.2.1.5.2 Write 16-bit data for RGB 4-4-4-bits input



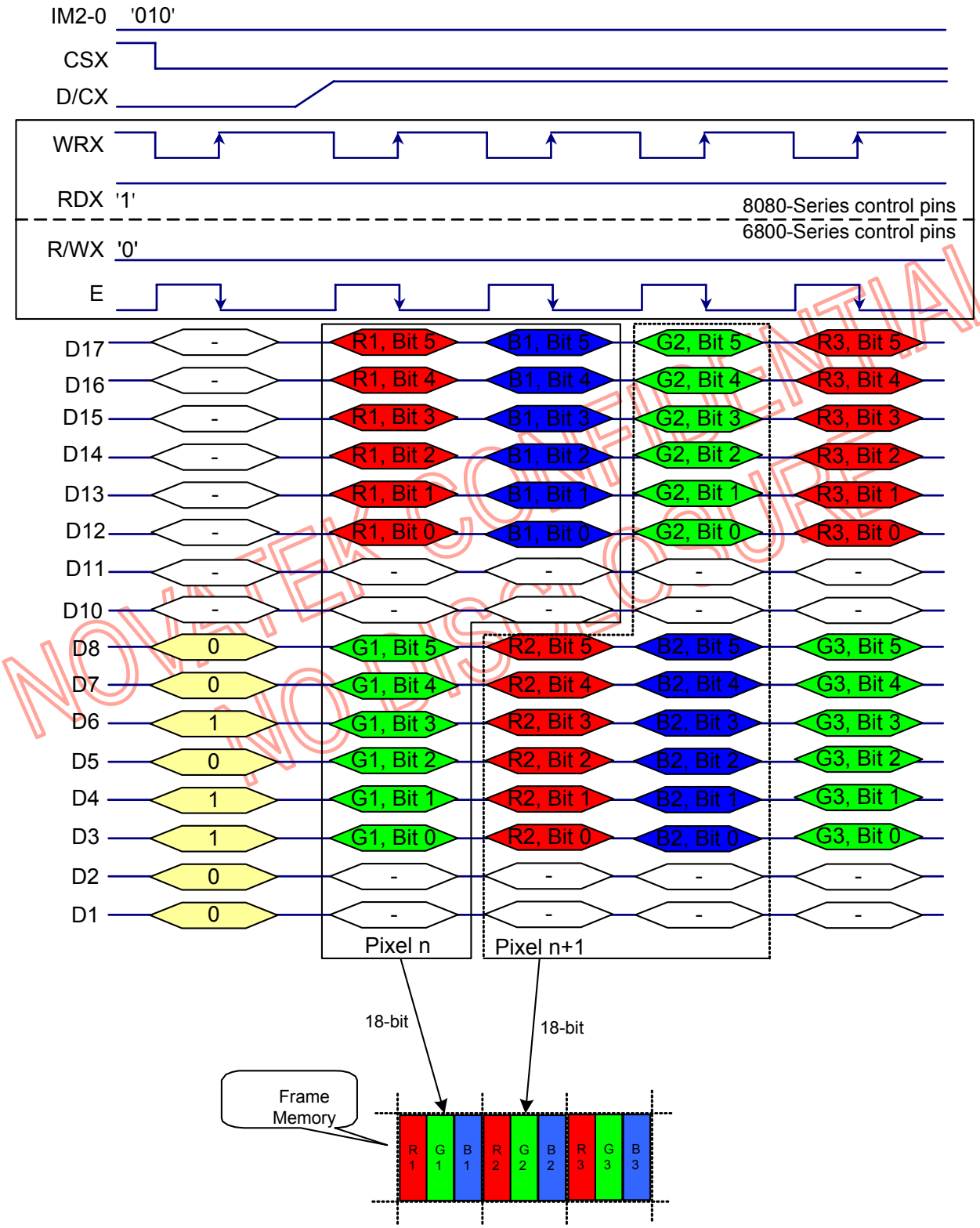
Note: '-' = Don't care - Can be set to '0' or '1'

Table 5.2.1.5.3 Write 16-bit data for RGB 5-6-5-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

Table 5.2.1.5.4 Write 16-bit data for RGB 6-6-6-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

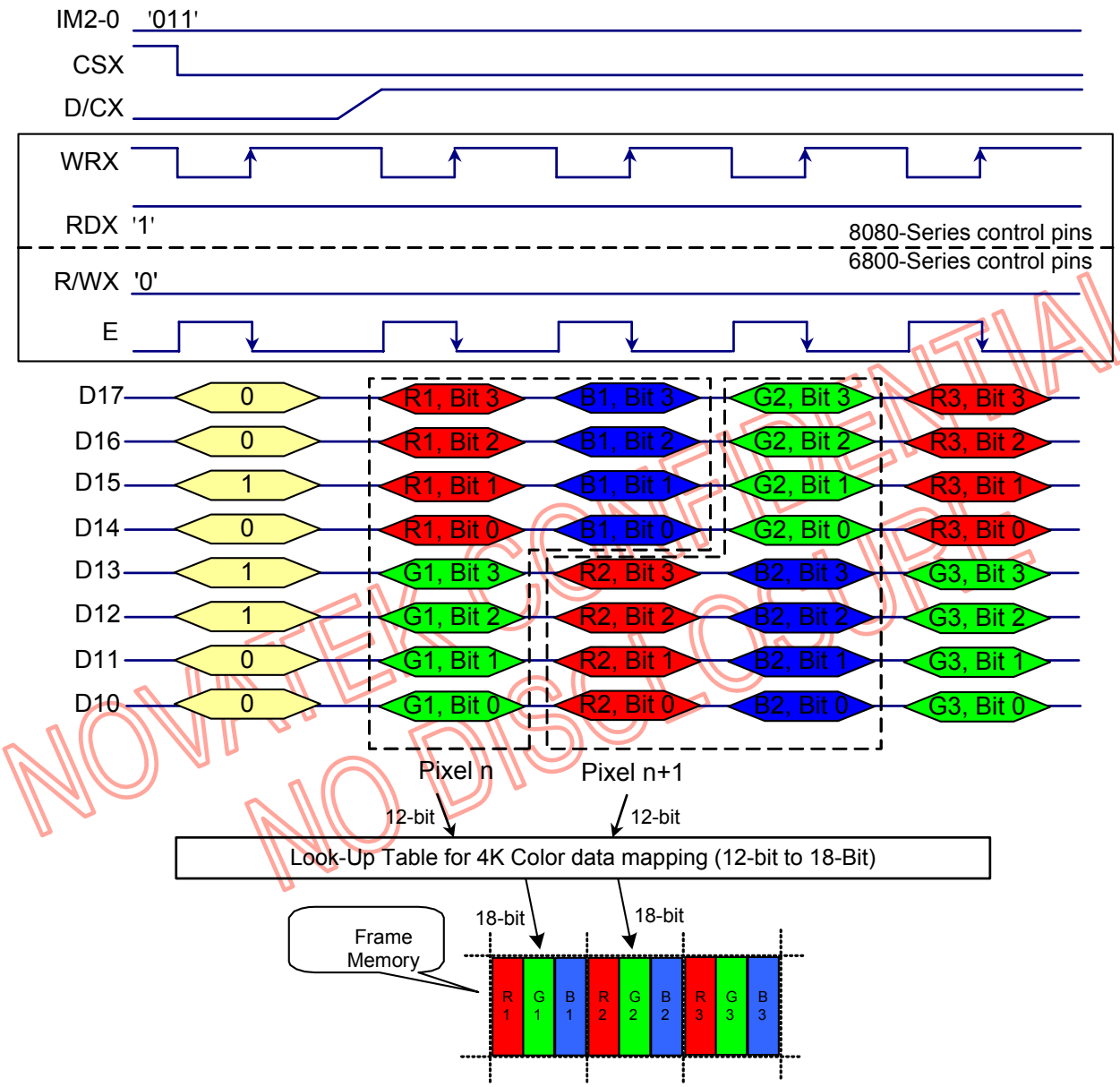
5.2.1.6 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE (IM2, IM1, IM0="011")

Different display data formats are available for four colors depth supported by the NT39125 listed below.
-4k colors, RGB 4,4,4-bits input
-65k colors, RGB 5,6,5-bits input
-262k colors, RGB 6,6,6-bits input

Table 5.2.1.6.1 8-Bits Parallel Interface Set Table

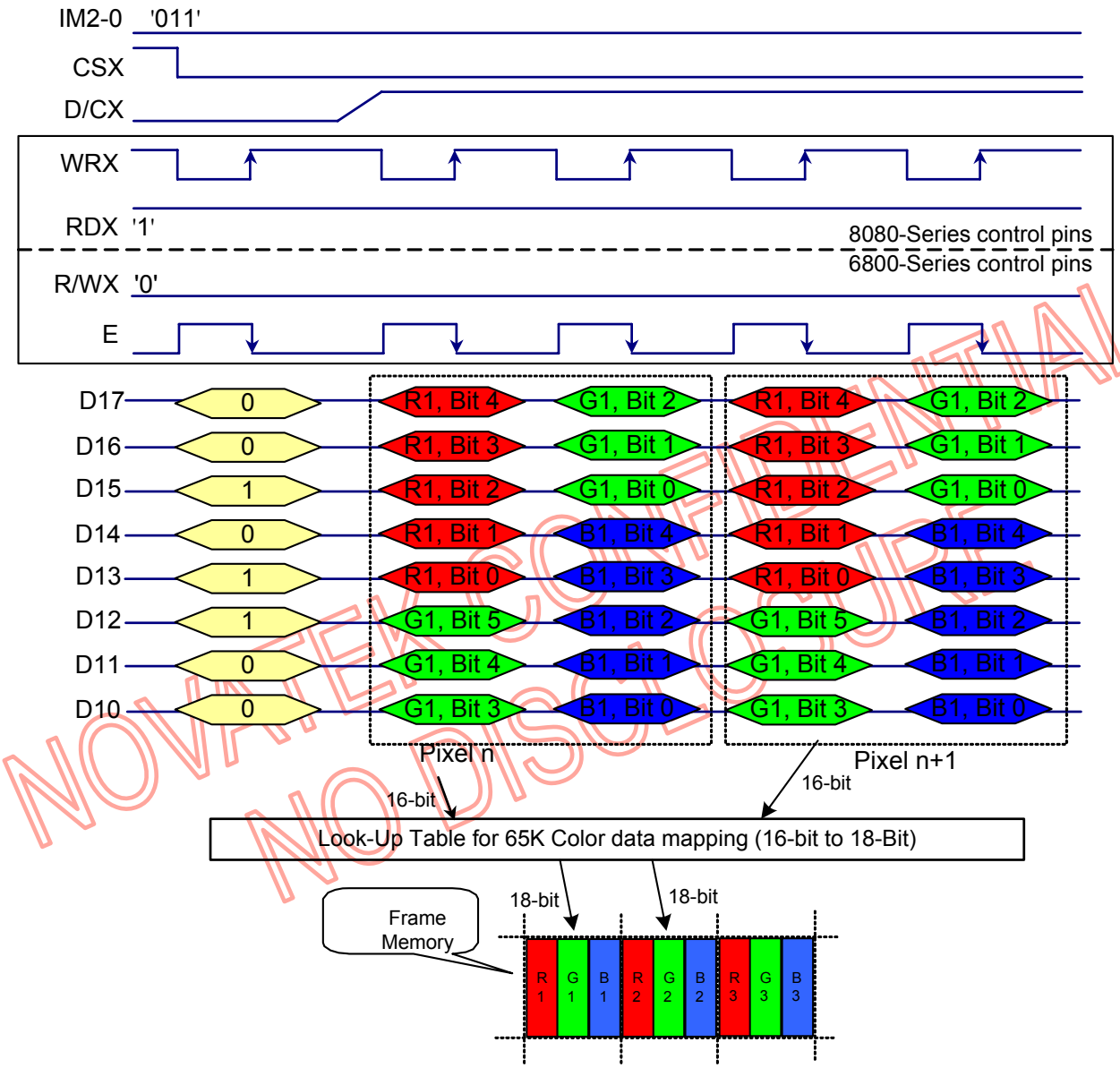
Register	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	0	0	1	0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	2Ch
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4096-Color
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.2.1.6.2 Write 8-bit data for RGB 4-4-4-bits input



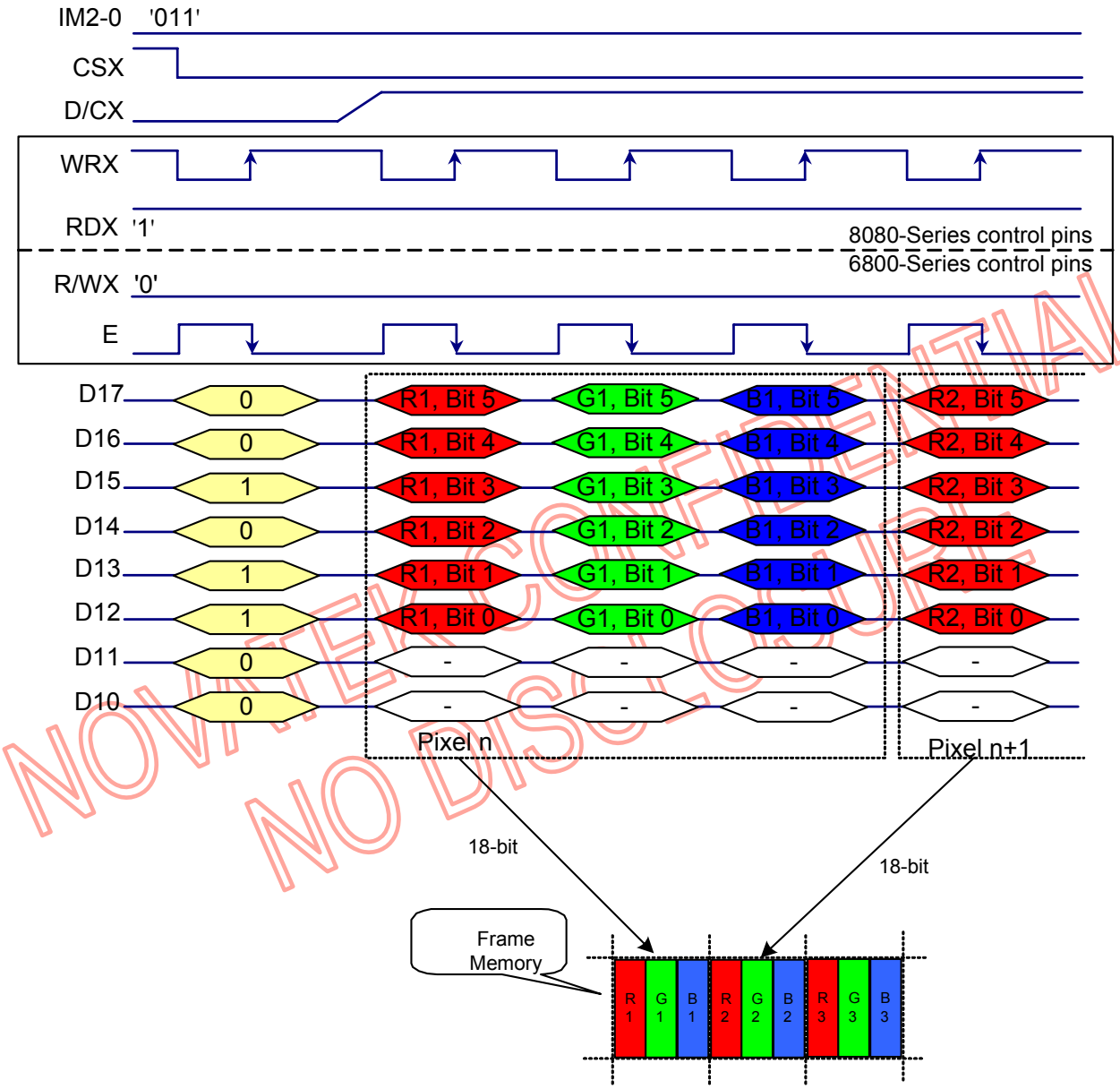
Note: '-' = Don't care - Can be set to '0' or '1'

Table 5.2.1.6.3 Write 8-bit data for RGB 5-6-5-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

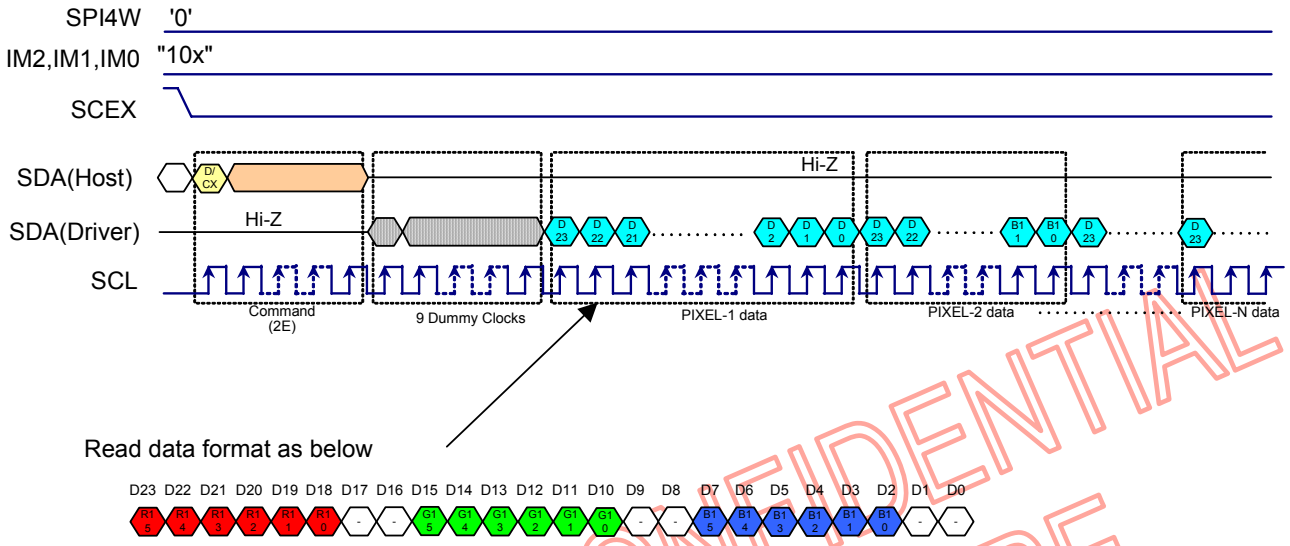
Table 5.2.1.6.4 Write 8-bit data for RGB 6-6-6-bits input



Note: '-' = Don't care - Can be set to '0' or '1'

5.2.1.7 3-PINS SERIAL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”10X”, 4WSPI = ‘0’)

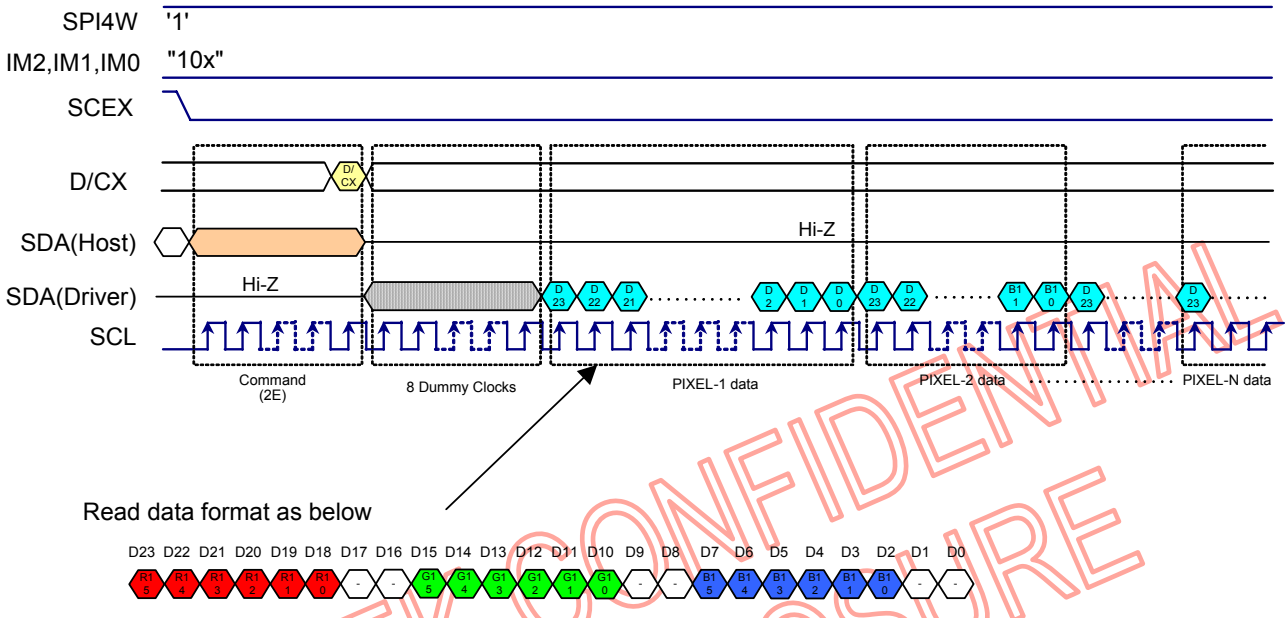
Table 5.2.1.7.1 READ data for RGB 6-6-6-bits output



Note : ‘-‘ = Don't care – Can be '0' or '1'

5.2.1.8 4-PINS SERIAL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”10X”, 4WSPI = ‘1’)

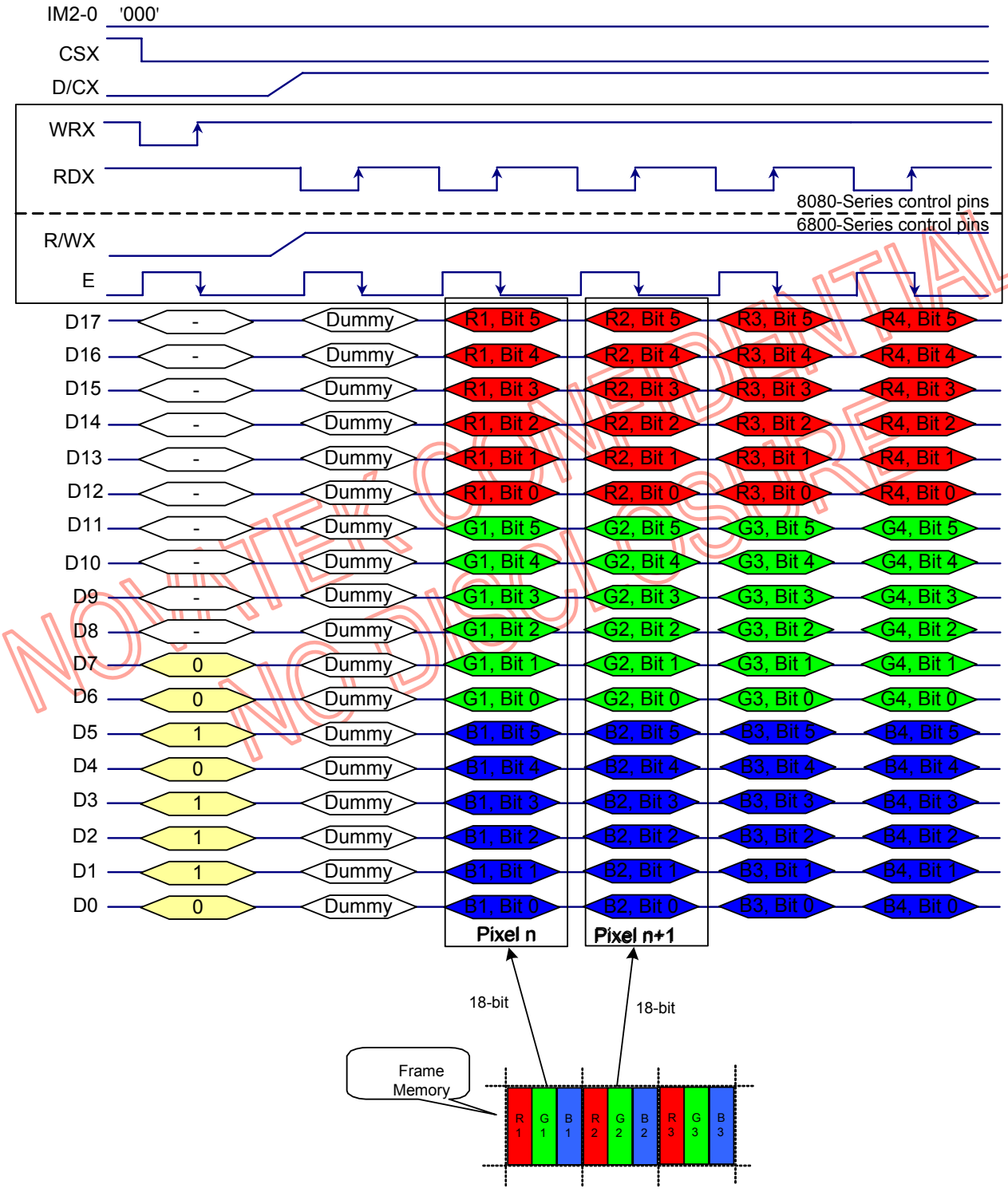
Table 5.2.1.8.1 READ data for RGB 6-6-6-bits output



Note : ‘-‘ = Don't care – Can be '0' or '1'

5.2.1.9 18-BIT PARALLEL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”000”)

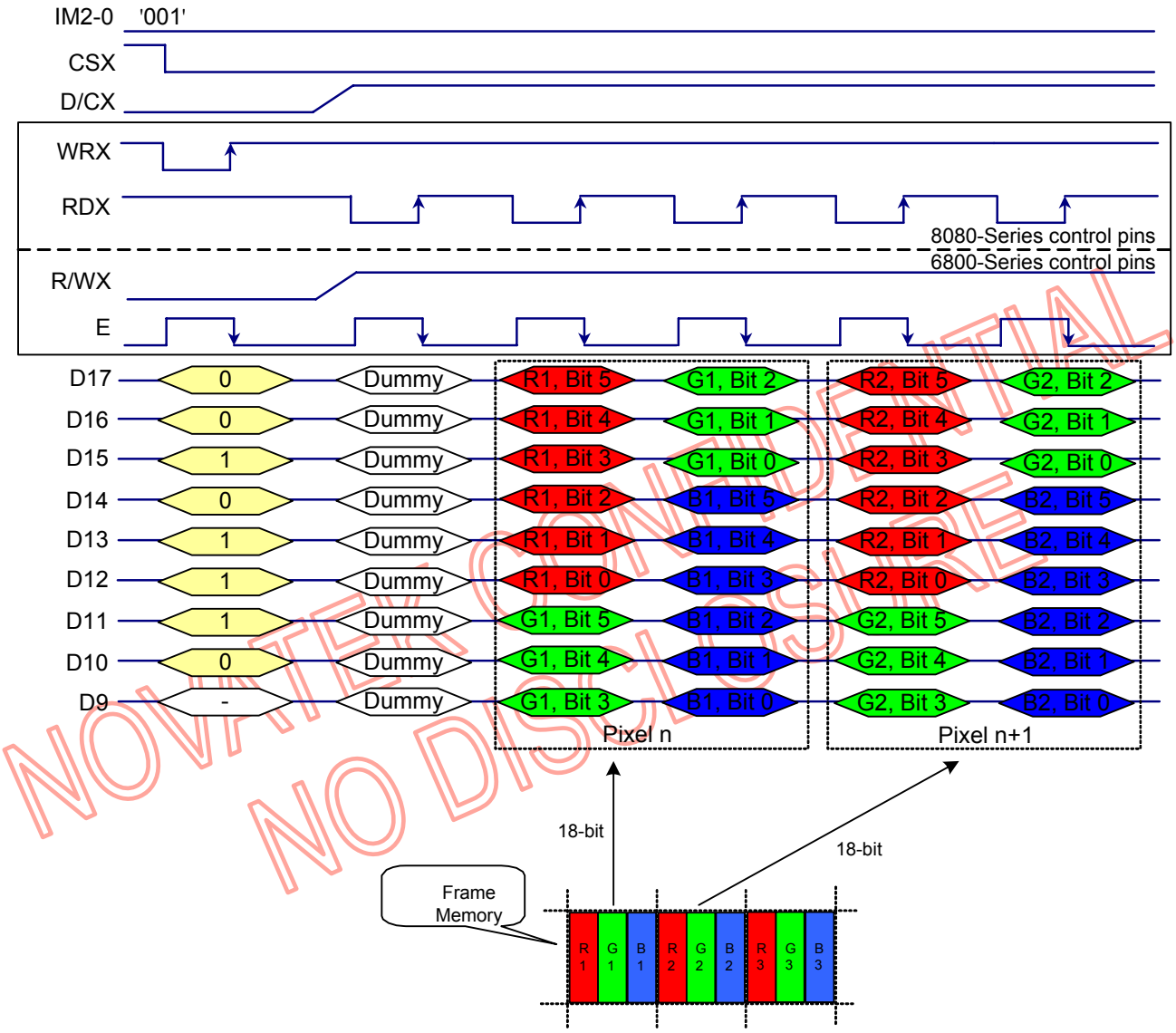
Table 5.2.1.9.1 READ data for RGB 6-6-6-bits output



Note : ‘-‘ = Don't care – Can be '0' or '1'

5.2.1.10 9-BIT PARALLEL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”001”)

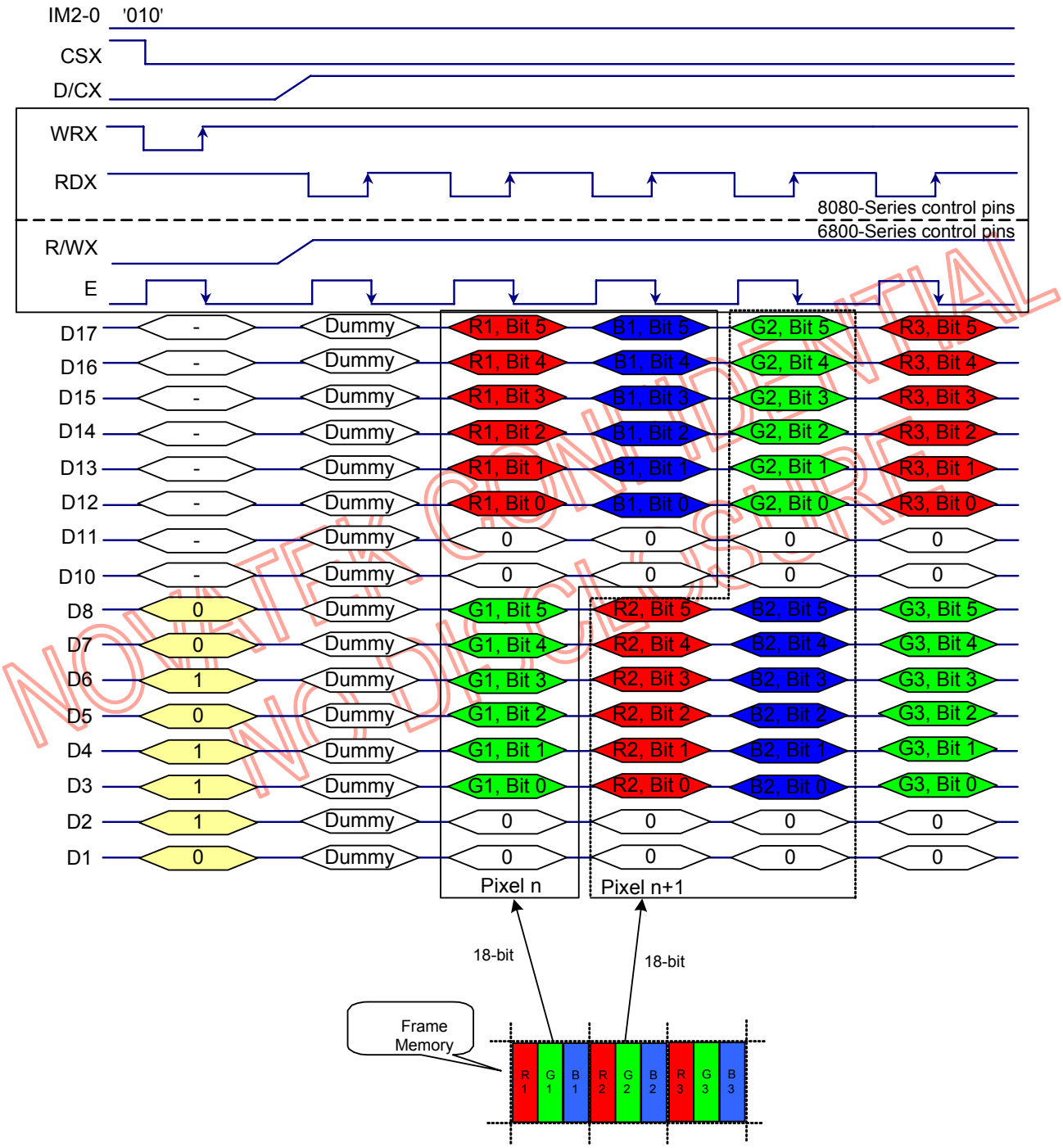
Table 5.2.1.10.1 READ data for RGB 6-6-6-bits output



Note : '-' = Don't care – Can be '0' or '1'

5.2.1.11 16-BIT PARALLEL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”010”)

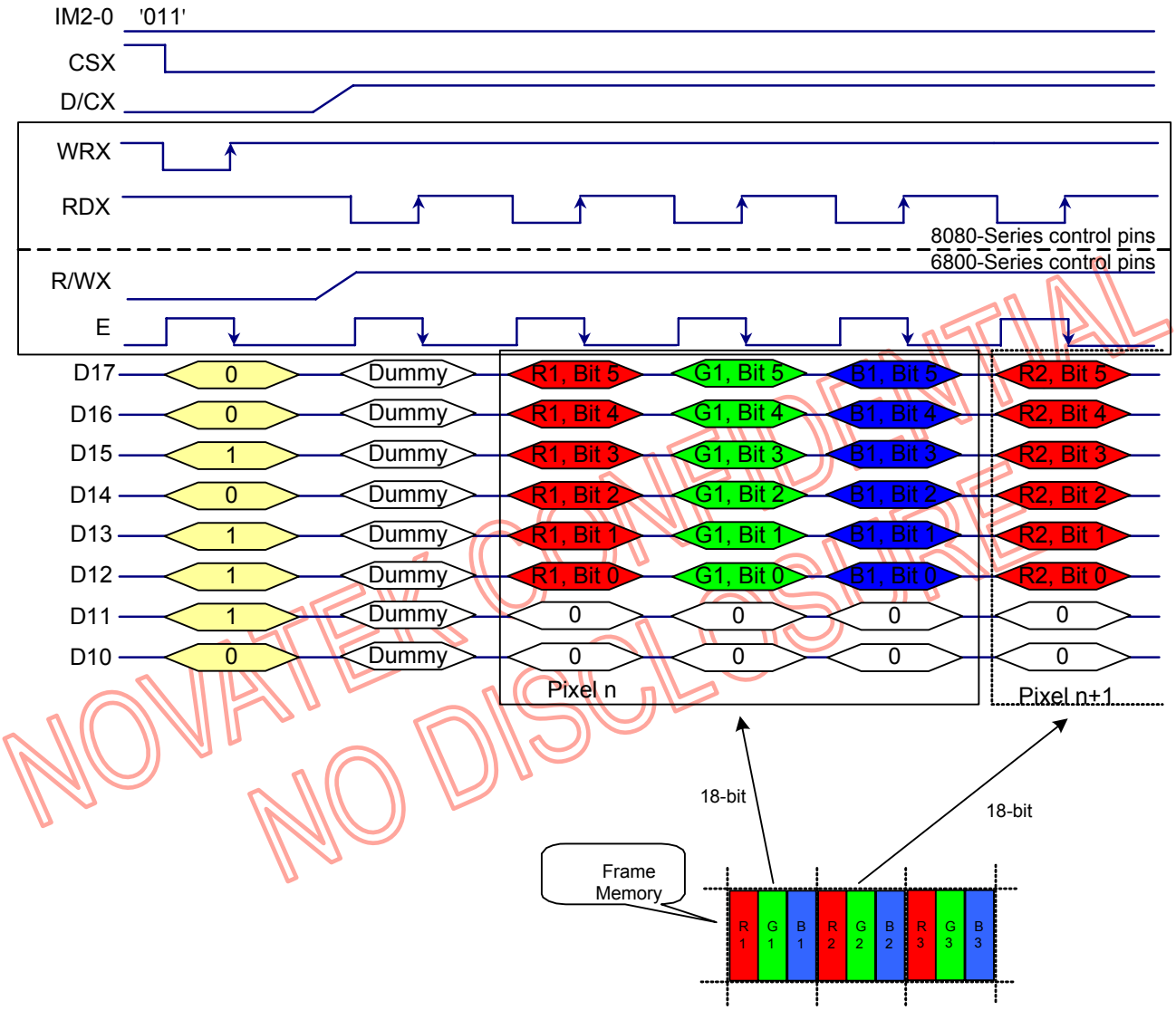
Table 5.2.1.11.1 READ data for RGB 6-6-6-bits output



Note : '-' = Don't care – Can be '0' or '1'

5.2.1.12 8-BIT PARALLEL INTERFACE FOR DATA RAM READ (IM2, IM1, IM0=”011”)

Table 5.2.1.12 READ data for RGB 8-8-8-bits output



Note : '-' = Don't care – Can be '0' or '1'

5.2.2 RGB Interface

For direct interface with both graphic controller and MPU, NT39125 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive (‘1’, high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= ’1’ and there is a rising edge of PCLK). D[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

5.2.2.1 RGB INTERFACE BUS WIDTH SET

All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command: VIPF[3:0]).

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
0101	R4	R3	R2	R1	R0		G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
1xxx	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	6-bit data
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

NOTE: Unused RGB data bus connected with IOVCC or GND.

5.2.2.2 RGB INTERFACE TIMING CHART

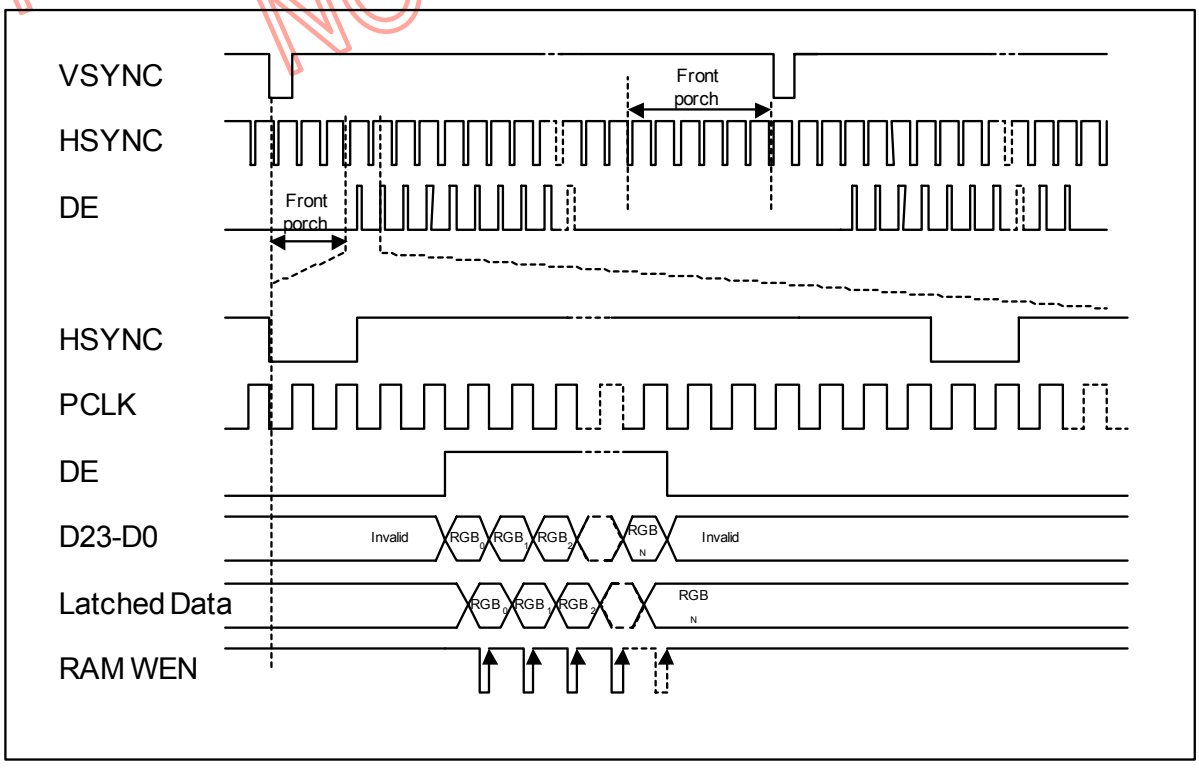


Fig. 5.2.1 Video signal data writing method in RGB Mode

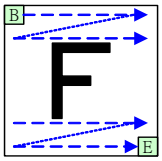
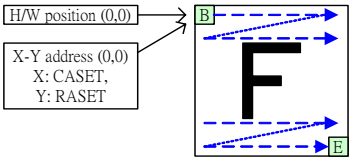
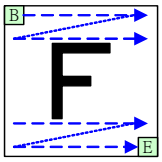
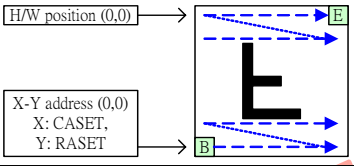
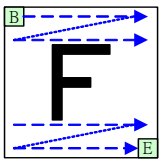
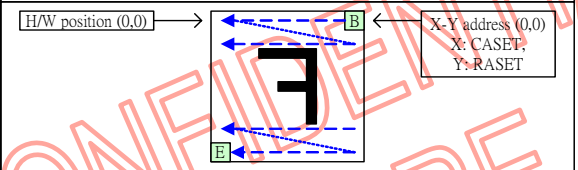
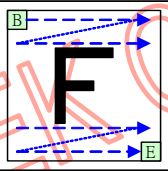
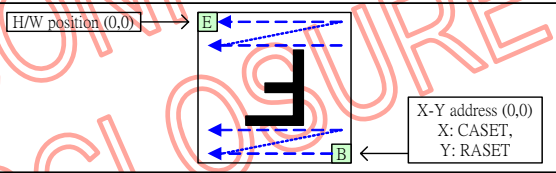
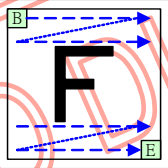
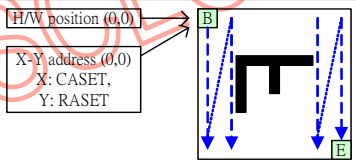
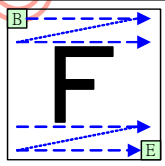
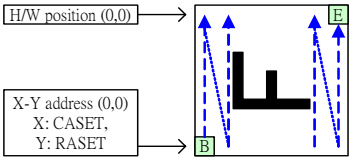
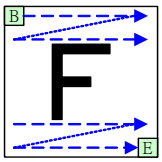
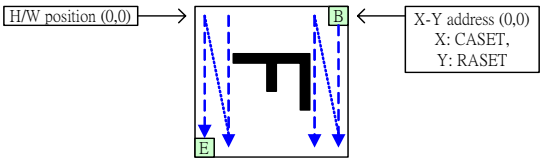
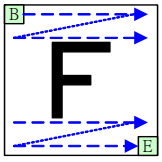
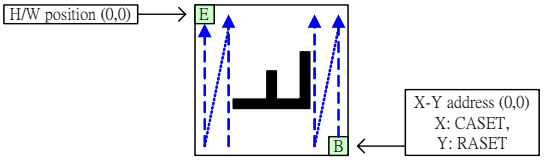
5.2.3 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The address pointers address the locations of RAM. The address ranges are X=0 to X=239 (EFh) and Y=0 to Y=431 (1AFh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address. For example, the whole display contents will be written, if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=239 (EFh), YE=431 (1AFh).
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).
For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.2 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

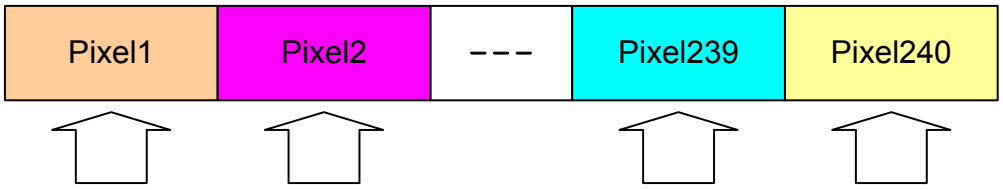
Fig. 5.2.2 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.2.4 Memory to Display Address Mapping

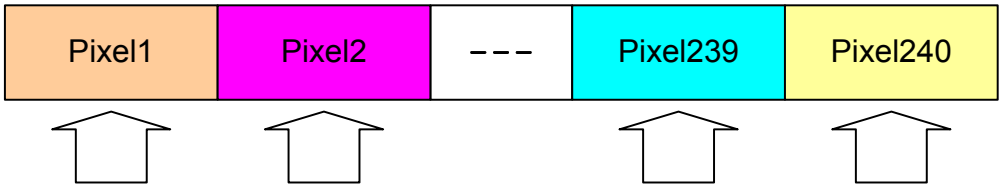
5.2.4.1 WHEN USING 240RGB X 432 RESOLUTION (GM1-0 = “00”)



RA																SA	
MY=0	*MY=1*	RGB=0 / RGB=1			RGB=0 / RGB=1			RGB Order	RGB=0 / RGB=1			RGB=0 / RGB=1				*ML=0*	*ML=1*
0	431	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	– – –	$R238_{5-0}$	$G238_{5-0}$	$B238_{5-0}$	$R239_{5-0}$	$G239_{5-0}$	$B239_{5-0}$		0	431
1	430							– – –								1	430
2	429							– – –								2	429
3	428							– – –								3	428
4	427							– – –								4	427
5	426							– – –								5	426
6	425							– – –								6	425
7	424							– – –								7	424
8	423							– – –								8	423
9	422							– – –								9	422
10	421							– – –								10	421
11	420							– – –								11	420
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮
424	7							– – –								424	7
425	6							– – –								425	6
426	5							– – –								426	5
427	4							– – –								427	4
428	3							– – –								428	3
429	2							– – –								429	2
430	1							– – –								430	1
431	0							– – –				RN_{5-0}	GN_{5-0}	BN_{5-0}		431	0
CA	*MX=0*	0			1			– – –	238			239					
	MX=1	239			238			– – –	1			0					

NOTE:
RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

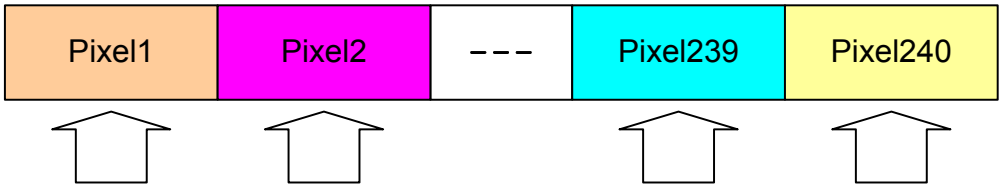
5.2.4.2 WHEN USING 240RGB X 400 RESOLUTION (GM1-0 = “01”)



RA															SA	
		RGB=0 / RGB=1			RGB=0 / RGB=1			RGB Order	RGB=0 / RGB=1			RGB=0 / RGB=1				
MY=0	*MY=1*														*ML=0*	*ML=1*
0	399	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	– – –	$R238_{5-0}$	$G238_{5-0}$	$B238_{5-0}$	$R239_{5-0}$	$G239_{5-0}$	$B239_{5-0}$	0	399
1	398							– – –							1	398
2	397							– – –							2	397
3	396							– – –							3	396
4	395							– – –							4	395
5	394							– – –							5	394
6	393							– – –							6	393
7	392							– – –							7	392
8	391							– – –							8	391
9	390							– – –							9	390
10	389							– – –							10	389
11	388							– – –							11	388
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
392	7							– – –							392	7
393	6							– – –							393	6
394	5							– – –							394	5
395	4							– – –							395	4
396	3							– – –							396	3
397	2							– – –							397	2
398	1							– – –							398	1
399	0							– – –				RN_{5-0}	GN_{5-0}	BN_{5-0}	399	0
CA	*MX=0*	0			1			– – –	238			239				
	MX=1	239			238			– – –	1			0				

NOTE:
RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2.4.3 WHEN USING 240RGB X 320 RESOLUTION (GM1-0 = “10”)



RA															SA	
		RGB=0 RGB=1			RGB=0 RGB=1			RGB Order	RGB=0 RGB=1			RGB=0 RGB=1				
MY=0	*MY=1*														*ML=0*	*ML=1*
0	319	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	– – –	$R238_{5-0}$	$G238_{5-0}$	$B238_{5-0}$	$R239_{5-0}$	$G239_{5-0}$	$B239_{5-0}$	0	319
1	318							– – –							1	318
2	317							– – –							2	317
3	316							– – –							3	316
4	315							– – –							4	315
5	314							– – –							5	314
6	313							– – –							6	313
7	312							– – –							7	312
8	311							– – –							8	311
9	310							– – –							9	310
10	309							– – –							10	309
11	308							– – –							11	308
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
312	7							– – –							312	7
313	6							– – –							313	6
314	5							– – –							314	5
315	4							– – –							315	4
316	3							– – –							316	3
317	2							– – –							317	2
318	1							– – –							318	1
319	0							– – –				RN_{5-0}	GN_{5-0}	BN_{5-0}	319	0
CA	*MX=0*	0			1			– – –	238			239				
	MX=1	239			238			– – –	1			0				

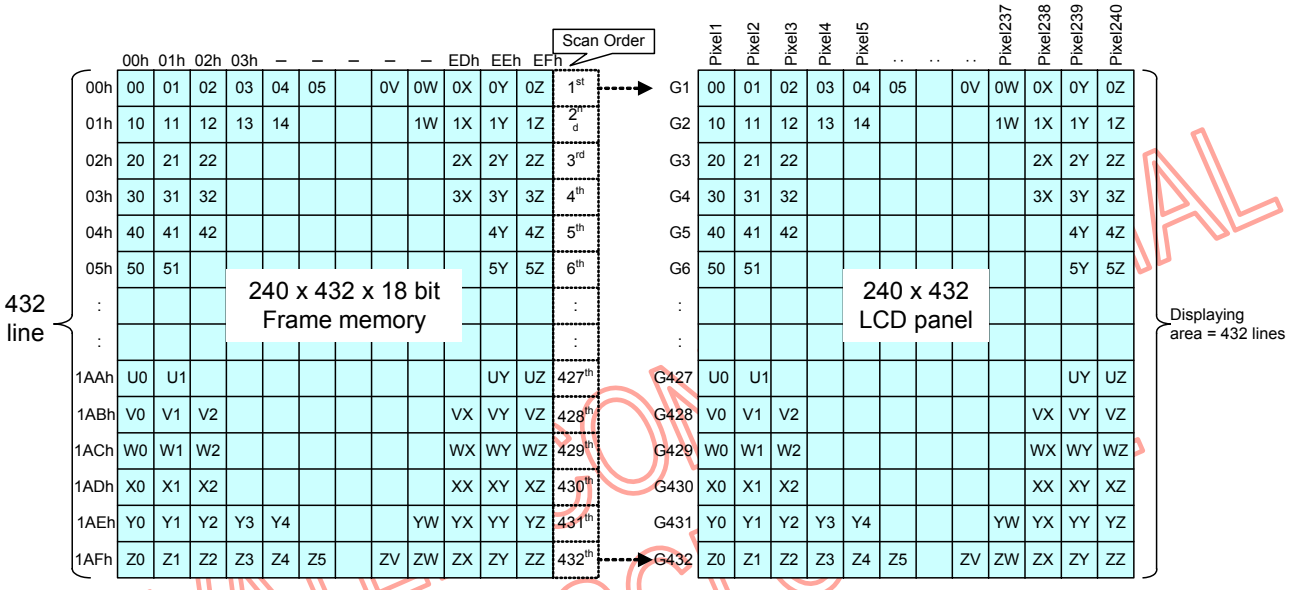
NOTE:
RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2.5 Normal Display On or Partial Mode On

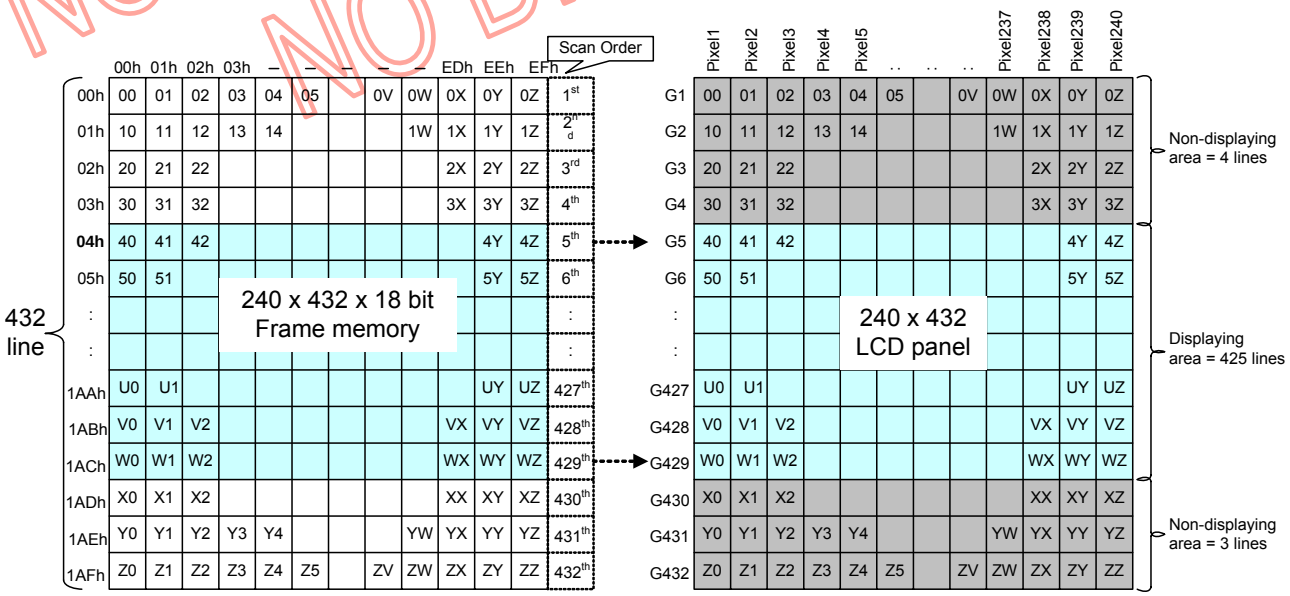
5.2.5.1 PARTIAL MODE

In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 000h to 1AFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

Example1) Normal Display On



Example2) Partial Display On（PSL [15:0] = 04h, PEL [15:0] = 1ACh）



5.2.6 Vertical Scroll

5.2.6.1 SCROLLING

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition”(33h) and “Vertical Scrolling Start Address” (37h).

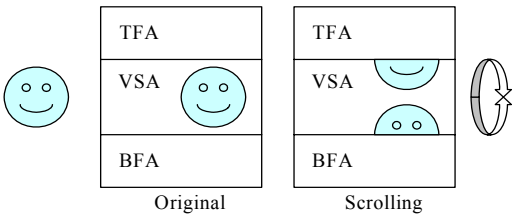
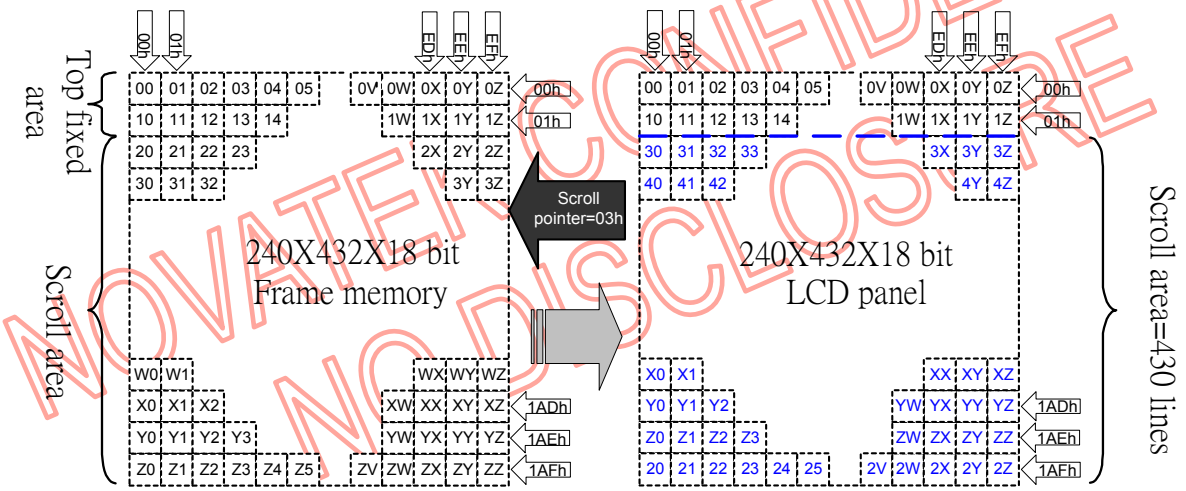


Fig. 5.2.6.1 Difference between Scrolling and original

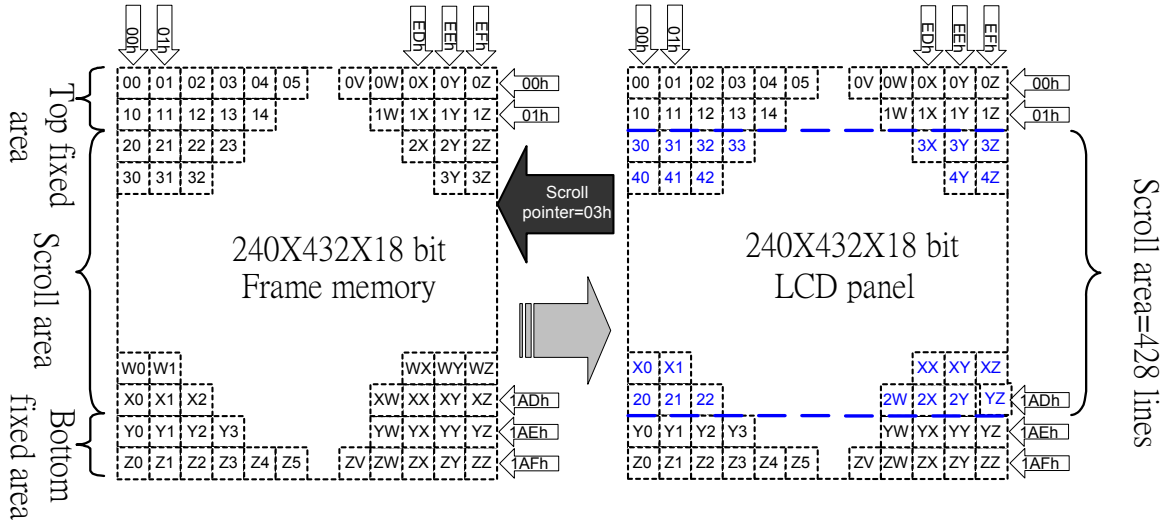
1). Example 1

TFA =2, VSA=430, BFA=0, when MADCTL Bit B4=0



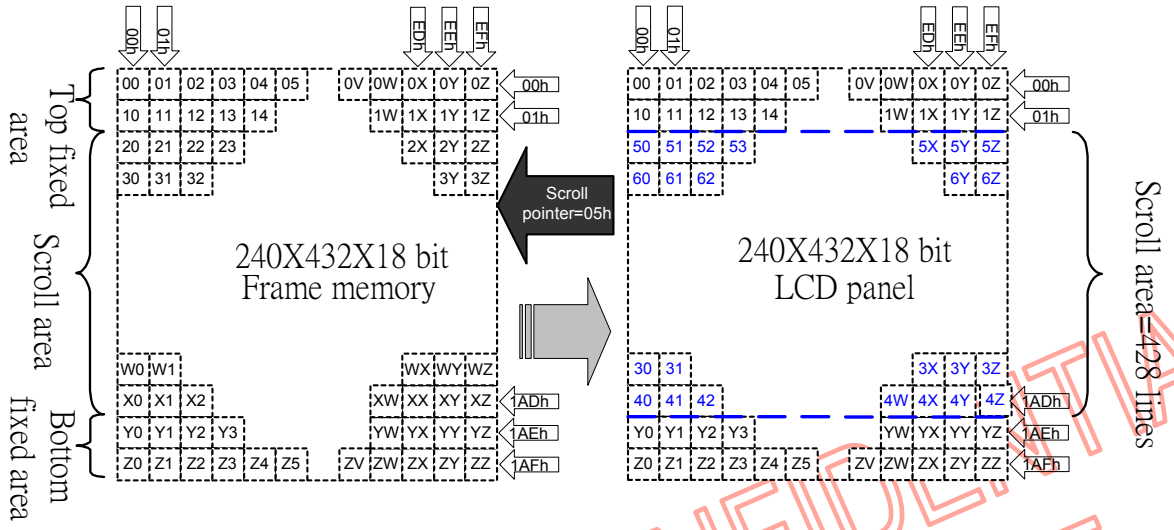
2). Example 2

TFA =2, VSA=428, BFA=2, when MADCTL Bit B4=0



3). Example 3

TFA =2, VSA=428, BFA=2, when MADCTL Bit B4=0



Note1 : For the 240xRGBx432 resolution (GM="00") and Vertical Scrolling Definition Parameter (TFA+VSA+BFA) ≠ 432,Scrolling Mode is undefined.

Note2 : For the 240xRGBx400 resolution (GM="01") and Vertical Scrolling Definition Parameter (TFA+VSA+BFA) ≠ 400,Scrolling Mode is undefined.

Note3 : For the 240xRGBx320 resolution (GM="10") and Vertical Scrolling Definition Parameter (TFA+VSA+BFA) ≠ 320,Scrolling Mode is undefined.

5.2.6.2 VERTICAL SCROLL EXAMPLE

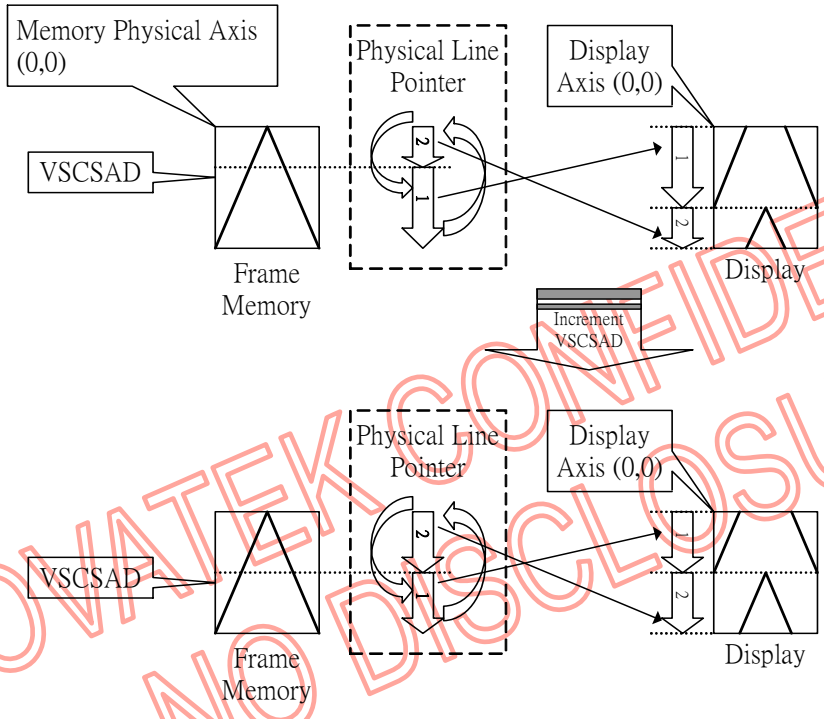
There are 2 cases of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA /= 430 (for 240xRGBx432 resolution)

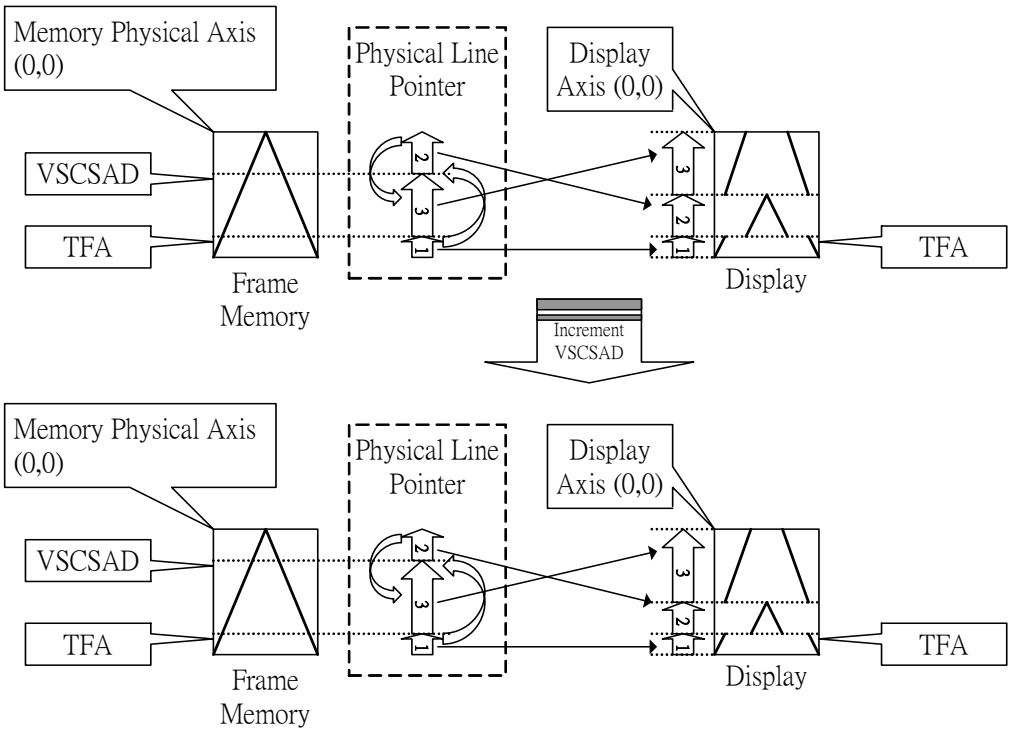
N/A. Do not set TFA + VSA + BFA /= 432. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=432 (for 240xRGBx432 resolution)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=432, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1", TFA=30, VSA=402, BFA=0 and VSCSAD=80.

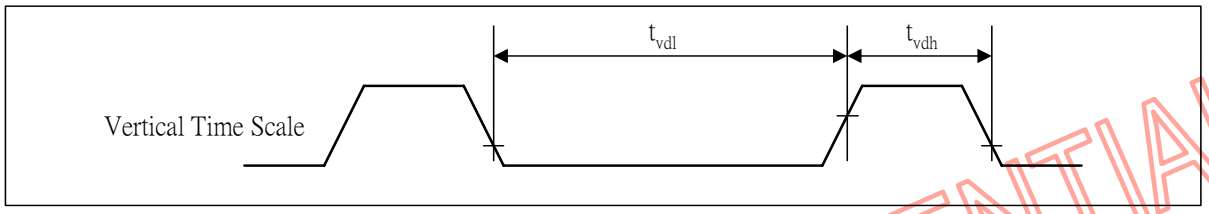


5.2.7 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

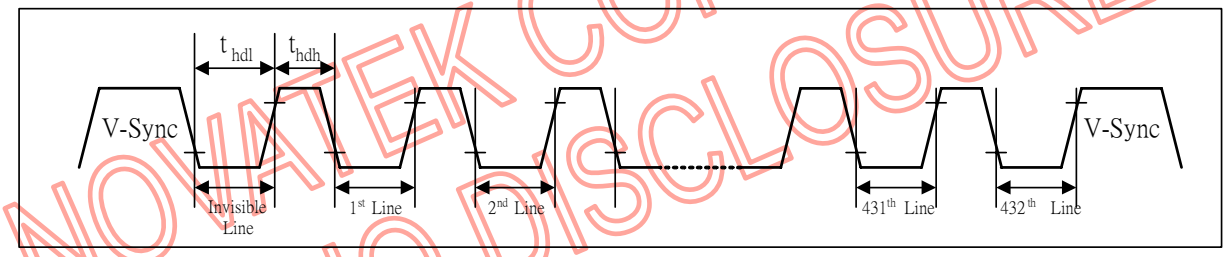
5.2.7.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

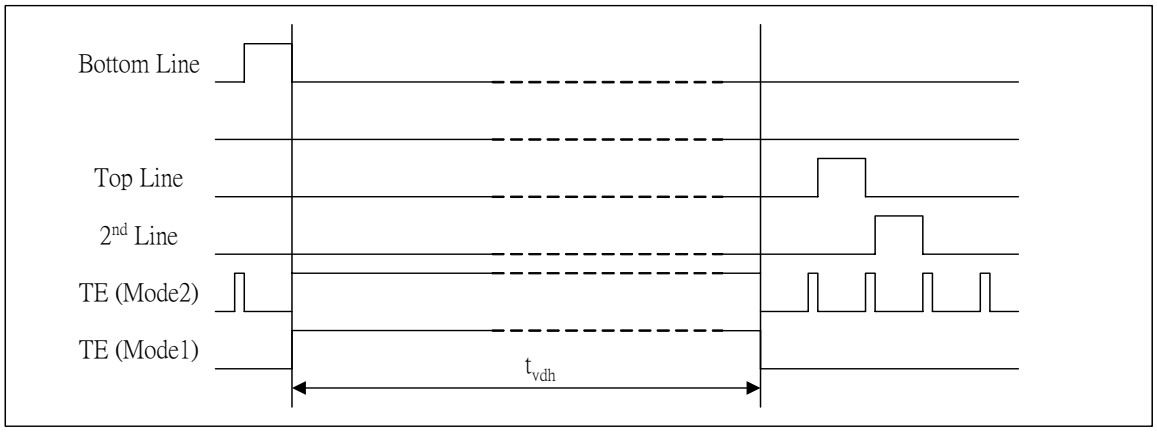


t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 432H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low

5.2.7.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:

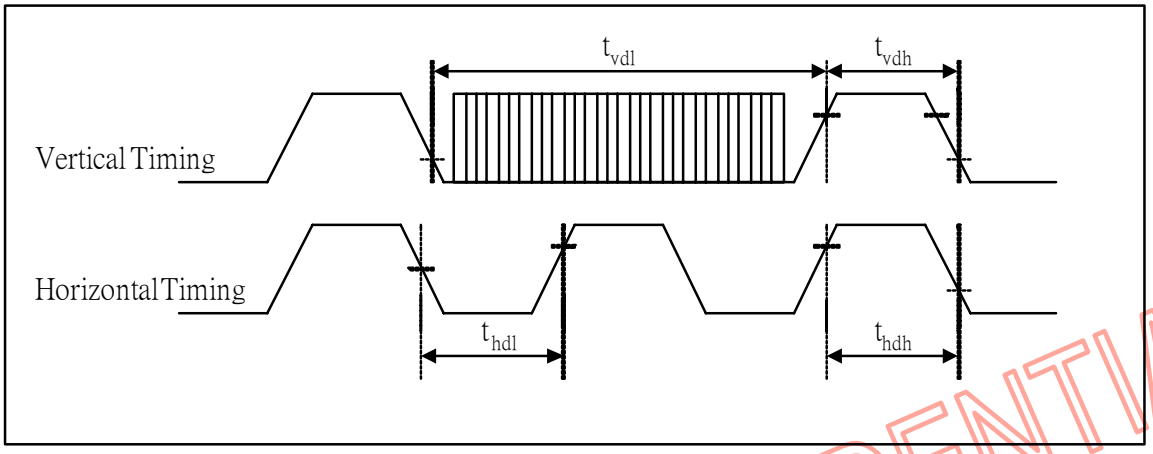


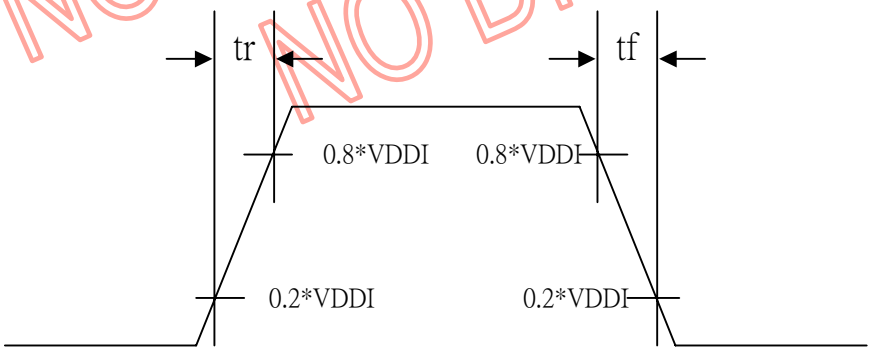
Table 5.2.17 AC characteristics of Tearing Effect Signal

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μs	
thdl	Horizontal Timing Low Duration	25	-	μs	
thdh	Horizontal Timing High Duration	18	370	μs	

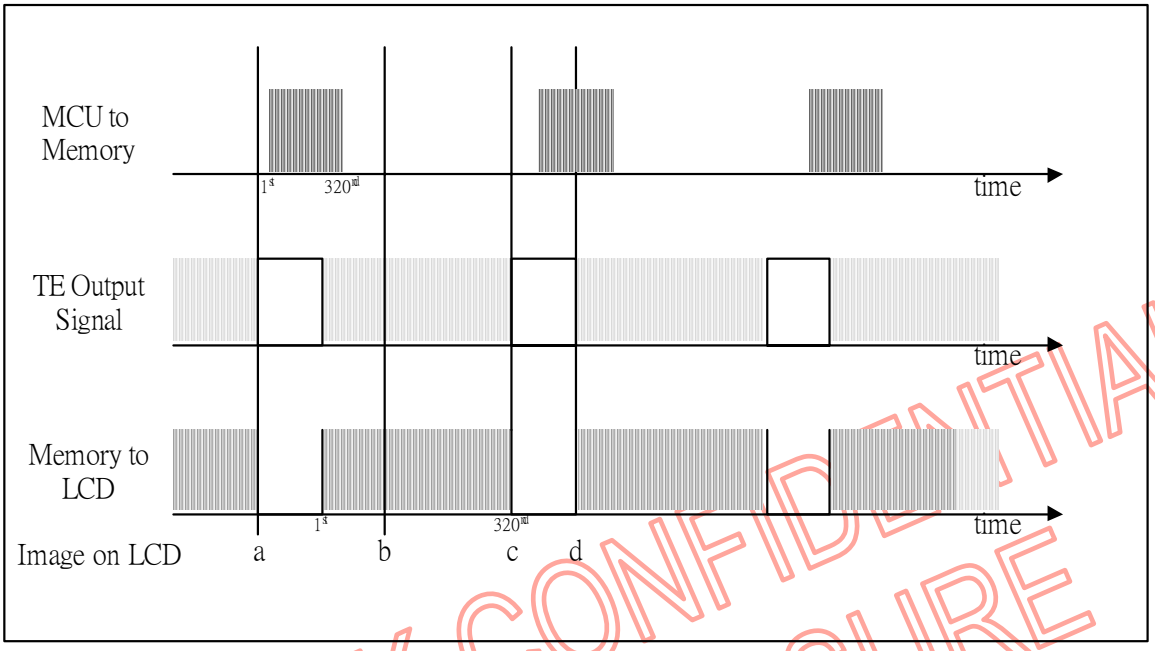
NOTE: The timings in Table 5.2.17 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

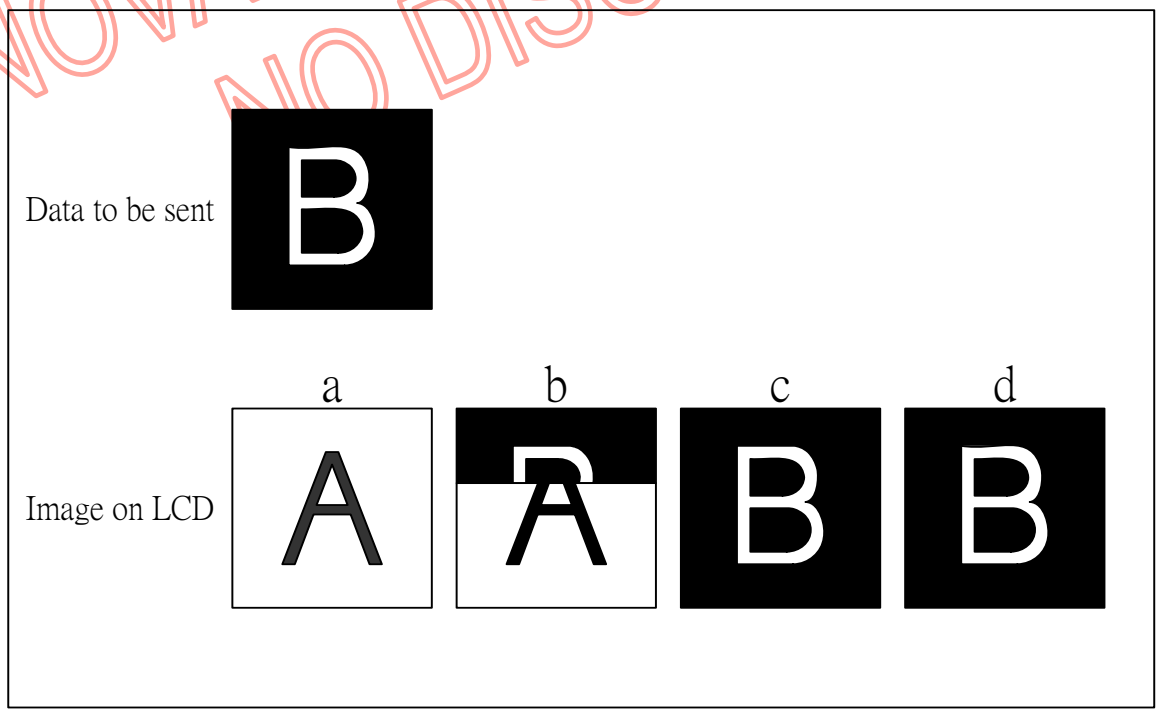
The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:



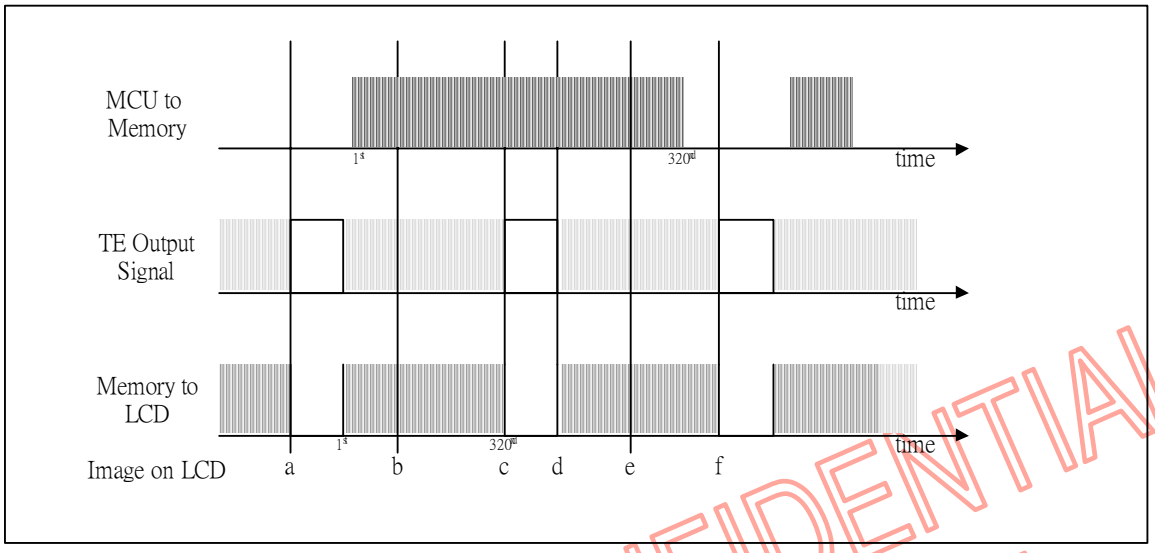
5.2.7.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.



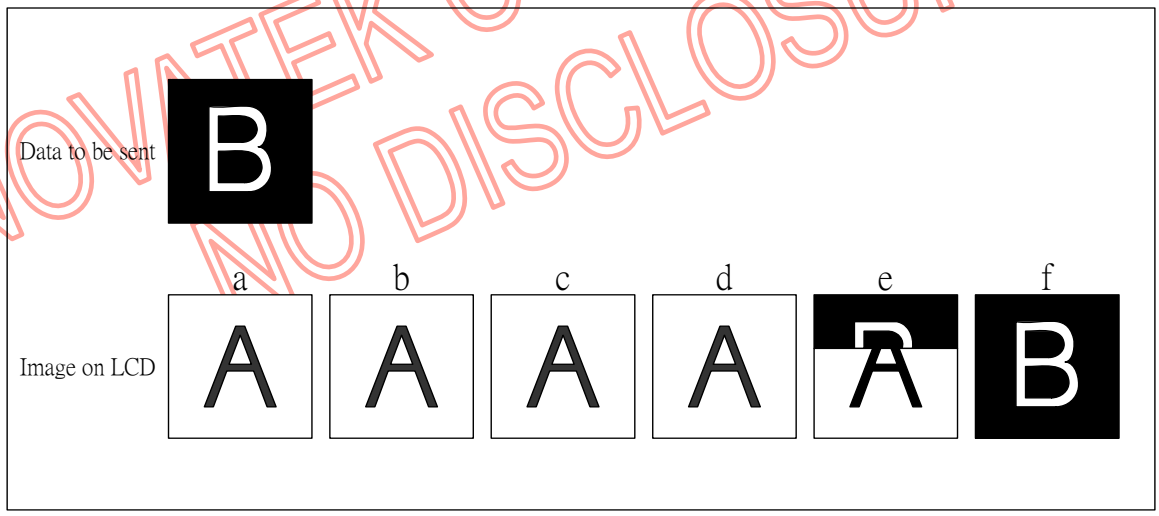
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.2.7.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



5.2.8 Color Depth Conversion Look Up Tables

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W reset (4k Color)	Default value after H/W reset (65k Color)	RGBSET parameter	Look Up Table Input Data	
					4k Color	65k Color
RED	$R_{005}R_{004}$ R_{003} R_{002} R_{001} R_{000}	000000	000000	1	0000	00000
	$R_{015}R_{014}$ R_{013} R_{012} R_{011} R_{010}	000100	000010	2	0001	00001
	$R_{025}R_{024}$ R_{023} R_{022} R_{021} R_{020}	001000	000100	3	0010	00010
	$R_{035}R_{034}$ R_{033} R_{032} R_{031} R_{030}	001100	000110	4	0011	00011
	$R_{045}R_{044}$ R_{043} R_{042} R_{041} R_{040}	010001	001000	5	0100	00100
	$R_{055}R_{054}$ R_{053} R_{052} R_{051} R_{050}	010101	001010	6	0101	00101
	$R_{065}R_{064}$ R_{063} R_{062} R_{061} R_{060}	011001	001100	7	0110	00110
	$R_{075}R_{074}$ R_{073} R_{072} R_{071} R_{070}	011101	001110	8	0111	00111
	$R_{085}R_{084}$ R_{083} R_{082} R_{081} R_{080}	100010	010000	9	1000	01000
	$R_{095}R_{094}$ R_{093} R_{092} R_{091} R_{090}	100110	010010	10	1001	01001
	$R_{105}R_{104}$ R_{103} R_{102} R_{101} R_{100}	101010	010100	11	1010	01010
	$R_{115}R_{114}$ R_{113} R_{112} R_{111} R_{110}	101110	010110	12	1011	01011
	$R_{125}R_{124}$ R_{123} R_{122} R_{121} R_{120}	110011	011000	13	1100	01100
	$R_{135}R_{134}$ R_{133} R_{132} R_{131} R_{130}	110111	011010	14	1101	01101
	$R_{145}R_{144}$ R_{143} R_{142} R_{141} R_{140}	111011	011100	15	1110	01110
	$R_{155}R_{154}$ R_{153} R_{152} R_{151} R_{150}	111111	011110	16	1111	01111
	$R_{165}R_{164}$ R_{163} R_{162} R_{161} R_{160}		100001	17	Not Used	10000
	$R_{175}R_{174}$ R_{173} R_{172} R_{171} R_{170}	-	100011	18		10001
	$R_{185}R_{184}$ R_{183} R_{182} R_{181} R_{180}	-	100101	19		10010
	$R_{195}R_{194}$ R_{193} R_{192} R_{191} R_{190}	-	100111	20		10011
	$R_{205}R_{204}$ R_{203} R_{202} R_{201} R_{200}	-	101001	21		10100
	$R_{215}R_{214}$ R_{213} R_{212} R_{211} R_{210}	-	101011	22		10101
	$R_{225}R_{224}$ R_{223} R_{222} R_{221} R_{220}	-	101101	23		10110
	$R_{235}R_{234}$ R_{233} R_{232} R_{231} R_{230}	-	101111	24		10111
	$R_{245}R_{244}$ R_{243} R_{242} R_{241} R_{240}	-	110001	25		11000
	$R_{255}R_{254}$ R_{253} R_{252} R_{251} R_{250}	-	110011	26		11001
	$R_{265}R_{264}$ R_{263} R_{262} R_{261} R_{260}	-	110101	27		11010
	$R_{275}R_{274}$ R_{273} R_{272} R_{271} R_{270}	-	110111	28		11011
	$R_{285}R_{284}$ R_{283} R_{282} R_{281} R_{280}	-	111001	29		11100
	$R_{295}R_{294}$ R_{293} R_{292} R_{291} R_{290}	-	111011	30		11101
	$R_{305}R_{304}$ R_{303} R_{302} R_{301} R_{300}	-	111101	31		11110
	$R_{315}R_{314}$ R_{313} R_{312} R_{311} R_{310}	-	111111	32		11111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W reset (4k Color)	Default value after H/W reset (65k Color)	RGBSET parameter	Look Up Table Input Data	
					4k Color	65k Color
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	000000	33	0000	000000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000100	000001	34	0001	000001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001000	000010	35	0010	000010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001100	000011	36	0011	000011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010001	000100	37	0100	000100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010101	000101	38	0101	000101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011001	000110	39	0110	000110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011101	000111	40	0111	000111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	100010	001000	41	1000	001000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	100110	001001	42	1001	001001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	101010	001010	43	1010	001010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	101110	001011	44	1011	001011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	110011	001100	45	1100	001100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	110111	001101	46	1101	001101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	111011	001110	47	1110	001110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	111111	001111	48	1111	001111
	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	-	010000	49	Not Used	010000
	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	-	010001	50		010001
	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	-	010010	51		010010
	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	-	010011	52		010011
	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	-	010100	53		010100
	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	-	010101	54		010101
	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	-	010110	55		010110
	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	-	010111	56		010111
	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	-	011000	57		011000
	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	-	011001	58		011001
	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	-	011010	59		011010
	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	-	011011	60		011011
	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	-	011100	61		011100
	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	-	011101	62		011101
	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	-	011110	63		011110
	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	-	011111	64		011111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W reset (4k Color)	Default value after H/W reset (65k Color)	RGBSET parameter	Look Up Table Input Data	
					4k Color	65k Color
GREEN	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	-	100000	65	Not Used	100000
	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	-	100001	66		100001
	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	-	100010	67		100010
	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	-	100011	68		100011
	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	-	100100	69		100100
	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	-	100101	70		100101
	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	-	100110	71		100110
	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	-	100111	72		100111
	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	-	101000	73		101000
	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	-	101001	74		101001
	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	-	101010	75		101010
	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	-	101011	76		101011
	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	-	101100	77		101100
	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	-	101101	78		101101
	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	-	101110	79		101110
	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	-	101111	80		101111
	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	-	110000	81		110000
	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	-	110001	82		110001
	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	-	110010	83		110010
	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	-	110011	84		110011
	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	-	110100	85		110100
	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	-	110101	86		110101
	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	-	110110	87		110110
	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	-	110111	88		110111
	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	-	111000	89		111000
	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	-	111001	90		111001
	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	-	111010	91		111010
	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	-	111011	92		111011
	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	-	111100	93		111100
	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	-	111101	94		111101
	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	-	111110	95		111110
	G_{635} G_{634} G_{533} G_{632} G_{631} G_{630}	-	111111	96		111111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W reset (4k Color)	Default value after H/W reset (65k Color)	RGBSET parameter	Look Up Table Input Data	
					4k Color	65k Color
BLUE	$B_{005}B_{004}$ B_{003} B_{002} B_{001} B_{000}	000000	000000	97	0000	00000
	$B_{015}B_{014}$ B_{013} B_{012} B_{011} B_{010}	000100	000010	98	0001	00001
	$B_{025}B_{024}$ B_{023} B_{022} B_{021} B_{020}	001000	000100	99	0010	00010
	$B_{035}B_{034}$ B_{033} B_{032} B_{031} B_{030}	001100	000110	100	0011	00011
	$B_{045}B_{044}$ B_{043} B_{042} B_{041} B_{040}	010001	001000	101	0100	00100
	$B_{055}B_{054}$ B_{053} B_{052} B_{051} B_{050}	010101	001010	102	0101	00101
	$B_{065}B_{064}$ B_{063} B_{062} B_{061} B_{060}	011001	001100	103	0110	00110
	$B_{075}B_{074}$ B_{073} B_{072} B_{071} B_{070}	011101	001110	104	0111	00111
	$B_{085}B_{084}$ B_{083} B_{082} B_{081} B_{080}	100010	010000	105	1000	01000
	$B_{095}B_{094}$ B_{093} B_{092} B_{091} B_{090}	100110	010010	106	1001	01001
	$B_{105}B_{104}$ B_{103} B_{102} B_{101} B_{100}	101010	010100	107	1010	01010
	$B_{115}B_{114}$ B_{113} B_{112} B_{111} B_{110}	101110	010110	108	1011	01011
	$B_{125}B_{124}$ B_{123} B_{122} B_{121} B_{120}	110011	011000	109	1100	01100
	$B_{135}B_{134}$ B_{133} B_{132} B_{131} B_{130}	110111	011010	110	1101	01101
	$B_{145}B_{144}$ B_{143} B_{142} B_{141} B_{140}	111011	011100	111	1110	01110
	$B_{155}B_{154}$ B_{153} B_{152} B_{151} B_{150}	111111	011110	112	1111	01111
	$B_{165}B_{164}$ B_{163} B_{162} B_{161} B_{160}	-	100001	113	Not Used	10000
	$B_{175}B_{174}$ B_{173} B_{172} B_{171} B_{170}	-	100011	114		10001
	$B_{185}B_{184}$ B_{183} B_{182} B_{181} B_{180}	-	100101	115		10010
	$B_{195}B_{194}$ B_{193} B_{192} B_{191} B_{190}	-	100111	116		10011
	$B_{205}B_{204}$ B_{203} B_{202} B_{201} B_{200}	-	101001	117		10100
	$B_{215}B_{214}$ B_{213} B_{212} B_{211} B_{210}	-	101011	118		10101
	$B_{225}B_{224}$ B_{223} B_{222} B_{221} B_{220}	-	101101	119		10110
	$B_{235}B_{234}$ B_{233} B_{232} B_{231} B_{230}	-	101111	120		10111
	$B_{245}B_{244}$ B_{243} B_{242} B_{241} B_{240}	-	110001	121		11000
	$B_{255}B_{254}$ B_{253} B_{252} B_{251} B_{250}	-	110011	122		11001
	$B_{265}B_{264}$ B_{263} B_{262} B_{261} B_{260}	-	110101	123		11010
	$B_{275}B_{274}$ B_{273} B_{272} B_{271} B_{270}	-	110111	124		11011
	$B_{285}B_{284}$ B_{283} B_{282} B_{281} B_{280}	-	111001	125		11100
	$B_{295}B_{294}$ B_{293} B_{292} B_{291} B_{290}	-	111011	126		11101
	$B_{305}B_{304}$ B_{303} B_{302} B_{301} B_{300}	-	111101	127		11110
	$B_{315}B_{314}$ B_{313} B_{312} B_{311} B_{310}	-	111111	128		11111

Note1: After Power-On or HW-Reset, the values of LUT (Look Up Table) could be changed by the command “RGBSET(R2Dh)”, otherwise, the default values follow the setting of “COLMODE(R3Ah)”.

Note2: The SW-Reset do not change the values of LUT.

5.3 INSTRUCTION DECODER & REGISTER

The instruction decoder identifies command words arriving at the interface and routes the following data type bytes to their destination. The command set can be found in “6 INSTRUCTION DESCRIPTION” section.

5.4 SYSTEM CLOCK GENERATOR

The timing generator produces the various signals to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.5 OSCILLATOR

NT39125 has on-chip oscillator which does not require external components. This oscillator output signal is used for system clock generation for internal display operation

5.6 SOURCE DRIVER

The source driver block includes 240x3 source outputs (S1 to S720), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simultaneous selected rows. When less then 720 sources are required the unused source outputs should be left open-circuit.

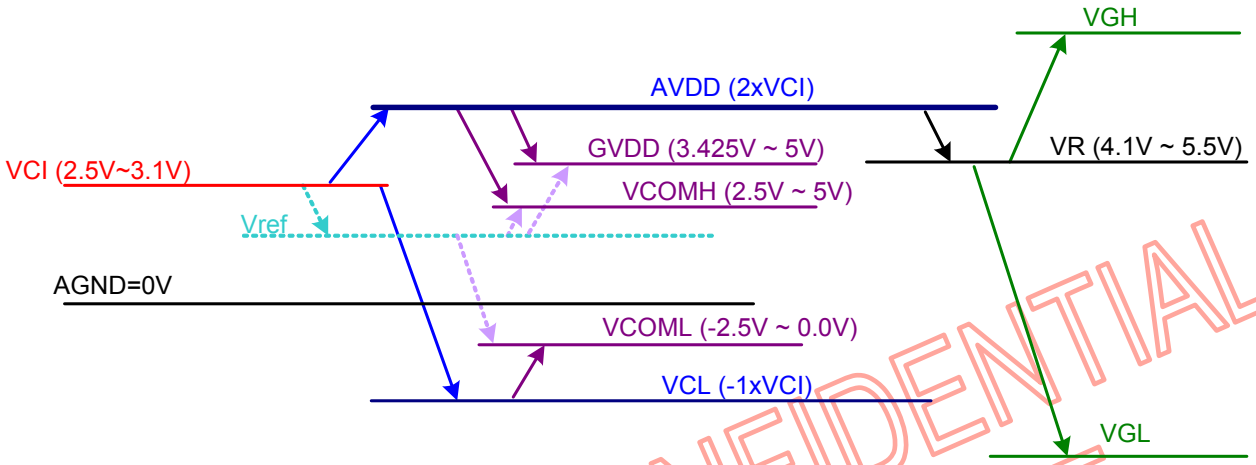
5.7 GATE DRIVER

The gate driver block includes 320 gate outputs (G1 to G432) which should be connected directly to the TFT-LCD.

5.8 LCD POWER GENERATION CIRCUIT

5.8.1 LCD Power Generation Scheme

The boost voltage generated in NT39125 is shown as below. (In case of default value)



Remark

1. AVDD supply to all power source (exclude VGH, VGL)

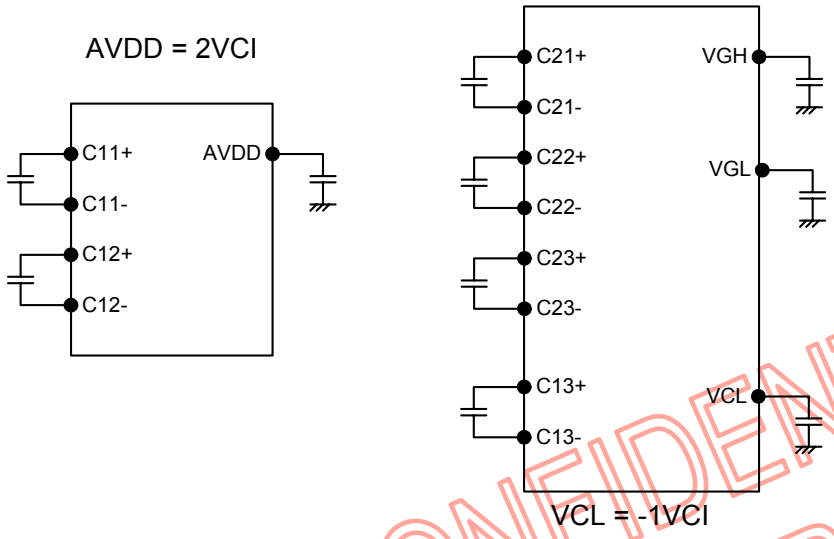
2. Source output range: 0.1V ~ GVDD-0.1V

3. Linear Range: 0.2V ~ GVDD-0.2V (For all output voltage, but exclude VGH, VGL)

4. Above operating voltages is min range.

5.8.2 Various Boosting Steps

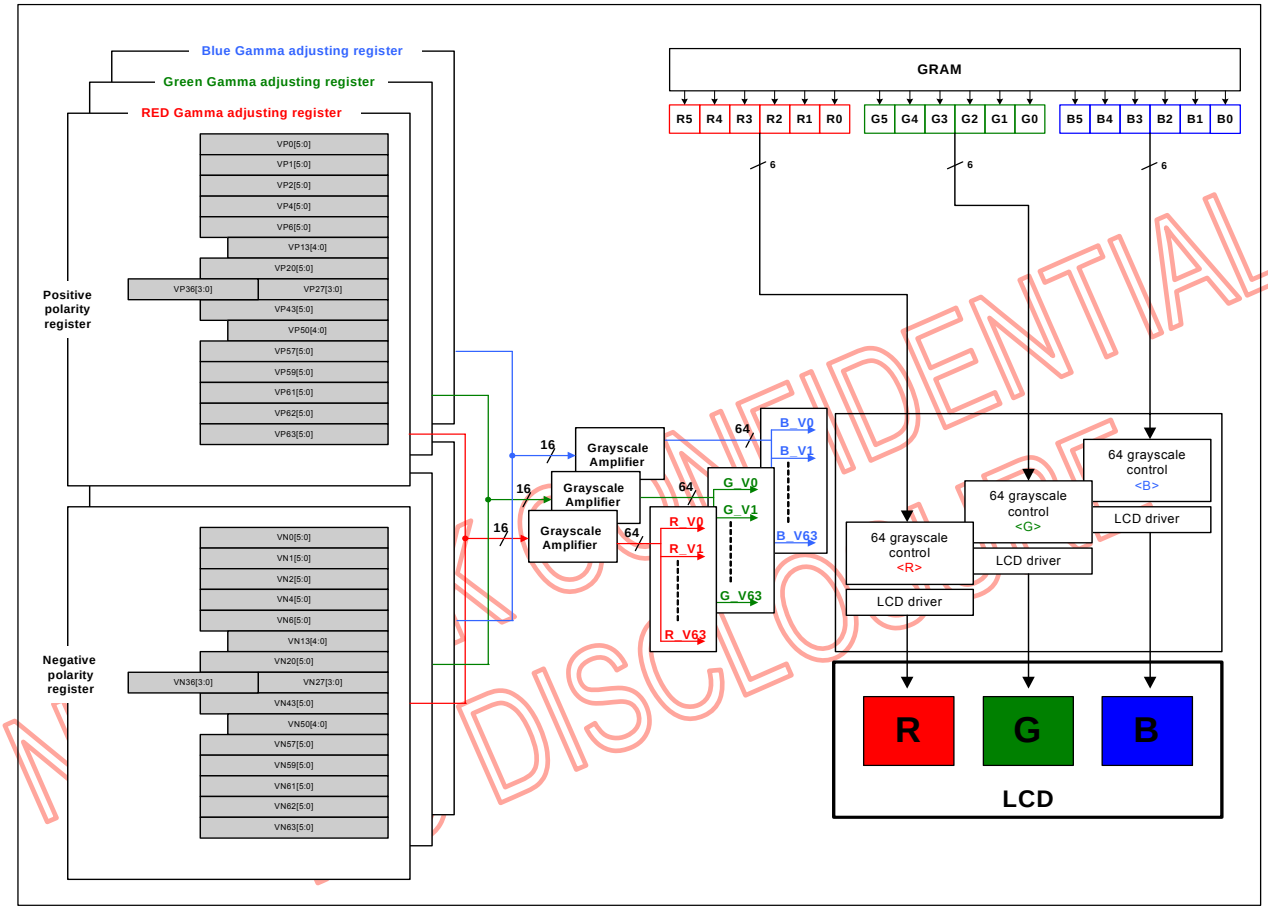
The boost steps of each boosting voltage are selected by BT[2:0]. Different booster applications are shown as below :



BT[2:0]		AVDD	VCL	VGH	VGL
000	0	VCI x 2	- VCI x 1	VR x 3	- VR x 2 – VCI
001	1				- VR x 2
010	2				- VR – VCI
011	3			VR x 2 + VCI	- VR x 2 – VCI
100	4				- VR x 2
101	5				- VR – VCI
110	6			VR x 2	- VR x 2
111	7				- VR – VCI

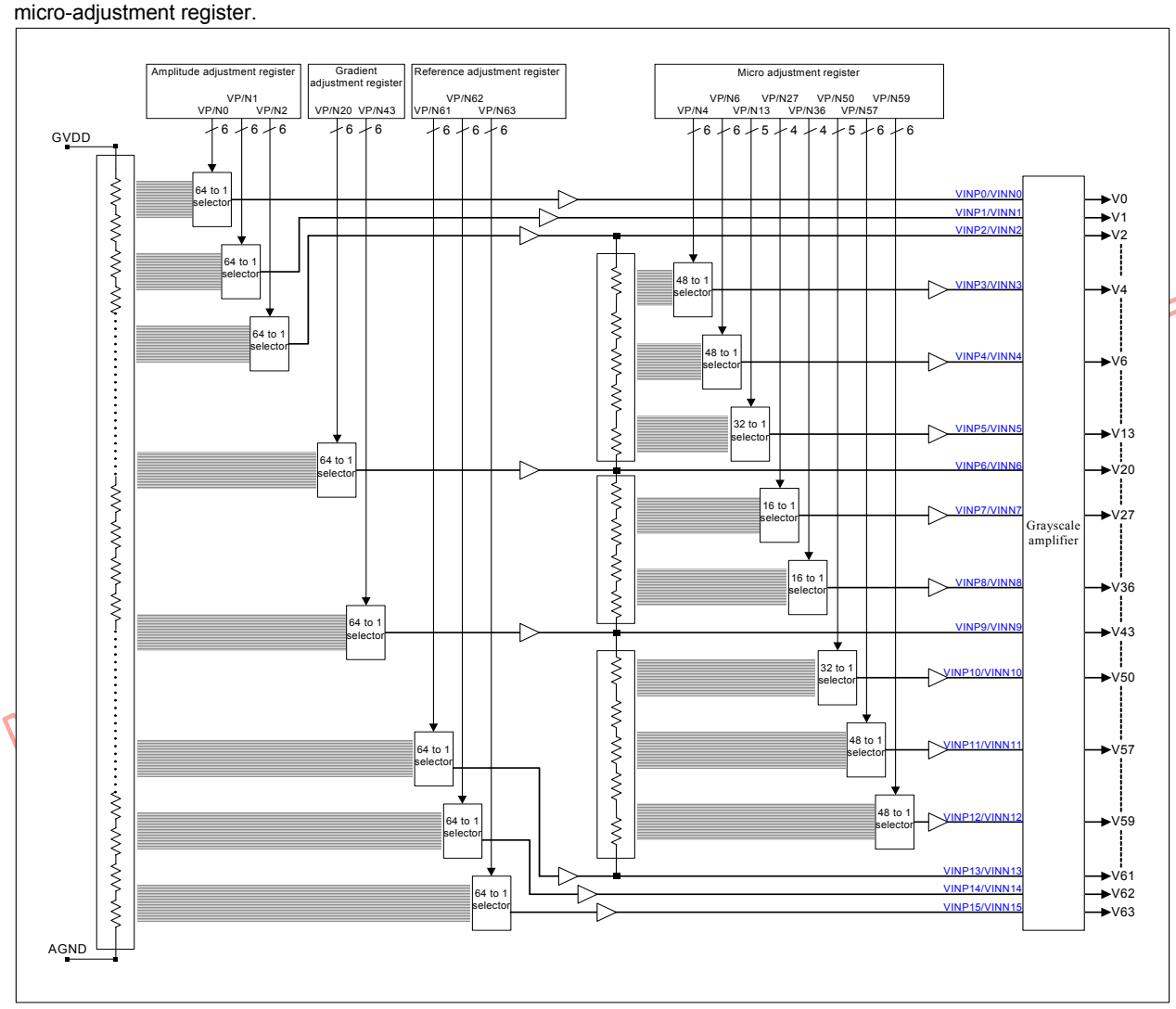
5.9 GAMMA CORRECTION FUNCTION

The NT39125 supports gamma-correction function to display in 262,144 colors simultaneously by determining 16 grayscale levels using gamma correction registers consisting of gradient-adjustment, amplitude-adjustment and fine-adjustment registers. The NT39125 separate the gamma registers for positive and negative polarities to allow settings for respective polarities according to the characteristics of liquid crystal panel.



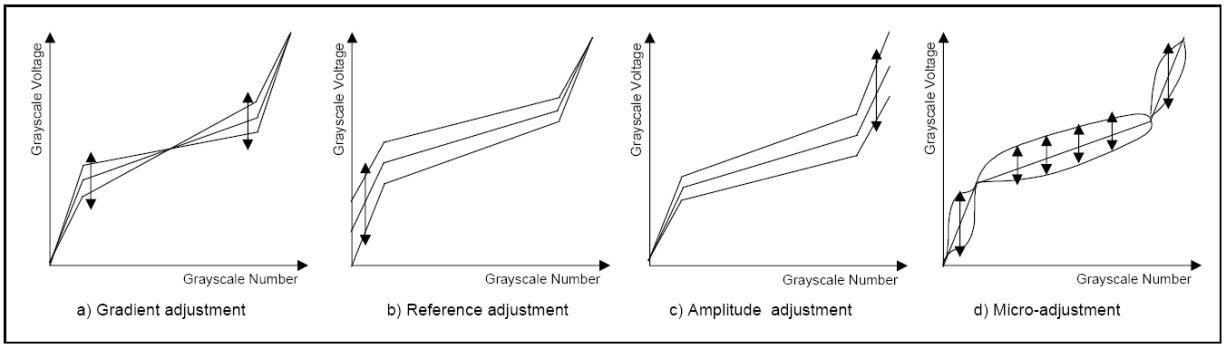
5.9.1 STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. The 16 voltage levels (VIN0-VIN15) between GVDD and AGND are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



5.9.2 GAMMA ADJUSTMENT REGISTER

This block has registers to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. The following figure indicates the operation of each adjustment register.



Gradient adjusting register

The gradient adjustment register is to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the VINP6/VINN6 and VINP9/VINN9 voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and AGND. Also, there is an independent register on the positive/negative polarities in order for corresponding to asymmetry drive.

Reference adjusting register

The Reference adjustment register is to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP13/VIN13, VINP14/VINN14 and VINP15/VINN15 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and AGND.

Amplitude adjusting register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VIN0, VINP1/VINN1 and VINP2/VINN2 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and AGND.

Micro-adjusting register

The Micro adjustment register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 16 to 1 selector, 32 to 1 selector or 48 to 1 selector towards the reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

Register	Postive polarity	Negative polarity	Set-up content
Gradient adjustment	VP20[5:0]	VN20[5:0]	The voltage of VINP6/VINN6 is select by the 64 to 1 select
	VP43[5:0]	VN43[5:0]	The voltage of VINP9/VINN9 is select by the 64 to 1 select
Amplitude adjustment	VP0[5:0]	VN0[5:0]	The voltage of VINP0/VINN0 is select by the 64 to 1 select
	VP1[5:0]	VN1[5:0]	The voltage of VINP1/VINN1 is select by the 64 to 1 select
	VP2[5:0]	VN2[5:0]	The voltage of VINP2/VINN2 is select by the 64 to 1 select
Reference adjustment	VP61[5:0]	VN61[5:0]	The voltage of VINP13/VINN13 is select by the 64 to 1 select
	VP62[5:0]	VN62[5:0]	The voltage of VINP14/VINN14 is select by the 64 to 1 select
	VP63[5:0]	VN63[5:0]	The voltage of VINP15/VINN15 is select by the 64 to 1 select
Micro adjustment	VP4[5:0]	VN4[5:0]	The voltage of VINP3/VINN3 is select by the 48 to 1 select
	VP6[5:0]	VN6[5:0]	The voltage of VINP4/VINN4 is select by the 48 to 1 select
	VP13[4:0]	VN13[4:0]	The voltage of VINP5/VINN5 is select by the 32 to 1 select
	VP27[3:0]	VN27[3:0]	The voltage of VINP7/VINN7 is select by the 16 to 1 select
	VP36[3:0]	VN36[3:0]	The voltage of VINP8/VINN8 is select by the 16 to 1 select
	VP50[4:0]	VN50[4:0]	The voltage of VINP10/VINN10 is select by the 32 to 1 select
	VP57[5:0]	VN57[5:0]	The voltage of VINP11/VINN11 is select by the 48 to 1 select
	VP59[5:0]	VN59[5:0]	The voltage of VINP12/VINN12 is select by the 48 to 1 select

Gamma adjusting voltage formula

Table1. Amplitude Adjustment (1)

VP(N)0[5:0]	Formula of VINP(N)0	VRP(N)0[5:0]	Formula of VINP(N)0
000000	GVDD –ΔV x (0R/130R)	100000	GVDD –ΔV x (32R/130R)
000001	GVDD –ΔV x (1R/130R)	100001	GVDD –ΔV x (33R/130R)
000010	GVDD –ΔV x (2R/130R)	100010	GVDD –ΔV x (34R/130R)
000011	GVDD –ΔV x (3R/130R)	100011	GVDD –ΔV x (35R/130R)
000100	GVDD –ΔV x (4R/130R)	100100	GVDD –ΔV x (36R/130R)
000101	GVDD –ΔV x (5R/130R)	100101	GVDD –ΔV x (37R/130R)
000110	GVDD –ΔV x (6R/130R)	100110	GVDD –ΔV x (38R/130R)
000111	GVDD –ΔV x (7R/130R)	100111	GVDD –ΔV x (39R/130R)
001000	GVDD –ΔV x (8R/130R)	101000	GVDD –ΔV x (40R/130R)
001001	GVDD –ΔV x (9R/130R)	101001	GVDD –ΔV x (41R/130R)
001010	GVDD –ΔV x (10R/130R)	101010	GVDD –ΔV x (42R/130R)
001011	GVDD –ΔV x (11R/130R)	101011	GVDD –ΔV x (43R/130R)
001100	GVDD –ΔV x (12R/130R)	101100	GVDD –ΔV x (44R/130R)
001101	GVDD –ΔV x (13R/130R)	101101	GVDD –ΔV x (45R/130R)
001110	GVDD –ΔV x (14R/130R)	101110	GVDD –ΔV x (46R/130R)
001111	GVDD –ΔV x (15R/130R)	101111	GVDD –ΔV x (47R/130R)
010000	GVDD –ΔV x (16R/130R)	110000	GVDD –ΔV x (48R/130R)
010001	GVDD –ΔV x (17R/130R)	110001	GVDD –ΔV x (49R/130R)
010010	GVDD –ΔV x (18R/130R)	110010	GVDD –ΔV x (50R/130R)
010011	GVDD –ΔV x (19R/130R)	110011	GVDD –ΔV x (51R/130R)
010100	GVDD –ΔV x (20R/130R)	110100	GVDD –ΔV x (52R/130R)
010101	GVDD –ΔV x (21R/130R)	110101	GVDD –ΔV x (53R/130R)
010110	GVDD –ΔV x (22R/130R)	110110	GVDD –ΔV x (54R/130R)
010111	GVDD –ΔV x (23R/130R)	110111	GVDD –ΔV x (55R/130R)
011000	GVDD –ΔV x (24R/130R)	111000	GVDD –ΔV x (56R/130R)
011001	GVDD –ΔV x (25R/130R)	111001	GVDD –ΔV x (57R/130R)
011010	GVDD –ΔV x (26R/130R)	111010	GVDD –ΔV x (58R/130R)
011011	GVDD –ΔV x (27R/130R)	111011	GVDD –ΔV x (59R/130R)
011100	GVDD –ΔV x (28R/130R)	111100	GVDD –ΔV x (60R/130R)
011101	GVDD –ΔV x (29R/130R)	111101	GVDD –ΔV x (61R/130R)
011110	GVDD –ΔV x (30R/130R)	111110	GVDD –ΔV x (62R/130R)
011111	GVDD –ΔV x (31R/130R)	111111	GVDD –ΔV x (63R/130R)

ΔV: Potential difference between GVDD and AGND

Table2. Amplitude Adjustment (2)

VP(N)1[5:0]	Formula of VINP(N)1	VRP(N)1[5:0]	Formula of VINP(N)1
000000	GVDD –ΔV x (0R/130R)	100000	GVDD –ΔV x (32R/130R)
000001	GVDD –ΔV x (1R/130R)	100001	GVDD –ΔV x (33R/130R)
000010	GVDD –ΔV x (2R/130R)	100010	GVDD –ΔV x (34R/130R)
000011	GVDD –ΔV x (3R/130R)	100011	GVDD –ΔV x (35R/130R)
000100	GVDD –ΔV x (4R/130R)	100100	GVDD –ΔV x (36R/130R)
000101	GVDD –ΔV x (5R/130R)	100101	GVDD –ΔV x (37R/130R)
000110	GVDD –ΔV x (6R/130R)	100110	GVDD –ΔV x (38R/130R)
000111	GVDD –ΔV x (7R/130R)	100111	GVDD –ΔV x (39R/130R)
001000	GVDD –ΔV x (8R/130R)	101000	GVDD –ΔV x (40R/130R)
001001	GVDD –ΔV x (9R/130R)	101001	GVDD –ΔV x (41R/130R)
001010	GVDD –ΔV x (10R/130R)	101010	GVDD –ΔV x (42R/130R)
001011	GVDD –ΔV x (11R/130R)	101011	GVDD –ΔV x (43R/130R)
001100	GVDD –ΔV x (12R/130R)	101100	GVDD –ΔV x (44R/130R)
001101	GVDD –ΔV x (13R/130R)	101101	GVDD –ΔV x (45R/130R)
001110	GVDD –ΔV x (14R/130R)	101110	GVDD –ΔV x (46R/130R)
001111	GVDD –ΔV x (15R/130R)	101111	GVDD –ΔV x (47R/130R)
010000	GVDD –ΔV x (16R/130R)	110000	GVDD –ΔV x (48R/130R)
010001	GVDD –ΔV x (17R/130R)	110001	GVDD –ΔV x (49R/130R)
010010	GVDD –ΔV x (18R/130R)	110010	GVDD –ΔV x (50R/130R)

010011	GVDD –ΔV x (19R/130R)	110011	GVDD –ΔV x (51R/130R)
010100	GVDD –ΔV x (20R/130R)	110100	GVDD –ΔV x (52R/130R)
010101	GVDD –ΔV x (21R/130R)	110101	GVDD –ΔV x (53R/130R)
010110	GVDD –ΔV x (22R/130R)	110110	GVDD –ΔV x (54R/130R)
010111	GVDD –ΔV x (23R/130R)	110111	GVDD –ΔV x (55R/130R)
011000	GVDD –ΔV x (24R/130R)	111000	GVDD –ΔV x (56R/130R)
011001	GVDD –ΔV x (25R/130R)	111001	GVDD –ΔV x (57R/130R)
011010	GVDD –ΔV x (26R/130R)	111010	GVDD –ΔV x (58R/130R)
011011	GVDD –ΔV x (27R/130R)	111011	GVDD –ΔV x (59R/130R)
011100	GVDD –ΔV x (28R/130R)	111100	GVDD –ΔV x (60R/130R)
011101	GVDD –ΔV x (29R/130R)	111101	GVDD –ΔV x (61R/130R)
011110	GVDD –ΔV x (30R/130R)	111110	GVDD –ΔV x (62R/130R)
011111	GVDD –ΔV x (31R/130R)	111111	GVDD –ΔV x (63R/130R)

ΔV: Potential difference between GVDD and AGND

Table3. Amplitude Adjustment (3)

VP(N)2[5:0]	Formula of VINP(N)2	VRP(N)2[5:0]	Formula of VINP(N)2
000000	GVDD –ΔV x (0R/130R)	100000	GVDD –ΔV x (32R/130R)
000001	GVDD –ΔV x (1R/130R)	100001	GVDD –ΔV x (33R/130R)
000010	GVDD –ΔV x (2R/130R)	100010	GVDD –ΔV x (34R/130R)
000011	GVDD –ΔV x (3R/130R)	100011	GVDD –ΔV x (35R/130R)
000100	GVDD –ΔV x (4R/130R)	100100	GVDD –ΔV x (36R/130R)
000101	GVDD –ΔV x (5R/130R)	100101	GVDD –ΔV x (37R/130R)
000110	GVDD –ΔV x (6R/130R)	100110	GVDD –ΔV x (38R/130R)
000111	GVDD –ΔV x (7R/130R)	100111	GVDD –ΔV x (39R/130R)
001000	GVDD –ΔV x (8R/130R)	101000	GVDD –ΔV x (40R/130R)
001001	GVDD –ΔV x (9R/130R)	101001	GVDD –ΔV x (41R/130R)
001010	GVDD –ΔV x (10R/130R)	101010	GVDD –ΔV x (42R/130R)
001011	GVDD –ΔV x (11R/130R)	101011	GVDD –ΔV x (43R/130R)
001100	GVDD –ΔV x (12R/130R)	101100	GVDD –ΔV x (44R/130R)
001101	GVDD –ΔV x (13R/130R)	101101	GVDD –ΔV x (45R/130R)
001110	GVDD –ΔV x (14R/130R)	101110	GVDD –ΔV x (46R/130R)
001111	GVDD –ΔV x (15R/130R)	101111	GVDD –ΔV x (47R/130R)
010000	GVDD –ΔV x (16R/130R)	110000	GVDD –ΔV x (48R/130R)
010001	GVDD –ΔV x (17R/130R)	110001	GVDD –ΔV x (49R/130R)
010010	GVDD –ΔV x (18R/130R)	110010	GVDD –ΔV x (50R/130R)
010011	GVDD –ΔV x (19R/130R)	110011	GVDD –ΔV x (51R/130R)
010100	GVDD –ΔV x (20R/130R)	110100	GVDD –ΔV x (52R/130R)
010101	GVDD –ΔV x (21R/130R)	110101	GVDD –ΔV x (53R/130R)
010110	GVDD –ΔV x (22R/130R)	110110	GVDD –ΔV x (54R/130R)
010111	GVDD –ΔV x (23R/130R)	110111	GVDD –ΔV x (55R/130R)
011000	GVDD –ΔV x (24R/130R)	111000	GVDD –ΔV x (56R/130R)
011001	GVDD –ΔV x (25R/130R)	111001	GVDD –ΔV x (57R/130R)
011010	GVDD –ΔV x (26R/130R)	111010	GVDD –ΔV x (58R/130R)
011011	GVDD –ΔV x (27R/130R)	111011	GVDD –ΔV x (59R/130R)
011100	GVDD –ΔV x (28R/130R)	111100	GVDD –ΔV x (60R/130R)
011101	GVDD –ΔV x (29R/130R)	111101	GVDD –ΔV x (61R/130R)
011110	GVDD –ΔV x (30R/130R)	111110	GVDD –ΔV x (62R/130R)
011111	GVDD –ΔV x (31R/130R)	111111	GVDD –ΔV x (63R/130R)

ΔV: Potential difference between GVDD and AGND

Table4. Reference Adjustment (1)

VP(N)61[5:0]	Formula of VINP(N)13	VRP(N)3[5:0]	Formula of VINP(N)13
000000	GVDD –ΔV x (67R/130R)	100000	GVDD –ΔV x (99R/130R)
000001	GVDD –ΔV x (68R/130R)	100001	GVDD –ΔV x (100R/130R)
000010	GVDD –ΔV x (69R/130R)	100010	GVDD –ΔV x (101R/130R)
000011	GVDD –ΔV x (70R/130R)	100011	GVDD –ΔV x (102R/130R)
000100	GVDD –ΔV x (71R/130R)	100100	GVDD –ΔV x (103R/130R)
000101	GVDD –ΔV x (72R/130R)	100101	GVDD –ΔV x (104R/130R)
000110	GVDD –ΔV x (73R/130R)	100110	GVDD –ΔV x (105R/130R)
000111	GVDD –ΔV x (74R/130R)	100111	GVDD –ΔV x (106R/130R)
001000	GVDD –ΔV x (75R/130R)	101000	GVDD –ΔV x (107R/130R)
001001	GVDD –ΔV x (76R/130R)	101001	GVDD –ΔV x (108R/130R)
001010	GVDD –ΔV x (77R/130R)	101010	GVDD –ΔV x (109R/130R)
001011	GVDD –ΔV x (78R/130R)	101011	GVDD –ΔV x (110R/130R)
001100	GVDD –ΔV x (79R/130R)	101100	GVDD –ΔV x (111R/130R)
001101	GVDD –ΔV x (80R/130R)	101101	GVDD –ΔV x (112R/130R)
001110	GVDD –ΔV x (81R/130R)	101110	GVDD –ΔV x (113R/130R)
001111	GVDD –ΔV x (82R/130R)	101111	GVDD –ΔV x (114R/130R)
010000	GVDD –ΔV x (83R/130R)	110000	GVDD –ΔV x (115R/130R)
010001	GVDD –ΔV x (84R/130R)	110001	GVDD –ΔV x (116R/130R)
010010	GVDD –ΔV x (85R/130R)	110010	GVDD –ΔV x (117R/130R)
010011	GVDD –ΔV x (86R/130R)	110011	GVDD –ΔV x (118R/130R)
010100	GVDD –ΔV x (87R/130R)	110100	GVDD –ΔV x (119R/130R)
010101	GVDD –ΔV x (88R/130R)	110101	GVDD –ΔV x (120R/130R)
010110	GVDD –ΔV x (89R/130R)	110110	GVDD –ΔV x (121R/130R)
010111	GVDD –ΔV x (90R/130R)	110111	GVDD –ΔV x (122R/130R)
011000	GVDD –ΔV x (91R/130R)	111000	GVDD –ΔV x (123R/130R)
011001	GVDD –ΔV x (92R/130R)	111001	GVDD –ΔV x (124R/130R)
011010	GVDD –ΔV x (93R/130R)	111010	GVDD –ΔV x (125R/130R)
011011	GVDD –ΔV x (94R/130R)	111011	GVDD –ΔV x (126R/130R)
011100	GVDD –ΔV x (95R/130R)	111100	GVDD –ΔV x (127R/130R)
011101	GVDD –ΔV x (96R/130R)	111101	GVDD –ΔV x (128R/130R)
011110	GVDD –ΔV x (97R/130R)	111110	GVDD –ΔV x (129R/130R)
011111	GVDD –ΔV x (98R/130R)	111111	GVDD –ΔV x (130R/130R)

ΔV: Potential difference between GVDD and AGND

Table5. Reference Adjustment (2)

VP(N)62[5:0]	Formula of VINP(N)14	VRP(N)4[5:0]	Formula of VINP(N)14
000000	GVDD –ΔV x (67R/130R)	100000	GVDD –ΔV x (99R/130R)
000001	GVDD –ΔV x (68R/130R)	100001	GVDD –ΔV x (100R/130R)
000010	GVDD –ΔV x (69R/130R)	100010	GVDD –ΔV x (101R/130R)
000011	GVDD –ΔV x (70R/130R)	100011	GVDD –ΔV x (102R/130R)
000100	GVDD –ΔV x (71R/130R)	100100	GVDD –ΔV x (103R/130R)
000101	GVDD –ΔV x (72R/130R)	100101	GVDD –ΔV x (104R/130R)
000110	GVDD –ΔV x (73R/130R)	100110	GVDD –ΔV x (105R/130R)
000111	GVDD –ΔV x (74R/130R)	100111	GVDD –ΔV x (106R/130R)
001000	GVDD –ΔV x (75R/130R)	101000	GVDD –ΔV x (107R/130R)
001001	GVDD –ΔV x (76R/130R)	101001	GVDD –ΔV x (108R/130R)
001010	GVDD –ΔV x (77R/130R)	101010	GVDD –ΔV x (109R/130R)
001011	GVDD –ΔV x (78R/130R)	101011	GVDD –ΔV x (110R/130R)
001100	GVDD –ΔV x (79R/130R)	101100	GVDD –ΔV x (111R/130R)
001101	GVDD –ΔV x (80R/130R)	101101	GVDD –ΔV x (112R/130R)
001110	GVDD –ΔV x (81R/130R)	101110	GVDD –ΔV x (113R/130R)
001111	GVDD –ΔV x (82R/130R)	101111	GVDD –ΔV x (114R/130R)
010000	GVDD –ΔV x (83R/130R)	110000	GVDD –ΔV x (115R/130R)
010001	GVDD –ΔV x (84R/130R)	110001	GVDD –ΔV x (116R/130R)
010010	GVDD –ΔV x (85R/130R)	110010	GVDD –ΔV x (117R/130R)
010011	GVDD –ΔV x (86R/130R)	110011	GVDD –ΔV x (118R/130R)

010100	GVDD –ΔV x (87R/130R)	110100	GVDD –ΔV x (119R/130R)
010101	GVDD –ΔV x (88R/130R)	110101	GVDD –ΔV x (120R/130R)
010110	GVDD –ΔV x (89R/130R)	110110	GVDD –ΔV x (121R/130R)
010111	GVDD –ΔV x (90R/130R)	110111	GVDD –ΔV x (122R/130R)
011000	GVDD –ΔV x (91R/130R)	111000	GVDD –ΔV x (123R/130R)
011001	GVDD –ΔV x (92R/130R)	111001	GVDD –ΔV x (124R/130R)
011010	GVDD –ΔV x (93R/130R)	111010	GVDD –ΔV x (125R/130R)
011011	GVDD –ΔV x (94R/130R)	111011	GVDD –ΔV x (126R/130R)
011100	GVDD –ΔV x (95R/130R)	111100	GVDD –ΔV x (127R/130R)
011101	GVDD –ΔV x (96R/130R)	111101	GVDD –ΔV x (128R/130R)
011110	GVDD –ΔV x (97R/130R)	111110	GVDD –ΔV x (129R/130R)
011111	GVDD –ΔV x (98R/130R)	111111	GVDD –ΔV x (130R/130R)

ΔV: Potential difference between GVDD and AGND

Table6. Reference Adjustment (3)

VP(N)63[5:0]	Formula of VINP(N)15	VRP(N)5[5:0]	Formula of VINP(N)15
000000	GVDD –ΔV x (67R/130R)	100000	GVDD –ΔV x (99R/130R)
000001	GVDD –ΔV x (68R/130R)	100001	GVDD –ΔV x (100R/130R)
000010	GVDD –ΔV x (69R/130R)	100010	GVDD –ΔV x (101R/130R)
000011	GVDD –ΔV x (70R/130R)	100011	GVDD –ΔV x (102R/130R)
000100	GVDD –ΔV x (71R/130R)	100100	GVDD –ΔV x (103R/130R)
000101	GVDD –ΔV x (72R/130R)	100101	GVDD –ΔV x (104R/130R)
000110	GVDD –ΔV x (73R/130R)	100110	GVDD –ΔV x (105R/130R)
000111	GVDD –ΔV x (74R/130R)	100111	GVDD –ΔV x (106R/130R)
001000	GVDD –ΔV x (75R/130R)	101000	GVDD –ΔV x (107R/130R)
001001	GVDD –ΔV x (76R/130R)	101001	GVDD –ΔV x (108R/130R)
001010	GVDD –ΔV x (77R/130R)	101010	GVDD –ΔV x (109R/130R)
001011	GVDD –ΔV x (78R/130R)	101011	GVDD –ΔV x (110R/130R)
001100	GVDD –ΔV x (79R/130R)	101100	GVDD –ΔV x (111R/130R)
001101	GVDD –ΔV x (80R/130R)	101101	GVDD –ΔV x (112R/130R)
001110	GVDD –ΔV x (81R/130R)	101110	GVDD –ΔV x (113R/130R)
001111	GVDD –ΔV x (82R/130R)	101111	GVDD –ΔV x (114R/130R)
010000	GVDD –ΔV x (83R/130R)	110000	GVDD –ΔV x (115R/130R)
010001	GVDD –ΔV x (84R/130R)	110001	GVDD –ΔV x (116R/130R)
010010	GVDD –ΔV x (85R/130R)	110010	GVDD –ΔV x (117R/130R)
010011	GVDD –ΔV x (86R/130R)	110011	GVDD –ΔV x (118R/130R)
010100	GVDD –ΔV x (87R/130R)	110100	GVDD –ΔV x (119R/130R)
010101	GVDD –ΔV x (88R/130R)	110101	GVDD –ΔV x (120R/130R)
010110	GVDD –ΔV x (89R/130R)	110110	GVDD –ΔV x (121R/130R)
010111	GVDD –ΔV x (90R/130R)	110111	GVDD –ΔV x (122R/130R)
011000	GVDD –ΔV x (91R/130R)	111000	GVDD –ΔV x (123R/130R)
011001	GVDD –ΔV x (92R/130R)	111001	GVDD –ΔV x (124R/130R)
011010	GVDD –ΔV x (93R/130R)	111010	GVDD –ΔV x (125R/130R)
011011	GVDD –ΔV x (94R/130R)	111011	GVDD –ΔV x (126R/130R)
011100	GVDD –ΔV x (95R/130R)	111100	GVDD –ΔV x (127R/130R)
011101	GVDD –ΔV x (96R/130R)	111101	GVDD –ΔV x (128R/130R)
011110	GVDD –ΔV x (97R/130R)	111110	GVDD –ΔV x (129R/130R)
011111	GVDD –ΔV x (98R/130R)	111111	GVDD –ΔV x (130R/130R)

ΔV: Potential difference between GVDD and AGND

Table7. Gradient Adjustment (1)

VP(N)20[5:0]	Formula of VINP(N)6	PRP(N)0[5:0]	Formula of VINP(N)6
000000	GVDD –ΔV x (31R/130R)	100000	GVDD –ΔV x (63R/130R)
000001	GVDD –ΔV x (32R/130R)	100001	GVDD –ΔV x (64R/130R)
000010	GVDD –ΔV x (33R/130R)	100010	GVDD –ΔV x (65R/130R)
000011	GVDD –ΔV x (34R/130R)	100011	GVDD –ΔV x (66R/130R)
000100	GVDD –ΔV x (35R/130R)	100100	GVDD –ΔV x (67R/130R)
000101	GVDD –ΔV x (36R/130R)	100101	GVDD –ΔV x (68R/130R)
000110	GVDD –ΔV x (37R/130R)	100110	GVDD –ΔV x (69R/130R)
000111	GVDD –ΔV x (38R/130R)	100111	GVDD –ΔV x (70R/130R)
001000	GVDD –ΔV x (39R/130R)	101000	GVDD –ΔV x (71R/130R)
001001	GVDD –ΔV x (40R/130R)	101001	GVDD –ΔV x (72R/130R)
001010	GVDD –ΔV x (41R/130R)	101010	GVDD –ΔV x (73R/130R)
001011	GVDD –ΔV x (42R/130R)	101011	GVDD –ΔV x (74R/130R)
001100	GVDD –ΔV x (43R/130R)	101100	GVDD –ΔV x (75R/130R)
001101	GVDD –ΔV x (44R/130R)	101101	GVDD –ΔV x (76R/130R)
001110	GVDD –ΔV x (45R/130R)	101110	GVDD –ΔV x (77R/130R)
001111	GVDD –ΔV x (46R/130R)	101111	GVDD –ΔV x (78R/130R)
010000	GVDD –ΔV x (47R/130R)	110000	GVDD –ΔV x (79R/130R)
010001	GVDD –ΔV x (48R/130R)	110001	GVDD –ΔV x (80R/130R)
010010	GVDD –ΔV x (49R/130R)	110010	GVDD –ΔV x (81R/130R)
010011	GVDD –ΔV x (50R/130R)	110011	GVDD –ΔV x (82R/130R)
010100	GVDD –ΔV x (51R/130R)	110100	GVDD –ΔV x (83R/130R)
010101	GVDD –ΔV x (52R/130R)	110101	GVDD –ΔV x (84R/130R)
010110	GVDD –ΔV x (53R/130R)	110110	GVDD –ΔV x (85R/130R)
010111	GVDD –ΔV x (54R/130R)	110111	GVDD –ΔV x (86R/130R)
011000	GVDD –ΔV x (55R/130R)	111000	GVDD –ΔV x (87R/130R)
011001	GVDD –ΔV x (56R/130R)	111001	GVDD –ΔV x (88R/130R)
011010	GVDD –ΔV x (57R/130R)	111010	GVDD –ΔV x (89R/130R)
011011	GVDD –ΔV x (58R/130R)	111011	GVDD –ΔV x (90R/130R)
011100	GVDD –ΔV x (59R/130R)	111100	GVDD –ΔV x (91R/130R)
011101	GVDD –ΔV x (60R/130R)	111101	GVDD –ΔV x (92R/130R)
011110	GVDD –ΔV x (61R/130R)	111110	GVDD –ΔV x (93R/130R)
011111	GVDD –ΔV x (62R/130R)	111111	GVDD –ΔV x (94R/130R)

ΔV: Potential difference between GVDD and AGND

Table8. Gradient Adjustment (2)

VP(N)43[5:0]	Formula of VINP(N)9	PRP(N)1[5:0]	Formula of VINP(N)9
000000	GVDD –ΔV x (36R/130R)	100000	GVDD –ΔV x (68R/130R)
000001	GVDD –ΔV x (37R/130R)	100001	GVDD –ΔV x (69R/130R)
000010	GVDD –ΔV x (38R/130R)	100010	GVDD –ΔV x (70R/130R)
000011	GVDD –ΔV x (39R/130R)	100011	GVDD –ΔV x (71R/130R)
000100	GVDD –ΔV x (40R/130R)	100100	GVDD –ΔV x (72R/130R)
000101	GVDD –ΔV x (41R/130R)	100101	GVDD –ΔV x (73R/130R)
000110	GVDD –ΔV x (42R/130R)	100110	GVDD –ΔV x (74R/130R)
000111	GVDD –ΔV x (43R/130R)	100111	GVDD –ΔV x (75R/130R)
001000	GVDD –ΔV x (44R/130R)	101000	GVDD –ΔV x (76R/130R)
001001	GVDD –ΔV x (45R/130R)	101001	GVDD –ΔV x (77R/130R)
001010	GVDD –ΔV x (46R/130R)	101010	GVDD –ΔV x (78R/130R)
001011	GVDD –ΔV x (47R/130R)	101011	GVDD –ΔV x (79R/130R)
001100	GVDD –ΔV x (48R/130R)	101100	GVDD –ΔV x (80R/130R)
001101	GVDD –ΔV x (49R/130R)	101101	GVDD –ΔV x (81R/130R)
001110	GVDD –ΔV x (50R/130R)	101110	GVDD –ΔV x (82R/130R)
001111	GVDD –ΔV x (51R/130R)	101111	GVDD –ΔV x (83R/130R)
010000	GVDD –ΔV x (52R/130R)	110000	GVDD –ΔV x (84R/130R)
010001	GVDD –ΔV x (53R/130R)	110001	GVDD –ΔV x (85R/130R)
010010	GVDD –ΔV x (54R/130R)	110010	GVDD –ΔV x (86R/130R)
010011	GVDD –ΔV x (55R/130R)	110011	GVDD –ΔV x (87R/130R)
010100	GVDD –ΔV x (56R/130R)	110100	GVDD –ΔV x (88R/130R)
010101	GVDD –ΔV x (57R/130R)	110101	GVDD –ΔV x (89R/130R)
010110	GVDD –ΔV x (58R/130R)	110110	GVDD –ΔV x (90R/130R)
010111	GVDD –ΔV x (59R/130R)	110111	GVDD –ΔV x (91R/130R)
011000	GVDD –ΔV x (60R/130R)	111000	GVDD –ΔV x (92R/130R)
011001	GVDD –ΔV x (61R/130R)	111001	GVDD –ΔV x (93R/130R)
011010	GVDD –ΔV x (62R/130R)	111010	GVDD –ΔV x (94R/130R)
011011	GVDD –ΔV x (63R/130R)	111011	GVDD –ΔV x (95R/130R)
011100	GVDD –ΔV x (64R/130R)	111100	GVDD –ΔV x (96R/130R)
011101	GVDD –ΔV x (65R/130R)	111101	GVDD –ΔV x (97R/130R)
011110	GVDD –ΔV x (66R/130R)	111110	GVDD –ΔV x (98R/130R)
011111	GVDD –ΔV x (67R/130R)	111111	GVDD –ΔV x (99R/130R)

ΔV: Potential difference between GVDD and AGND

Table9. Macro adjustment

Macro adjusting register	Register values	Formula	Reference Voltage
VP(N)4	000000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (0R/47R)	VINP(N)3
	000001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (1R/47R)	
	000010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (2R/47R)	
	000011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (3R/47R)	
	000100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (4R/47R)	
	000101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (5R/47R)	
	000110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (6R/47R)	
	000111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (7R/47R)	
	001000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (8R/47R)	
	001001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (9R/47R)	
	001010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (10R/47R)	
	001011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (11R/47R)	
	001100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (12R/47R)	
	001101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (13R/47R)	
	001110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (14R/47R)	
	001111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (15R/47R)	
	010000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (16R/47R)	
	010001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (17R/47R)	
	010010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (18R/47R)	
	010011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (19R/47R)	
	010100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (20R/47R)	
	010101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (21R/47R)	
	010110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (22R/47R)	
	010111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (23R/47R)	
	011000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (24R/47R)	
	011001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (25R/47R)	
	011010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (26R/47R)	
	011011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (27R/47R)	
	011100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (28R/47R)	
	011101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (29R/47R)	
	011110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (30R/47R)	
	011111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (31R/47R)	
	100000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (32R/47R)	
	100001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (33R/47R)	
	100010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (34R/47R)	
	100011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (35R/47R)	
	100100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (36R/47R)	
	100101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (37R/47R)	
	100110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (38R/47R)	
	100111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (39R/47R)	
	101000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (40R/47R)	
	101001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (41R/47R)	
	101010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (42R/47R)	
	101011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (43R/47R)	
	101100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (44R/47R)	
	101101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (45R/47R)	
	101110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (46R/47R)	
	101111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (47R/47R)	
VP(N)6	000000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (0R/47R)	VINP(N)4
	000001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (1R/47R)	
	000010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (2R/47R)	
	000011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (3R/47R)	
	000100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (4R/47R)	
	000101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (5R/47R)	
	000110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (6R/47R)	
	000111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (7R/47R)	
	001000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (8R/47R)	

	001001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (9R/47R)	
	001010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (10R/47R)	
	001011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (11R/47R)	
	001100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (12R/47R)	
	001101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (13R/47R)	
	001110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (14R/47R)	
	001111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (15R/47R)	
	010000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (16R/47R)	
	010001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (17R/47R)	
	010010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (18R/47R)	
	010011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (19R/47R)	
	010100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (20R/47R)	
	010101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (21R/47R)	
	010110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (22R/47R)	
	010111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (23R/47R)	
	011000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (24R/47R)	
	011001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (25R/47R)	
	011010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (26R/47R)	
	011011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (27R/47R)	
	011100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (28R/47R)	
	011101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (29R/47R)	
	011110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (30R/47R)	
	011111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (31R/47R)	
	100000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (32R/47R)	
	100001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (33R/47R)	
	100010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (34R/47R)	
	100011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (35R/47R)	
	100100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (36R/47R)	
	100101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (37R/47R)	
	100110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (38R/47R)	
	100111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (39R/47R)	
	101000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (40R/47R)	
	101001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (41R/47R)	
	101010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (42R/47R)	
	101011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (43R/47R)	
	101100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (44R/47R)	
	101101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (45R/47R)	
	101110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (46R/47R)	
	101111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (47R/47R)	
VP(N)13	00000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (16R/47R)	VINP(N)5
	00001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (17R/47R)	
	00010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (18R/47R)	
	00011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (19R/47R)	
	00100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (20R/47R)	
	00101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (21R/47R)	
	00110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (22R/47R)	
	00111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (23R/47R)	
	01000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (24R/47R)	
	01001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (25R/47R)	
	01010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (26R/47R)	
	01011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (27R/47R)	
	01100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (28R/47R)	
	01101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (29R/47R)	
	01110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (30R/47R)	
	01111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (31R/47R)	
	10000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (32R/47R)	
	10001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (33R/47R)	
	10010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (34R/47R)	
	10011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (35R/47R)	
	10100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (36R/47R)	
	10101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (37R/47R)	

	10110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (38R/47R)	
	10111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (39R/47R)	
	11000	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (40R/47R)	
	11001	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (41R/47R)	
	11010	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (42R/47R)	
	11011	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (43R/47R)	
	11100	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (44R/47R)	
	11101	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (45R/47R)	
	11110	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (46R/47R)	
	11111	VINP(N)2 – (VINP(N)2 – VINP(N)6) x (47R/47R)	
VP(N)27	0000	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (3R/39R)	VINP(N)7
	0001	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (4R/39R)	
	0010	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (5R/39R)	
	0011	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (6R/39R)	
	0100	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (7R/39R)	
	0101	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (8R/39R)	
	0110	VINP(N)6 – (VINP(N) – VINP(N)9) x (9R/39R)	
	0111	VINP(N)6– (VINP(N)6 – VINP(N)9) x (10R/39R)	
	1000	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (11R/39R)	
	1001	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (12R/39R)	
	1010	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (13R/39R)	
	1011	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (14R/39R)	
	1100	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (15R/39R)	
	1101	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (16R/39R)	
	1110	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (17R/39R)	
	1111	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (18R/39R)	
VP(N)36	0000	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (21R/39R)	VINP(N)8
	0001	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (22R/39R)	
	0010	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (23R/39R)	
	0011	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (24R/39R)	
	0100	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (25R/39R)	
	0101	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (26R/39R)	
	0110	VINP(N)6 – (VINP(N) – VINP(N)9) x (27R/39R)	
	0111	VINP(N)6– (VINP(N)6 – VINP(N)9) x (28R/39R)	
	1000	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (29R/39R)	
	1001	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (30R/39R)	
	1010	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (31R/39R)	
	1011	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (32R/39R)	
	1100	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (33R/39R)	
	1101	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (34R/39R)	
	1110	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (35R/39R)	
	1111	VINP(N)6 – (VINP(N)6 – VINP(N)9) x (36R/39R)	
VP(N)50	00000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (1R/47R)	VINP(N)10
	00001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (2R/47R)	
	00010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (3R/47R)	
	00011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (4R/47R)	
	00100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (5R/47R)	
	00101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (6R/47R)	
	00110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (7R/47R)	
	00111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (8R/47R)	
	01000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (9R/47R)	
	01001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (10R/47R)	
	01010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (11R/47R)	
	01011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (12R/47R)	
	01100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (13R/47R)	
	01101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (14R/47R)	
	01110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (15R/47R)	
	01111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (16R/47R)	
	10000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (17R/47R)	
	10001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (18R/47R)	
	10010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (19R/47R)	

	10011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (20R/47R)	
	10100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (21R/47R)	
	10101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (22R/47R)	
	10110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (23R/47R)	
	10111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (24R/47R)	
	11000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (25R/47R)	
	11001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (26R/47R)	
	11010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (27R/47R)	
	11011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (28R/47R)	
	11100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (29R/47R)	
	11101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (30R/47R)	
	11110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (31R/47R)	
	11111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (32R/47R)	
VP(N)57	000000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (0R/47R)	VINP(N)11
	000001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (1R/47R)	
	000010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (2R/47R)	
	000011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (3R/47R)	
	000100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (4R/47R)	
	000101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (5R/47R)	
	000110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (6R/47R)	
	000111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (7R/47R)	
	001000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (8R/47R)	
	001001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (9R/47R)	
	001010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (10R/47R)	
	001011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (11R/47R)	
	001100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (12R/47R)	
	001101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (13R/47R)	
	001110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (14R/47R)	
	001111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (15R/47R)	
	010000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (16R/47R)	
	010001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (17R/47R)	
	010010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (18R/47R)	
	010011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (19R/47R)	
	010100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (20R/47R)	
	010101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (21R/47R)	
	010110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (22R/47R)	
	010111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (23R/47R)	
	011000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (24R/47R)	
	011001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (25R/47R)	
	011010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (26R/47R)	
	011011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (27R/47R)	
	011100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (28R/47R)	
	011101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (29R/47R)	
	011110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (30R/47R)	
	011111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (31R/47R)	
	100000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (32R/47R)	
	100001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (33R/47R)	
	100010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (34R/47R)	
	100011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (35R/47R)	
	100100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (36R/47R)	
	100101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (37R/47R)	
	100110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (38R/47R)	
	100111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (39R/47R)	
	101000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (40R/47R)	
	101001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (41R/47R)	
	101010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (42R/47R)	
	101011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (43R/47R)	
	101100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (44R/47R)	
	101101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (45R/47R)	
	101110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (46R/47R)	
	101111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (47R/47R)	

VP(N)59	000000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (0R/47R)	VINP(N)12
	000001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (1R/47R)	
	000010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (2R/47R)	
	000011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (3R/47R)	
	000100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (4R/47R)	
	000101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (5R/47R)	
	000110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (6R/47R)	
	000111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (7R/47R)	
	001000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (8R/47R)	
	001001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (9R/47R)	
	001010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (10R/47R)	
	001011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (11R/47R)	
	001100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (12R/47R)	
	001101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (13R/47R)	
	001110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (14R/47R)	
	001111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (15R/47R)	
	010000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (16R/47R)	
	010001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (17R/47R)	
	010010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (18R/47R)	
	010011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (19R/47R)	
	010100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (20R/47R)	
	010101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (21R/47R)	
	010110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (22R/47R)	
	010111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (23R/47R)	
	011000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (24R/47R)	
	011001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (25R/47R)	
	011010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (26R/47R)	
	011011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (27R/47R)	
	011100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (28R/47R)	
	011101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (29R/47R)	
	011110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (30R/47R)	
	011111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (31R/47R)	
	100000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (32R/47R)	
	100001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (33R/47R)	
	100010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (34R/47R)	
	100011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (35R/47R)	
	100100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (36R/47R)	
	100101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (37R/47R)	
	100110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (38R/47R)	
	100111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (39R/47R)	
	101000	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (40R/47R)	
	101001	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (41R/47R)	
	101010	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (42R/47R)	
	101011	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (43R/47R)	
	101100	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (44R/47R)	
	101101	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (45R/47R)	
	101110	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (46R/47R)	
	101111	VINP(N)9 – (VINP(N)9 – VINP(N)13) x (47R/47R)	

Table10. Formula for calculating Gamma adjusting voltage (Positive Polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V36 + (V27 – V36) x (80 / 180)
V1	VINP1	V33	V36 + (V27 – V36) x (60 / 180)
V2	VINP2	V34	V36 + (V27 – V36) x (40 / 180)
V3	V4 + (V2 – V4) x (75 / 155)	V35	V36 + (V27 – V36) x (20 / 180)
V4	VINP3	V36	VINP8
V5	V6 + (V4 – V6) x (65 / 135)	V37	V43 + (V36 – V43) x (120 / 140)
V6	VINP4	V38	V43 + (V36 – V43) x (100 / 140)
V7	V13 + (V7 – V13) x (305 / 365)	V39	V43 + (V36 – V43) x (80 / 140)
V8	V13 + (V7 – V13) x (245 / 365)	V40	V43 + (V36 – V43) x (60 / 140)
V9	V13 + (V7 – V13) x (190 / 365)	V41	V43 + (V36 – V43) x (40 / 140)
V10	V13 + (V7 – V13) x (135 / 365)	V42	V43 + (V36 – V43) x (20 / 140)
V11	V13 + (V7 – V13) x (85 / 365)	V43	VINP9
V12	V13 + (V7 – V13) x (40 / 365)	V44	V50 + (V43 – V50) x (120 / 140)
V13	VINP5	V45	V50 + (V43 – V50) x (100 / 140)
V14	V20 + (V13 – V20) x (175 / 210)	V46	V50 + (V43 – V50) x (80 / 140)
V15	V20 + (V13 – V20) x (140 / 210)	V47	V50 + (V43 – V50) x (60 / 140)
V16	V20 + (V13 – V20) x (110 / 210)	V48	V50 + (V43 – V50) x (40 / 140)
V17	V20 + (V13 – V20) x (80 / 210)	V49	V50 + (V43 – V50) x (20 / 140)
V18	V20 + (V13 – V20) x (50 / 210)	V50	VINP10
V19	V20 + (V13 – V20) x (25 / 210)	V51	V57 + (V50 – V57) x (140 / 160)
V20	VINP6	V52	V57 + (V50 – V57) x (120 / 160)
V21	V27 + (V20 – V27) x (140 / 165)	V53	V57 + (V50 – V57) x (100 / 160)
V22	V27 + (V20 – V27) x (115 / 165)	V54	V57 + (V50 – V57) x (75 / 160)
V23	V27 + (V20 – V27) x (90 / 165)	V55	V57 + (V50 – V57) x (50 / 160)
V24	V27 + (V20 – V27) x (65 / 165)	V56	V57 + (V50 – V57) x (25 / 160)
V25	V27 + (V20 – V27) x (40 / 165)	V57	VINP11
V26	V27 + (V20 – V27) x (20 / 165)	V58	V59 + (V57 – V59) x (35 / 65)
V27	VINP7	V59	VINP12
V28	V36 + (V27 – V36) x (160 / 180)	V60	V61 + (V59 – V61) x (45 / 85)
V29	V36 + (V27 – V36) x (140 / 180)	V61	VINP13
V30	V36 + (V27 – V36) x (120 / 180)	V62	VINP14
V31	V36 + (V27 – V36) x (100 / 180)	V63	VINP15

Table11. Formula for calculating Gamma adjusting voltage (Negative Polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V36 + (V27 – V36) x (80 / 180)
V1	VINN1	V33	V36 + (V27 – V36) x (60 / 180)
V2	VINN2	V34	V36 + (V27 – V36) x (40 / 180)
V3	V4 + (V2 – V4) x (40 / 85)	V35	V36 + (V27 – V36) x (20 / 180)
V4	VINN3	V36	VINN8
V5	V6 + (V4 – V6) x (30 / 65)	V37	V43 + (V36 – V43) x (145 / 165)
V6	VINN4	V38	V43 + (V36 – V43) x (125 / 165)
V7	V13 + (V7 – V13) x (135 / 160)	V39	V43 + (V36 – V43) x (100 / 165)
V8	V13 + (V7 – V13) x (110 / 160)	V40	V43 + (V36 – V43) x (75 / 165)
V9	V13 + (V7 – V13) x (85 / 160)	V41	V43 + (V36 – V43) x (50 / 165)
V10	V13 + (V7 – V13) x (60 / 160)	V42	V43 + (V36 – V43) x (25 / 165)
V11	V13 + (V7 – V13) x (40 / 160)	V43	VINN9
V12	V13 + (V7 – V13) x (20 / 160)	V44	V50 + (V43 – V50) x (185 / 210)
V13	VINN5	V45	V50 + (V43 – V50) x (160 / 210)
V14	V20 + (V13 – V20) x (120 / 140)	V46	V50 + (V43 – V50) x (130 / 210)
V15	V20 + (V13 – V20) x (100 / 140)	V47	V50 + (V43 – V50) x (100 / 210)
V16	V20 + (V13 – V20) x (80 / 140)	V48	V50 + (V43 – V50) x (70 / 210)
V17	V20 + (V13 – V20) x (60 / 140)	V49	V50 + (V43 – V50) x (35 / 210)
V18	V20 + (V13 – V20) x (40 / 140)	V50	VINN10
V19	V20 + (V13 – V20) x (20 / 140)	V51	V57 + (V50 – V57) x (325 / 365)
V20	VINN6	V52	V57 + (V50 – V57) x (280 / 365)
V21	V27 + (V20 – V27) x (120 / 140)	V53	V57 + (V50 – V57) x (230 / 365)
V22	V27 + (V20 – V27) x (100 / 140)	V54	V57 + (V50 – V57) x (175 / 365)
V23	V27 + (V20 – V27) x (80 / 140)	V55	V57 + (V50 – V57) x (120 / 365)
V24	V27 + (V20 – V27) x (60 / 140)	V56	V57 + (V50 – V57) x (60 / 365)
V25	V27 + (V20 – V27) x (40 / 140)	V57	VINN11
V26	V27 + (V20 – V27) x (20 / 140)	V58	V59 + (V57 – V59) x (70 / 135)
V27	VINN7	V59	VINN12
V28	V36 + (V27 – V36) x (160 / 180)	V60	V61 + (V59 – V61) x (80 / 155)
V29	V36 + (V27 – V36) x (140 / 180)	V61	VINN13
V30	V36 + (V27 – V36) x (120 / 180)	V62	VINN14
V31	V36 + (V27 – V36) x (100 / 180)	V63	VINN15

5.9.3 Gray Voltage Generator for Source Driver

The NT39125 present four gamma curves (Gamma1.0, Gamma1.8, Gamma2.2 and Gamma2.5). And the gamma curve can be selected by setting the GC0~GC3. (see command GAMSET)

Data	Output Voltage (TN-TM-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	1	1.8	2.2	2.5	Gamma	1	1.8	2.2	2.5
0	V0+	4.800	4.800	4.800	4.800	V0-	0.111	0.111	0.111	0.111
1	V1+	3.212	4.505	4.763	3.212	V1-	1.698	0.406	0.148	1.698
2	V2+	2.880	4.098	4.652	2.880	V2-	2.031	0.812	0.258	2.031
3	V3+	2.753	3.851	4.459	2.753	V3-	2.157	1.060	0.452	2.157
4	V4+	2.635	3.618	4.278	2.635	V4-	2.276	1.292	0.633	2.276
5	V5+	2.557	3.408	4.062	2.557	V5-	2.354	1.503	0.849	2.354
6	V6+	2.484	3.212	3.861	2.484	V6-	2.427	1.698	1.050	2.427
7	V7+	2.434	3.121	3.731	2.434	V7-	2.476	1.799	1.180	2.476
8	V8+	2.385	3.030	3.601	2.385	V8-	2.526	1.881	1.310	2.526
9	V9+	2.339	2.947	3.482	2.339	V9-	2.571	1.964	1.429	2.571
0A	V10+	2.294	2.863	3.363	2.294	V10-	2.617	2.047	1.548	2.617
0B	V11+	2.253	2.787	3.254	2.253	V11-	2.658	2.123	1.656	2.658
0C	V12+	2.215	2.719	3.157	2.215	V12-	2.695	2.192	1.754	2.695
0D	V13+	2.182	2.658	3.070	2.182	V13-	2.728	2.252	1.841	2.728
0E	V14+	2.151	2.609	3.008	2.151	V14-	2.760	2.302	1.903	2.760
0F	V15+	2.120	2.560	2.945	2.120	V15-	2.791	2.351	1.966	2.791
10	V16+	2.093	2.518	2.892	2.093	V16-	2.818	2.393	2.019	2.818
11	V17+	2.066	2.476	2.838	2.066	V17-	2.845	2.435	2.073	2.845
12	V18+	2.039	2.433	2.785	2.039	V18-	2.872	2.477	2.126	2.872
13	V19+	2.016	2.398	2.740	2.016	V19-	2.894	2.513	2.171	2.894
14	V20+	1.994	2.363	2.695	1.994	V20-	2.917	2.548	2.215	2.917
15	V21+	1.975	2.333	2.652	1.975	V21-	2.936	2.578	2.256	2.936
16	V22+	1.956	2.303	2.609	1.956	V22-	2.955	2.607	2.296	2.955
17	V23+	1.937	2.274	2.566	1.937	V23-	2.974	2.637	2.336	2.974
18	V24+	1.918	2.244	2.523	1.918	V24-	2.993	2.667	2.376	2.993
19	V25+	1.899	2.214	2.480	1.899	V25-	3.012	2.697	2.416	3.012
1A	V26+	1.884	2.190	2.446	1.884	V26-	3.027	2.721	2.448	3.027
1B	V27+	1.869	2.166	2.411	1.869	V27-	3.042	2.745	2.480	3.042
1C	V28+	1.852	2.141	2.384	1.852	V28-	3.059	2.770	2.512	3.059
1D	V29+	1.834	2.116	2.357	1.834	V29-	3.077	2.795	2.544	3.077
1E	V30+	1.817	2.090	2.329	1.817	V30-	3.094	2.820	2.575	3.094
1F	V31+	1.799	2.065	2.302	1.799	V31-	3.111	2.846	2.607	3.111
20	V32+	1.782	2.040	2.275	1.782	V32-	3.129	2.871	2.638	3.129
21	V33+	1.765	2.015	2.247	1.765	V33-	3.146	2.896	2.670	3.146
22	V34+	1.747	1.989	2.220	1.747	V34-	3.163	2.921	2.701	3.163
23	V35+	1.730	1.964	2.193	1.730	V35-	3.181	2.947	2.733	3.181
24	V36+	1.713	1.939	2.165	1.713	V36-	3.198	2.972	2.764	3.198
25	V37+	1.695	1.915	2.135	1.695	V37-	3.216	2.996	2.792	3.216
26	V38+	1.677	1.891	2.106	1.677	V38-	3.234	3.019	2.819	3.234
27	V39+	1.659	1.868	2.076	1.659	V39-	3.252	3.043	2.846	3.252
28	V40+	1.641	1.844	2.046	1.641	V40-	3.270	3.067	2.873	3.270
29	V41+	1.623	1.820	2.016	1.623	V41-	3.287	3.091	2.900	3.287

2A	V42+	1.606	1.796	1.987	1.606	V42-	3.305	3.115	2.927	3.305
2B	V43+	1.588	1.772	1.957	1.588	V43-	3.323	3.138	2.954	3.323
2C	V44+	1.566	1.746	1.929	1.566	V44-	3.345	3.165	2.979	3.345
2D	V45+	1.544	1.719	1.901	1.544	V45-	3.367	3.192	3.005	3.367
2E	V46+	1.522	1.692	1.874	1.522	V46-	3.389	3.219	3.031	3.389
2F	V47+	1.500	1.665	1.846	1.500	V47-	3.411	3.245	3.056	3.411
30	V48+	1.478	1.639	1.818	1.478	V48-	3.433	3.272	3.082	3.433
31	V49+	1.456	1.612	1.791	1.456	V49-	3.455	3.299	3.107	3.455
32	V50+	1.434	1.585	1.763	1.434	V50-	3.477	3.325	3.133	3.477
33	V51+	1.412	1.557	1.731	1.412	V51-	3.499	3.354	3.167	3.499
34	V52+	1.390	1.529	1.699	1.390	V52-	3.521	3.382	3.200	3.521
35	V53+	1.368	1.500	1.668	1.368	V53-	3.543	3.411	3.234	3.543
36	V54+	1.340	1.465	1.628	1.340	V54-	3.571	3.446	3.276	3.571
37	V55+	1.313	1.429	1.588	1.313	V55-	3.598	3.482	3.318	3.598
38	V56+	1.285	1.394	1.549	1.285	V56-	3.626	3.517	3.360	3.626
39	V57+	1.258	1.358	1.509	1.258	V57-	3.653	3.552	3.402	3.653
3A	V58+	1.222	1.315	1.454	1.222	V58-	3.689	3.596	3.457	3.689
3B	V59+	1.181	1.265	1.390	1.181	V59-	3.730	3.646	3.521	3.730
3C	V60+	1.129	1.208	1.327	1.129	V60-	3.782	3.703	3.584	3.782
3D	V61+	1.071	1.145	1.255	1.071	V61-	3.840	3.766	3.655	3.840
3E	V62+	0.960	1.034	1.108	0.960	V62-	3.951	3.877	3.803	3.951
3F	V63+	0.702	0.702	0.702	0.702	V63-	4.209	4.209	4.209	4.209

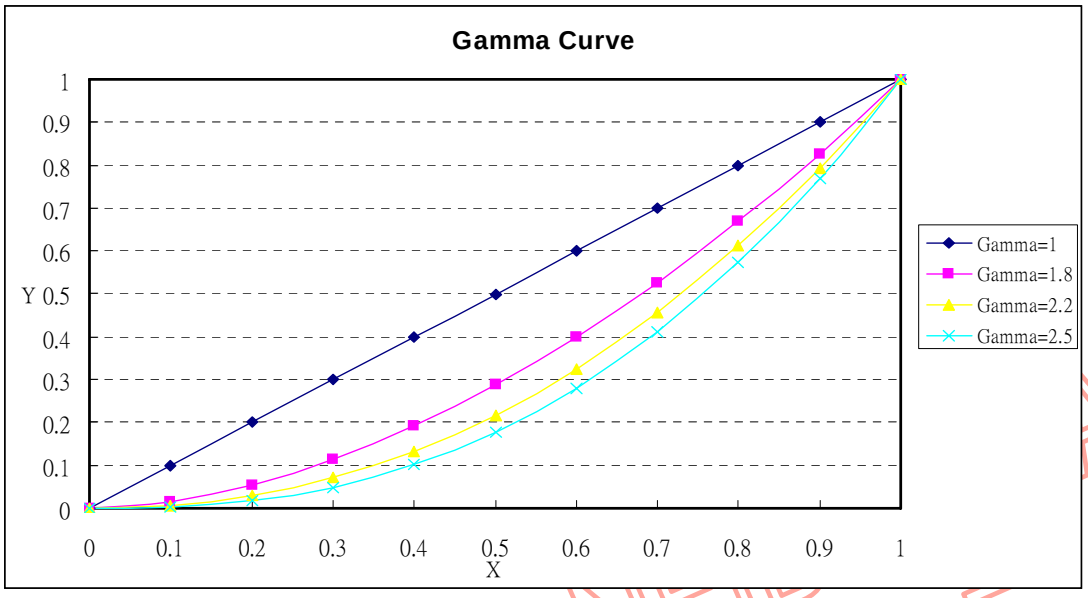


Fig. 5.9.3 Gamma Curve according to the GC0 to GC3 bit

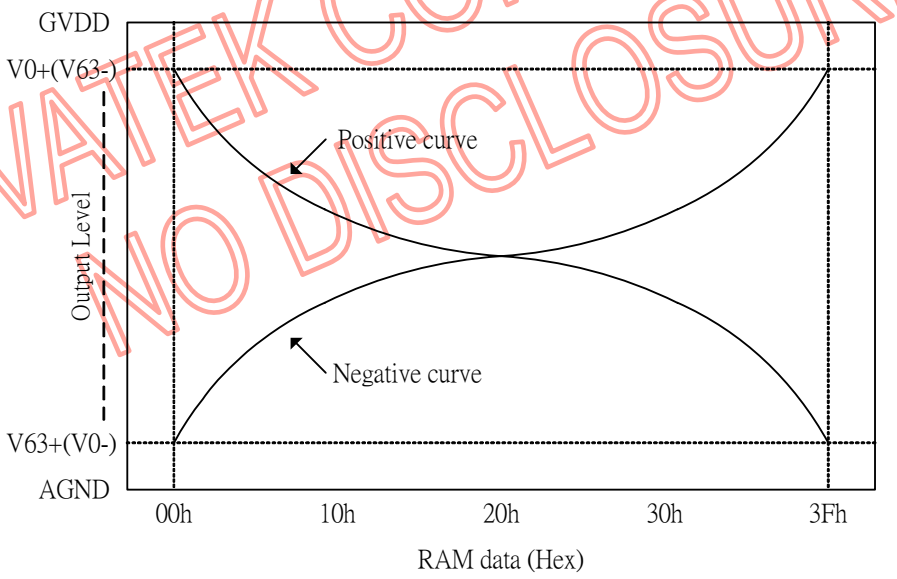


Fig. 5.9.4 Relationship between RAM data and output level

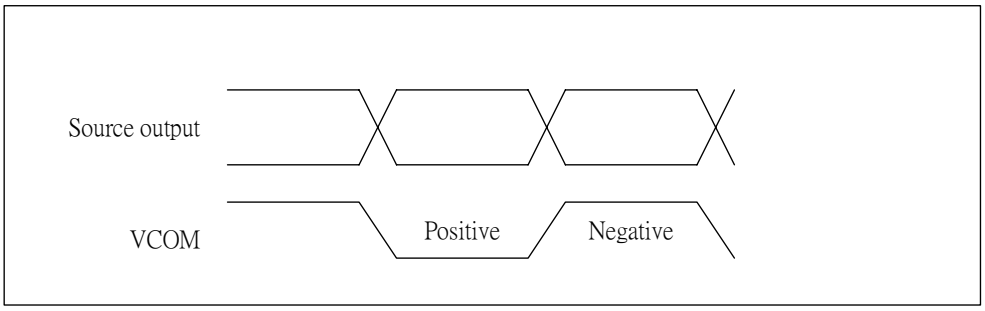


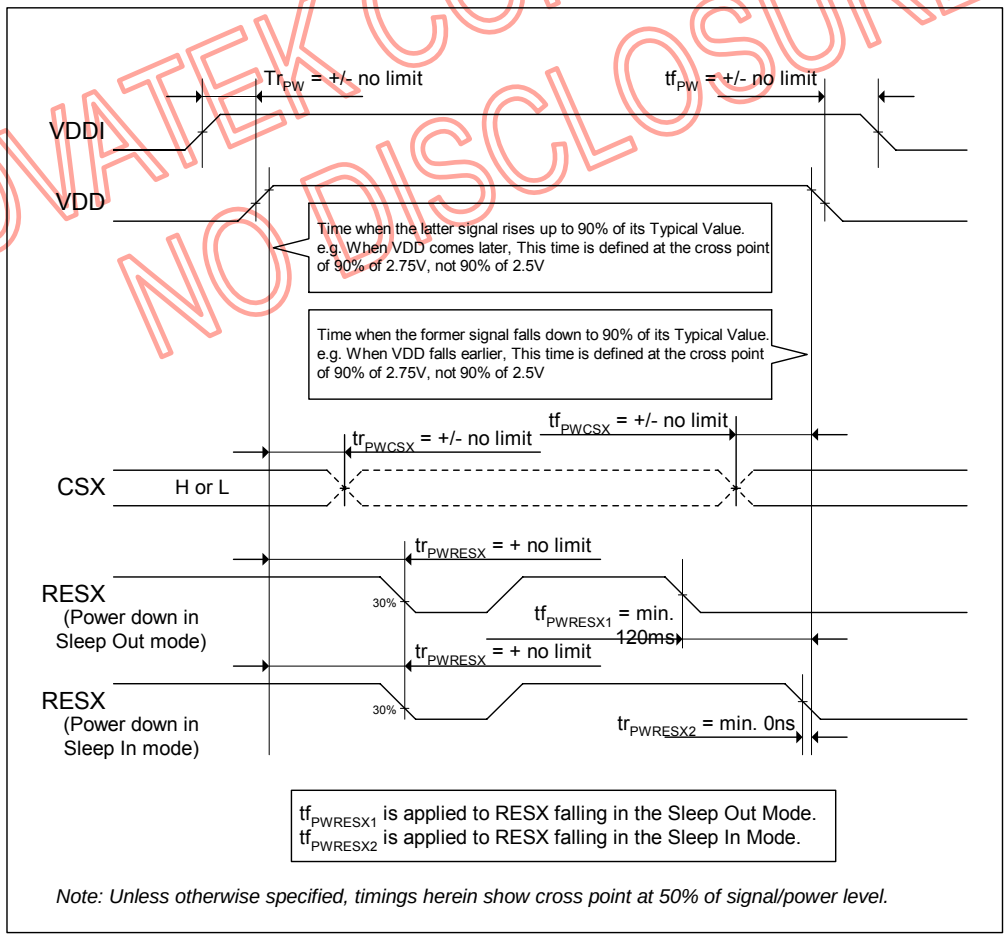
Fig. 5.9.5 Relationship between source output and VCOM

5.10 POWER ON/OFF SEQUENCE

IOVCC and VCI can be applied in any order.
VCI and IOVCC can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.
SCEX can be applied at any timing or can be permanently grounded. RESX has priority over SCEX.
There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.10.1 and 5.10.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
The power on/off sequence is illustrated below:

5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

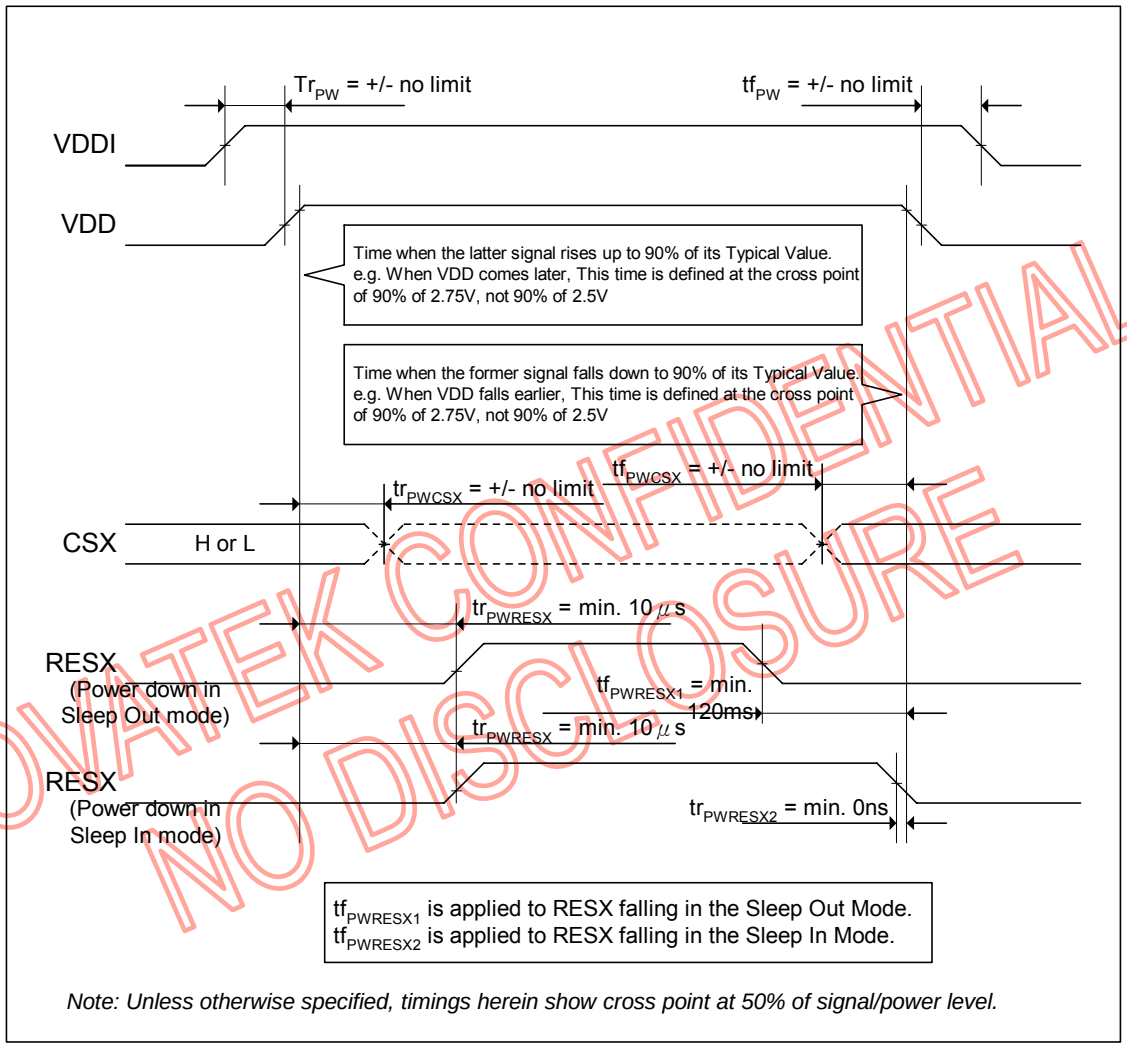
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.10.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and IOVCC have been applied.

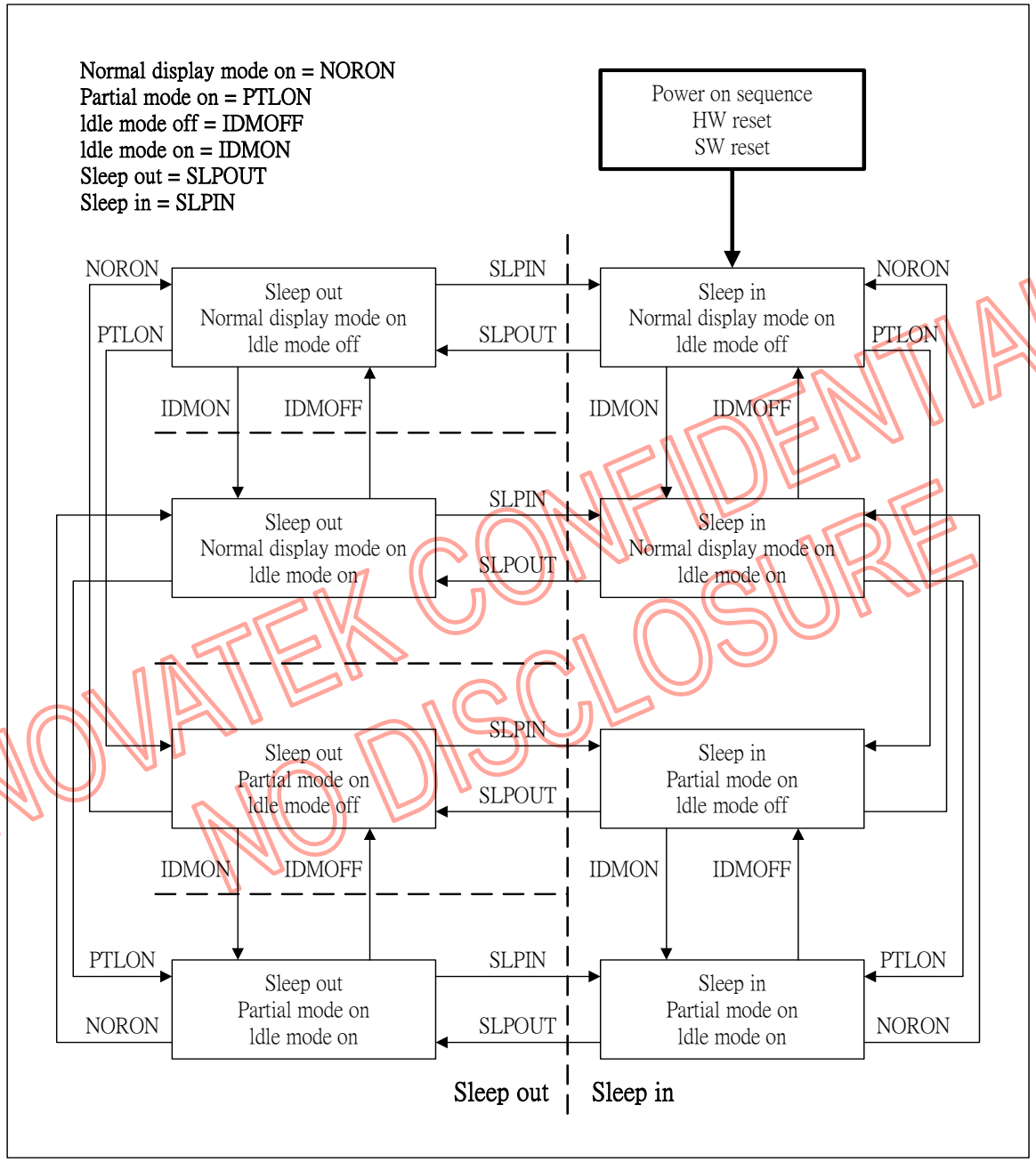


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.11 UNCONTROLLED POWER OFF

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.12 POWER FLOW CHART FOR DIFFERENT POWER MODES



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.
Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

5.13 INPUT / OUTPUT PIN STATE

5.13.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
TEST pins	Low	Low	Low

Note: There will be no output from D17-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

5.13.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 5.10	Input valid	Input valid	Input valid	See Section 5.10
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D17 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS	Input invalid	Input valid	Input valid	Input valid	Input invalid
VS	Input invalid	Input valid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input valid	Input invalid
P68, 4WSPI, IM2, IM1, IM0, GM1, GM0, RCM	Input invalid	Input valid	Input valid	Input valid	Input invalid

6 INSTRUCTION DESCRIPTION

6.1 System function Command List and Description

6.1.1 System Function Instruction Code Table

Table 6.1.1 Instruction Code

NO	Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	NOP	0	W	0	0	0	0	0	0	0	0	00h	No Operation
2	SWRESET	0	W	0	0	0	0	0	0	0	1	01h	Software reset
3	RDDID	0	W	0	0	0	0	0	1	0	0	04h	Read Display ID
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	0	0	1	1	1	0	0	0	-	38h
		1	R	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	ID2 read
		1	R	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	ID3 read
4	RDDST	0	W	0	0	0	0	1	0	0	1	09h	Read Display Status
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-	-
		1	R	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-	-
		1	R	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-	-
		1	R	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-	-
5	RDDPM	0	W	0	0	0	0	1	0	1	0	0Ah	Read Display Power Mode
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-
6	RDDMADCTR	0	W	0	0	0	0	1	0	1	1	0Bh	Read Display MADCTR
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-
7	RDDCOLMOD	0	W	0	0	0	0	1	1	0	0	0Ch	Read Display Pixel Format
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-
8	RDDIM	0	W	0	0	0	0	1	1	0	1	0Dh	Read Display Image Mode
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-
9	RDDSM	0	W	0	0	0	0	1	1	1	0	0Eh	Read Display Signal
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-
10	RDDSDR	0	W	0	0	0	0	1	1	1	1	0Fh	Read self-diagnotic
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	-

Table 6.1.2 Instruction Code (Continued)

NO	Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
11	SLPIN	0	W	0	0	0	1	0	0	0	0	10h	Sleep in & booster off
12	SLPOUT	0	W	0	0	0	1	0	0	0	1	11h	Sleep out & booster on
13	PTLON	0	W	0	0	0	1	0	0	1	0	12h	Partial mode on
14	NORON	0	W	0	0	0	1	0	0	1	1	13h	Partial off (Normal)
15	INVOFF	0	W	0	0	1	0	0	0	0	0	20h	Display inversion off (normal)
16	INVON	0	W	0	0	1	0	0	0	0	1	21h	Display inversion on
17	GMSET	0	W	0	0	1	0	0	1	1	0	26h	Gamma set
		1	W	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		
18	DISPOFF	0	W	0	0	1	0	1	0	0	0	28h	Display off
19	DISPON	0	W	0	0	1	0	1	0	0	1	29h	Display on
20	CASET	0	W	0	0	1	0	1	0	1	0	2Ah	Column address set
		1	W	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0 ≤XS ≤EFh ,MV='0'
		1	W	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	W	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: XS ≤XE ≤EFh ,MV='0'
		1	W	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
21	RASET	0	W	0	0	1	0	1	0	1	1	2Bh	Row address set
		1	W	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0 ≤YS ≤13Fh ,MV='0'
		1	W	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	W	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: YS ≤YE ≤13Fh ,MV='0'
		1	W	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
22	RAMWR	0	W	0	0	1	0	1	1	0	0	2Ch	Memory write
		1	W	D7	D6	D5	D4	D3	D2	D1	D0	-	Write data
23	RAMRD	0	W	0	0	1	0	1	1	1	0	2Eh	Memory read
		1	R	-	-	-	-	-	-	-	-	-	Dummy read
		1	R	D7	D6	D5	D4	D3	D2	D1	D0	-	Read data
24	RGBSET a = 31, b = 63, c = 31	0	W	0	0	1	0	1	1	0	1	2Dh	LUT for 4k and 65k color display
		1	W	R007	R006	R005	R004	R003	R002	R001	R000	-	Red tone 00000
		1	W	:	:	:	:	:	:	:	:	-	: -
		1	W	Ra7	Ra6	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0	-	Red tone 11111
		1	W	G007	G006	G005	G004	G003	G002	G001	G000	-	Green tone 000000
		1	W	:	:	:	:	:	:	:	:	-	: -
		1	W	Gb7	Gb6	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0	-	Green tone 111111
		1	W	B007	B006	B005	B004	B003	B002	B001	B000	-	Blue tone 00000
		1	W	:	:	:	:	:	:	:	:	-	: -
		1	W	Bc7	Bc6	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0	-	Blue tone 11111

Table 6.1.2 Instruction Code (Continued)

NO	Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
25	PTLAR	0	W	0	0	1	1	0	0	0	0	30h	Partial start/end address set
		1	W	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	Partial start address
		1	W	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
		1	W	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-	Partial end address
		1	W	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	
26	SCRLAR	0	W	0	0	1	1	0	0	1	1	33h	Scroll Area Set
		1	W	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-	Top Fixed Area
		1	W	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	
		1	W	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-	Vertical Scroll Area
		1	W	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-	
		1	W	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-	Bottom Fixed Area
		1	W	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-	
27	TEOFF	0	W	0	0	1	1	0	1	0	0	34h	Tearing effect line off
28	TEON	0	W	0	0	1	1	0	1	0	1	35h	Tearing effect mode set & on
		1	W	-	-	-	-	-	-	-	M	-	M="0": Mode1, M="1": Mode2
29	MADCTR	0	W	0	0	1	1	0	1	1	0	36h	Memory data access control
		1	W	MY	MX	MV	ML	RGB	MH	-	-	-	-
30	VSCSAD	0	W	0	0	1	1	0	1	1	1	37h	Scroll Start Address of RAM
		1	W	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	-	
		1	W	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	-	
31	IDMOFF	0	W	0	0	1	1	1	0	0	0	38h	Idle Mode Off
32	IDMON	0	W	0	0	1	1	1	0	0	1	39h	Idle Mode On
33	COLMOD	0	W	0	0	1	1	1	0	1	0	3Ah	Interface pixel format
		1	W	VIPF3	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	-	Interface format
34	RDID1	0	W	1	1	0	1	1	0	1	0	DAh	Read ID1
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	0	0	1	1	1	0	0	0	-	38h
35	RDID2	0	W	1	1	0	1	1	0	1	1	DBh	Read ID2
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	Read parameter
36	RDID3	0	W	1	1	0	1	1	1	0	0	DCh	Read ID3
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	Read parameter

6.1.2 NOP (00h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	W	0	0	0	0	0	0	0	0	00h
Parameter	No Parameter										

NOTE: "-" Don't care

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart -

6.1.3 SWRESET: Software Reset (01h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	0	W	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter										

NOTE: "-" Don't care

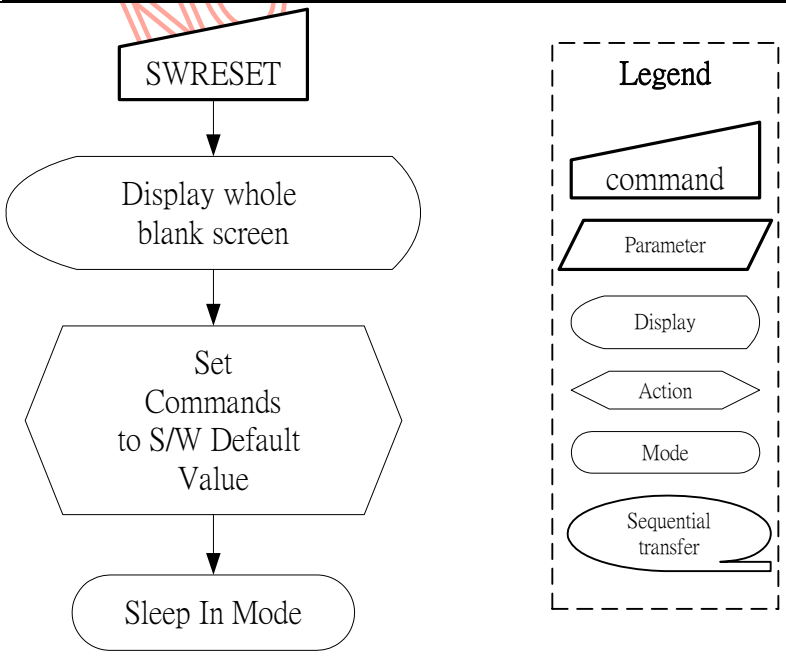
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to GND (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



6.1.4 RDDID: Read Display ID (04h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDID	0	W	0	0	0	0	0	1	0	0	04h
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	0	0	1	1	1	0	0	0	38h
2nd parameter	1	R	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
3rd parameter	1	R	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 24-bit display identification information.
The 1st parameter is dummy data
The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
The 3rd parameter (ID27 to ID20): LCD module/driver version ID.
The 4th parameter (ID37 to UD30): LCD module/driver ID.
NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

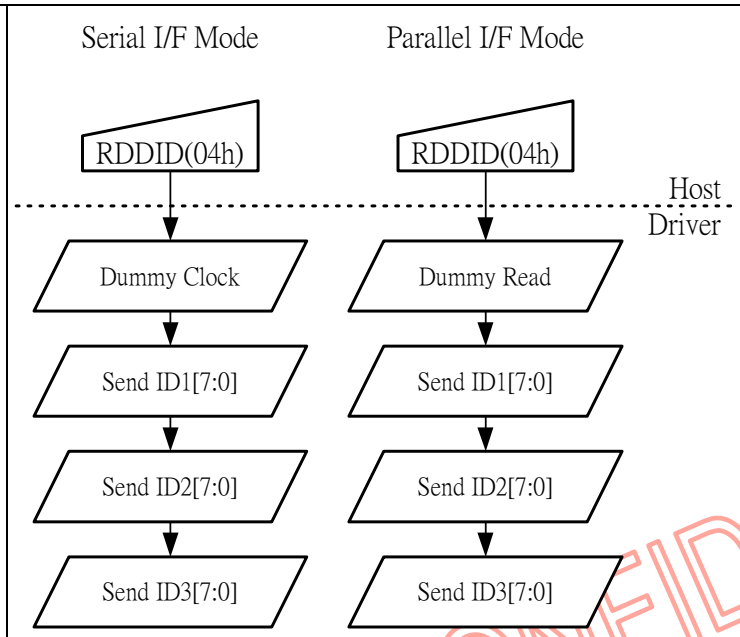
If ID2 and ID3 MTP are not yet programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	80h	00h
S/W Reset	38h	80h	00h
H/W Reset	38h	80h	00h

If ID2 and ID3 MTP were programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	(MTP value)	(MTP value)
S/W Reset	38h	(MTP value)	(MTP value)

Flow Chart



6.1.5 RDDST: Read Display Status (09h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	0	W	0	0	0	0	1	0	0	1	09h
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
2nd parameter	1	R	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
3rd parameter	1	R	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
4th parameter	1	R	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Exchange (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Vertical refresh Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Horizontal refresh Order (MH)	"1"=Decrement, "0"=Increment
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22-20	Interface Color Pixel Format Definition	"011" = 12-bit / pixel "101" = 16-bit / pixel, "110" = 18-bit / pixel
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On (Not Used)	"0"
ST11	All Pixels Off (Not Used)	"0"
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8-6	Gamma Curve Selection	"000" = GC1 "001" = GC2 "010" = GC3 "011" = GC4 "100" to "111" = Not defined
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"

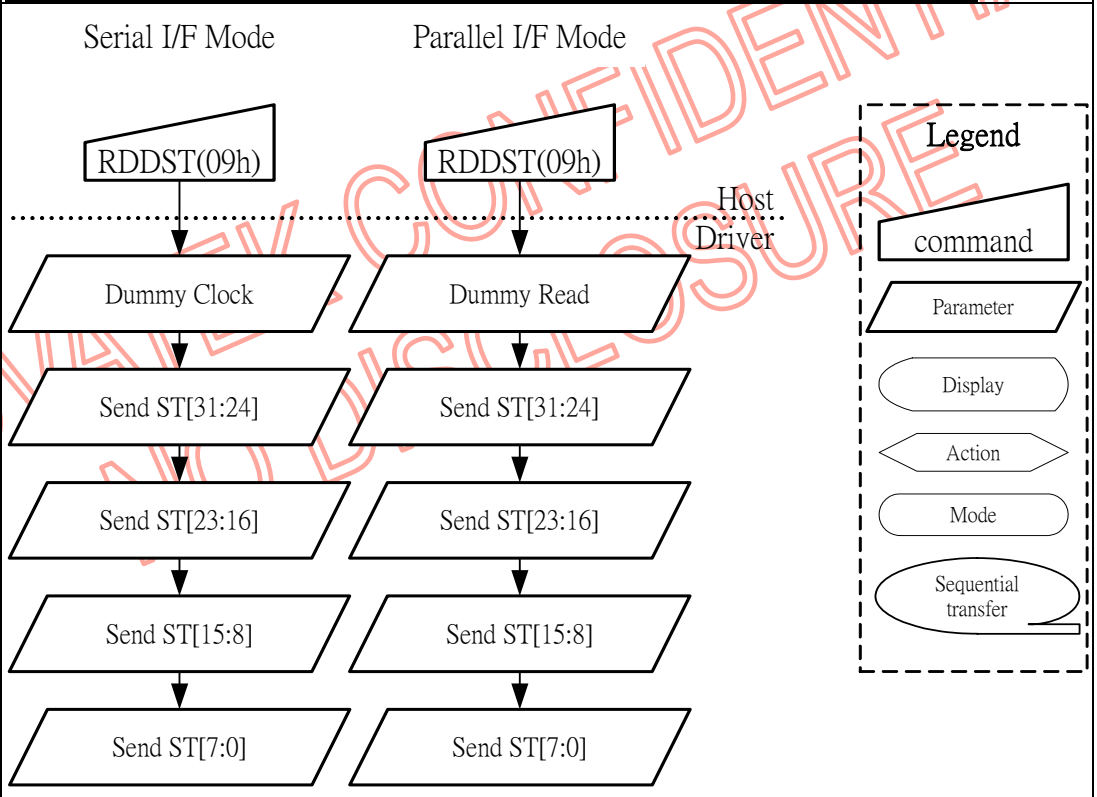
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0):
Power On Sequence	0000 0000_0110 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0110 0001_0000 0000_0000 0000

Flow Chart



6.1.6 RDDPM: Read Display Power Mode (0Ah)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDPM	0	W	0	0	0	0	1	0	1	0	0Ah
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	
D7	Booster Voltage Status	"1"=Booster on,	"0"=Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On,	"0"= Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On,	"0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out,	"0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display,	"0" = Partial Display
D2	Display On/Off	"1" = Display On,	"0" = Display Off
D1	Not Used	"0"	
D0	Not Used	"0"	

Restriction

-

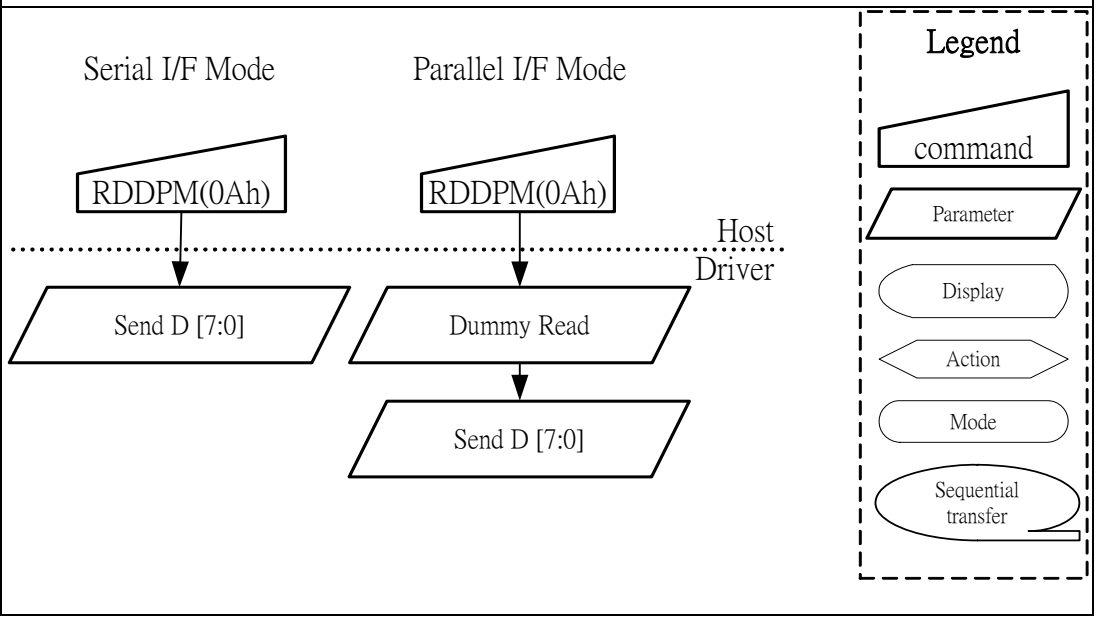
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)

Flow Chart



6.1.7 RDDMADCTR: Read Display MADCTR (0Bh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDMADCTR	0	W	0	0	0	0	1	0	1	1	0Bh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order	"1"=Decrement, "0"=Increment
D6	Column Address Order	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Vertical fresh Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Horizontal fresh Order (MH)	"1"=Decrement, "0"=Increment
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

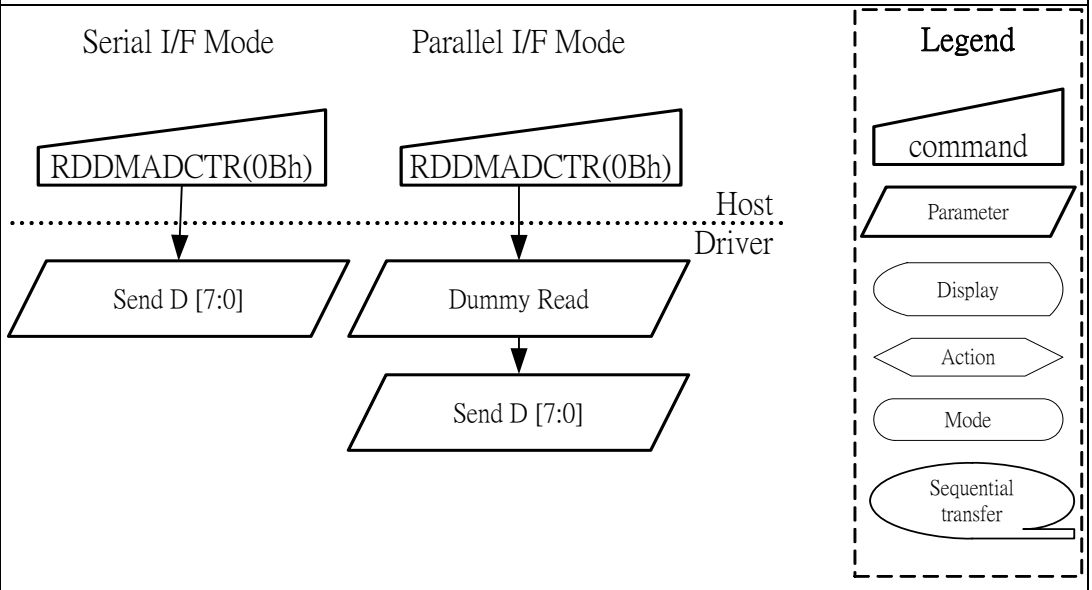
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change

Flow Chart



6.1.8 RDDCOLMOD: Read Display Pixel Format (0Ch)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDCOLMOD	0	W	0	0	0	0	1	1	0	0	0Ch
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Not Used	"0"
D4	Not Used	"0"
D3	Not Used	"0"
D2-0	Control Interface Color Format	"011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel The others = not defined

Restriction

-

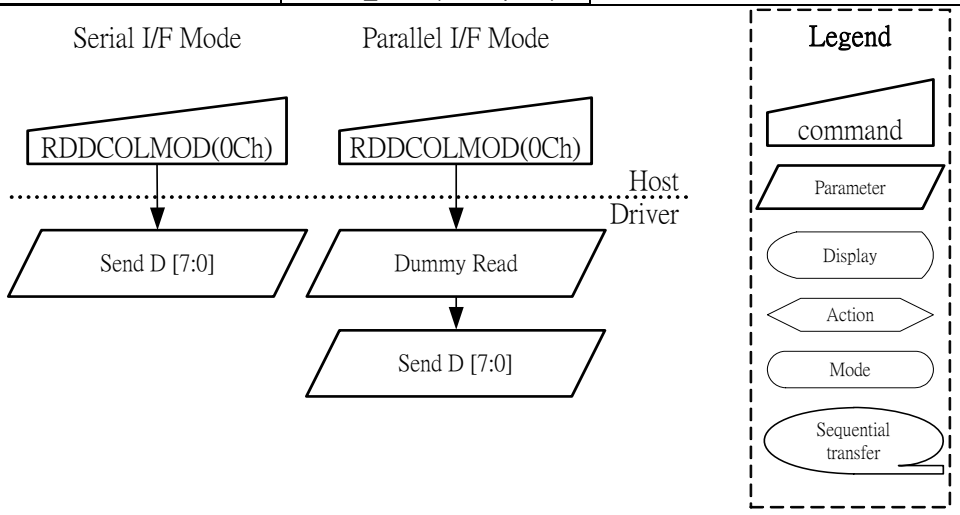
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000_0110 (18 bit/pixel)
S/W Reset	No Change
H/W Reset	0000_0110 (18 bit/pixel)

Flow Chart



6.1.9 RDDIM: Read Display Image Mode (0Dh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDIM	0	W	0	0	0	0	1	1	0	1	0Dh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
D5	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
D2 -0	Gamma Curve Selection	"000" = GC1 "001" = GC2 "010" = GC3 "011" = GC4 "100" to "111" = Not defined

Restriction

-

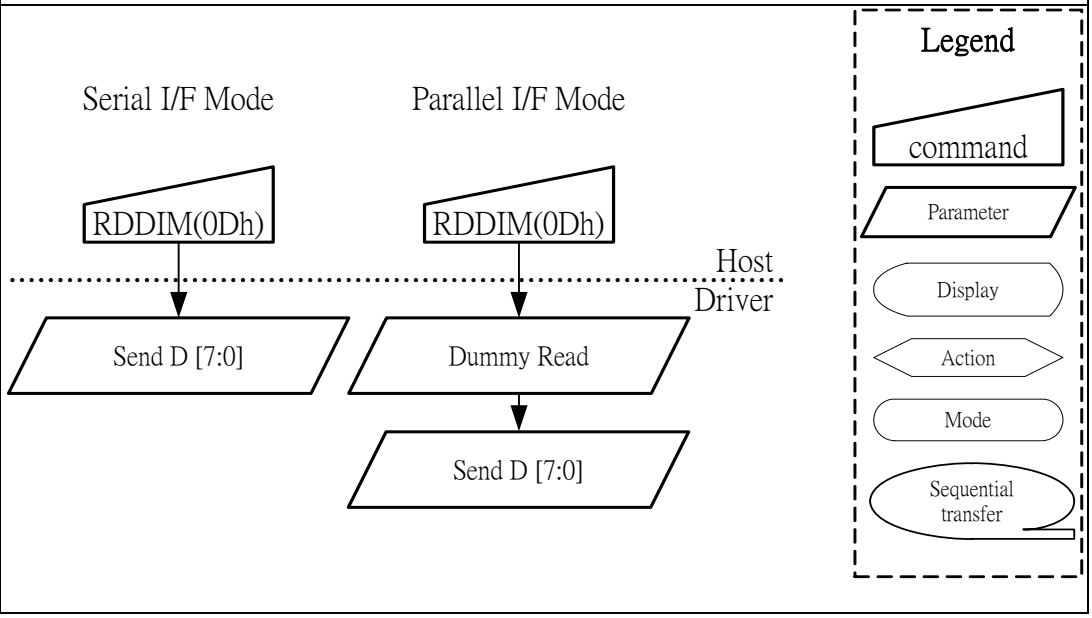
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



6.1.10 RDDSM: Read Display Signal Mode (0Eh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSM	0	W	0	0	0	0	1	1	1	0	0Eh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing effect line mode	"0" = mode1, "1" = mode2
D5	Horizontal Sync. (RGB I/F)On/Off	"0"
D4	Vertical Sync. (RGB I/F)On/Off	"0"
D3	Pixel Clock (PCLK, RGB I/F)On/Off	"0"
D2	Data Enable (DE, RGB I/F)On/Off	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

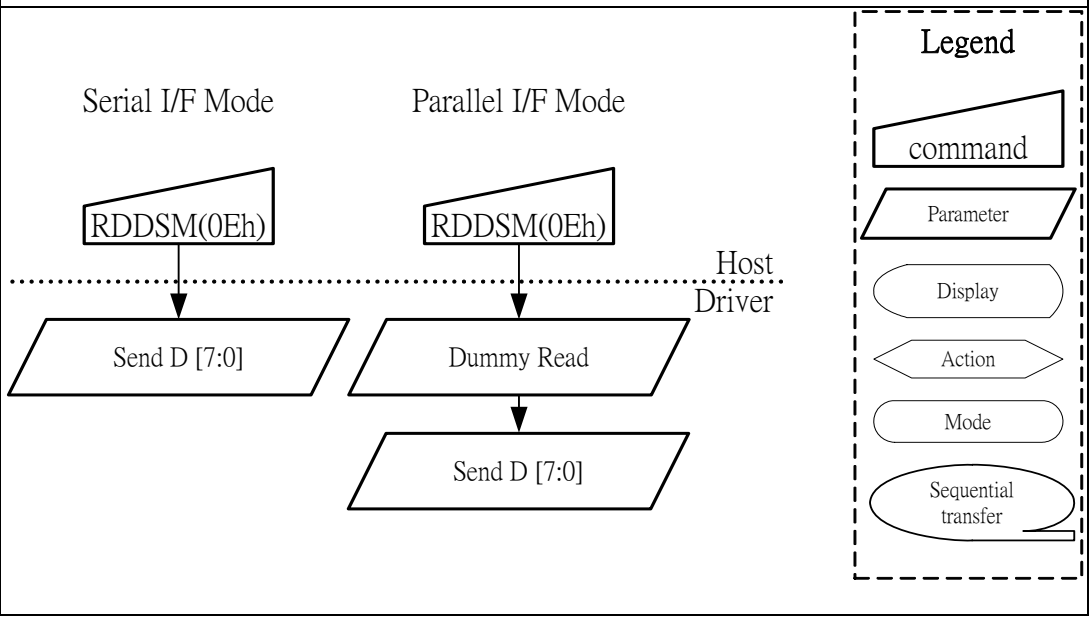
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



6.1.11 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSDR	0	W	0	0	0	0	1	1	1	1	0Fh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

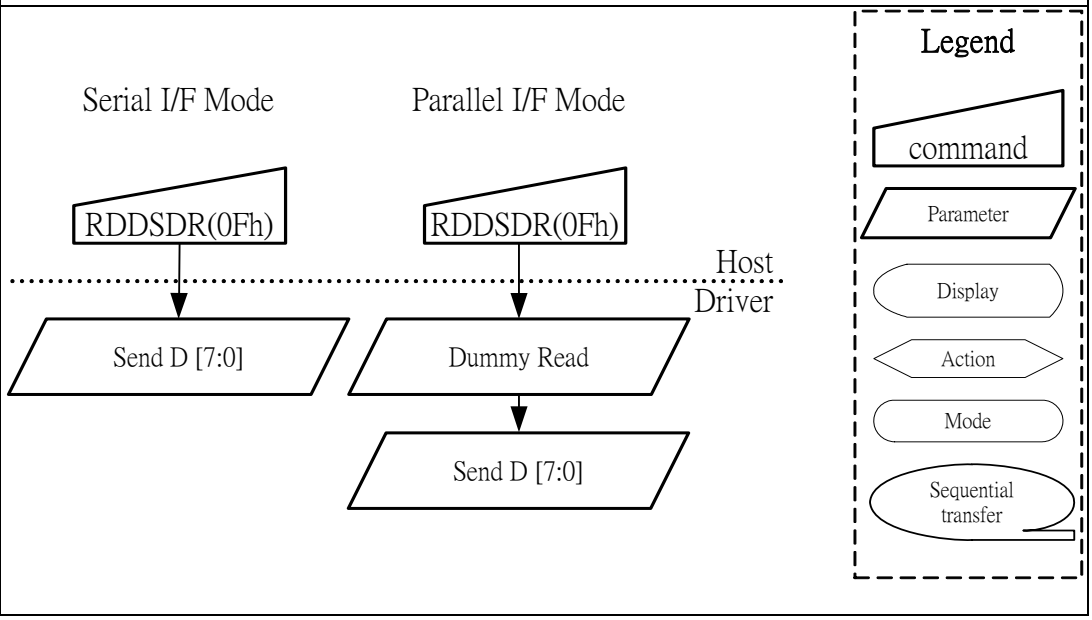
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



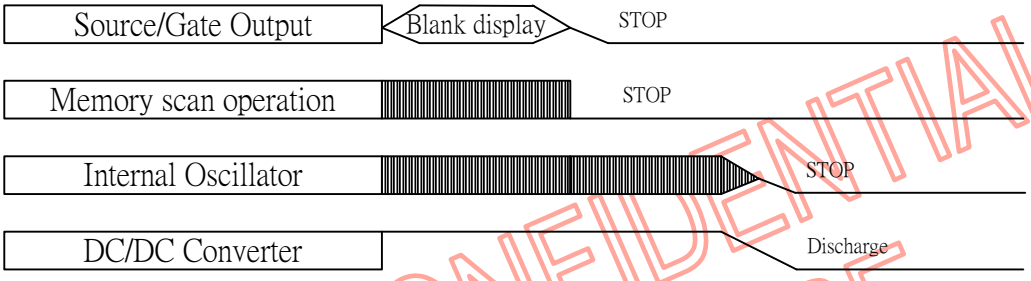
6.1.12 SLPIN: Sleep In (10h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	0	W	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



MPU interface and memory are still working and the memory keeps its contents.

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

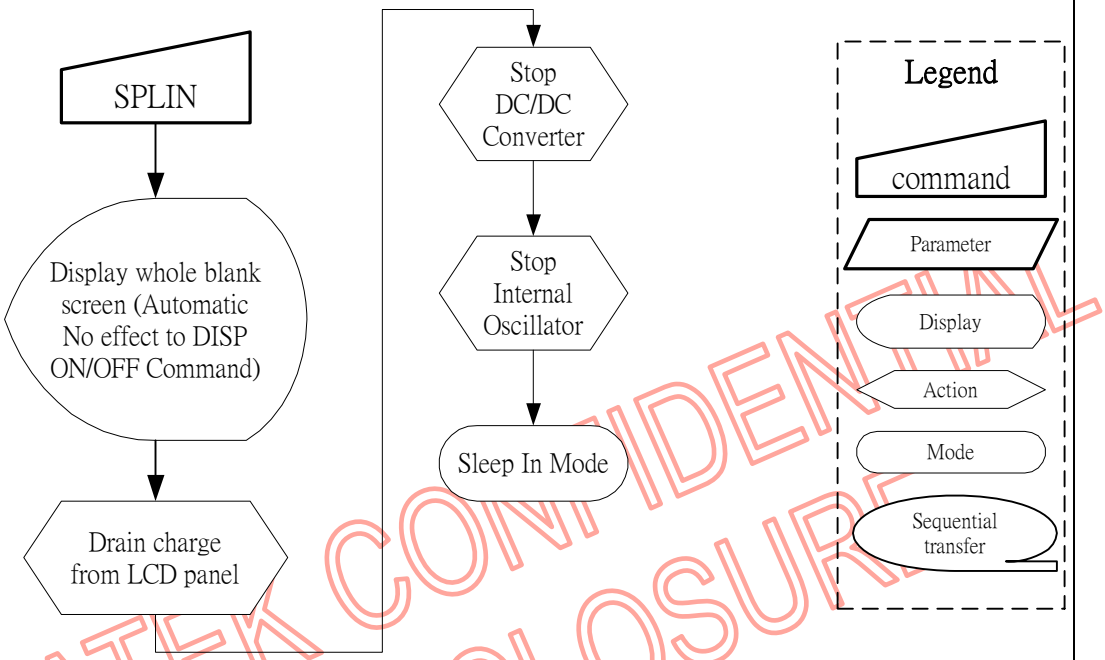
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31.



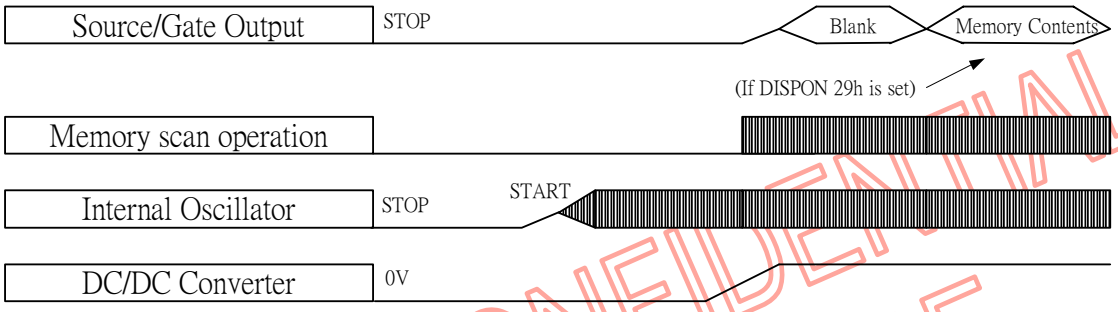
6.1.13 SLPOUT: Sleep Out (11h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	0	W	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
NT39125 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT39125 is already Sleep Out –mode.

Register Availability

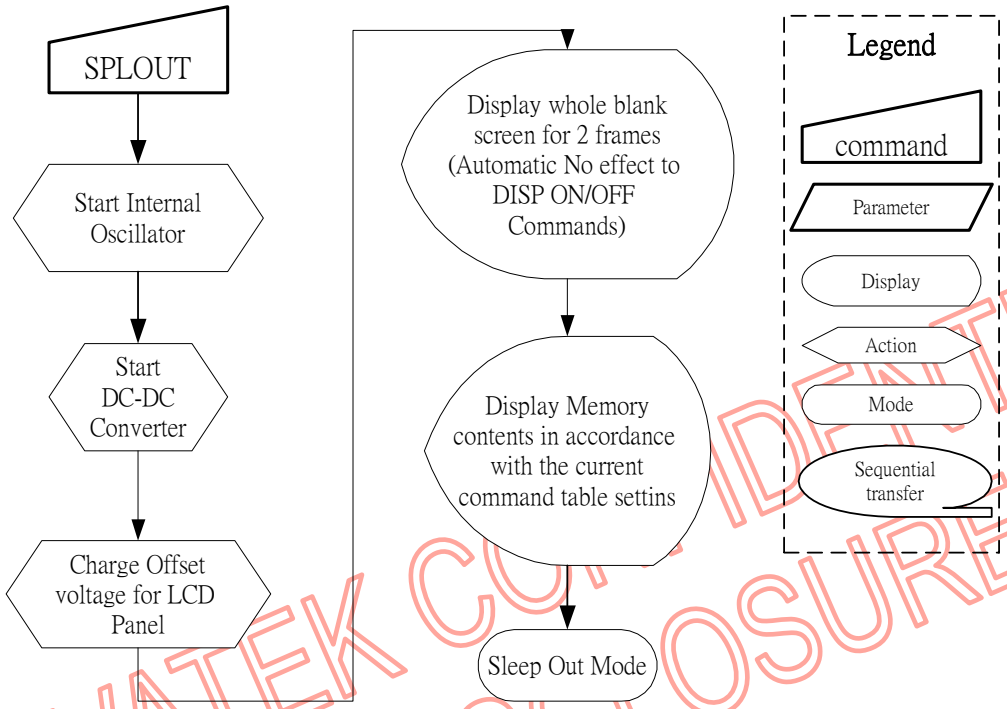
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart

It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued.
The results of booster on can be checked by RDDST (09h) command Bit31.



6.1.14 PTLON: Partial Display Mode On (12h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLON	0	W	0	0	0	1	0	0	1	0	12h
Parameter	No Parameter										

NOTE: "-" Don't care

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart: See Partial Area (30h)

6.1.15 NORON: Normal Display Mode On (13h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	0	W	0	0	0	1	0	0	1	1	13h
Parameter	No Parameter										

NOTE: "-" Don't care

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

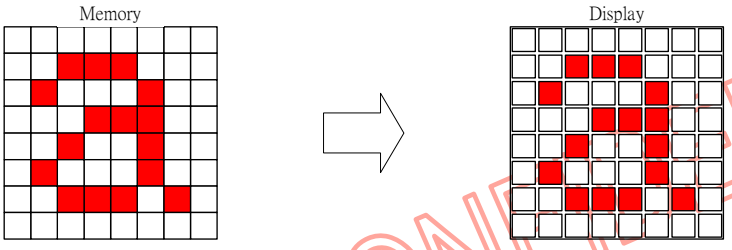
6.1.16 INVOFF: Display Inversion Off (20h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	0	W	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already inversion off mode.

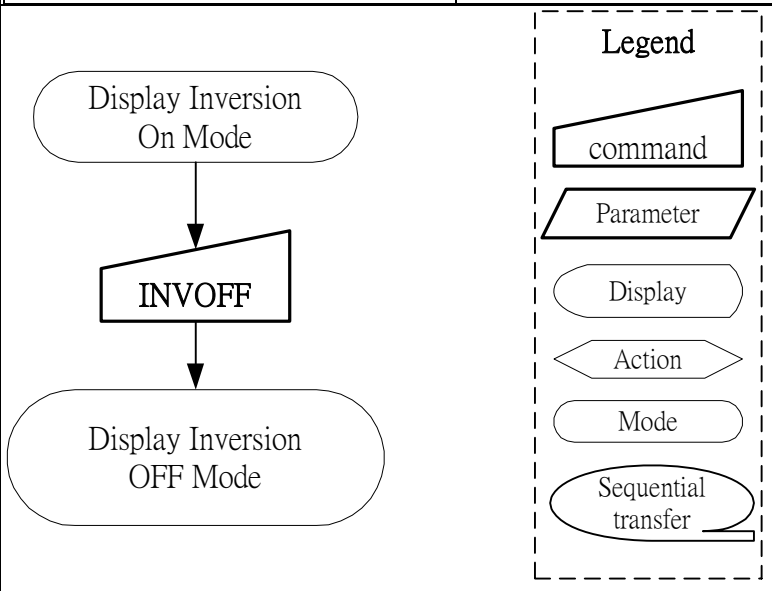
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



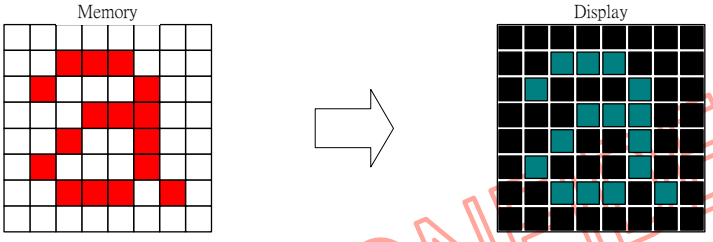
6.1.17 INVON: Display Inversion On (21h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVON	0	W	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to enter display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.



(Example)

Restriction

This command has no effect when module is already Inversion On mode.

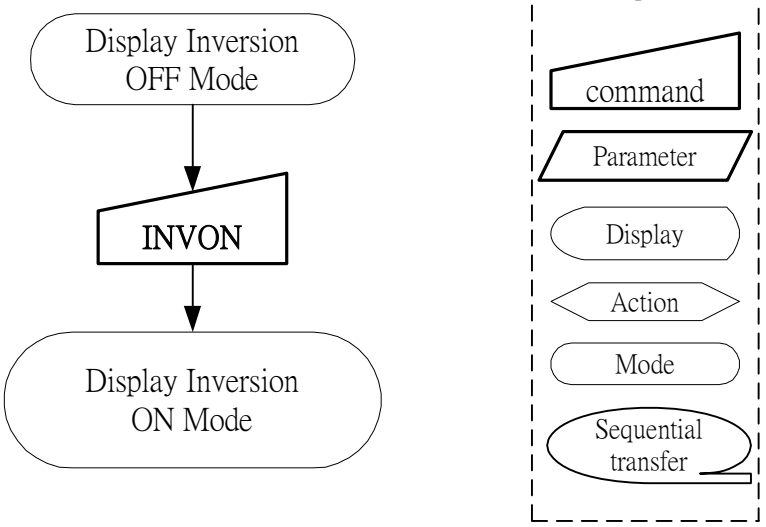
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.1.18 GAMSET: Gamma Set (26h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GAMSET	0	W	0	0	1	0	0	1	1	0	26h
Parameter	1	W	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

NOTE: "-" Don't care

Description

This command is used to select the desired Gamma curve for the current display. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (Gamma 2.2)
02h	GC1	Gamma Curve 2 (Gamma 1.8)
04h	GC2	Gamma Curve 3 (Gamma 2.5)
08h	GC3	Gamma Curve 4 (Gamma 1.0)

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

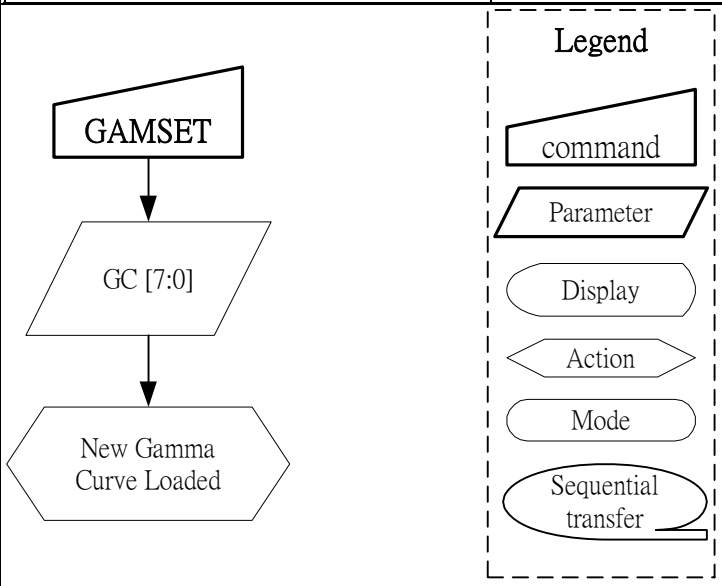
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



6.1.19 DISPOFF: Display Off (28h)

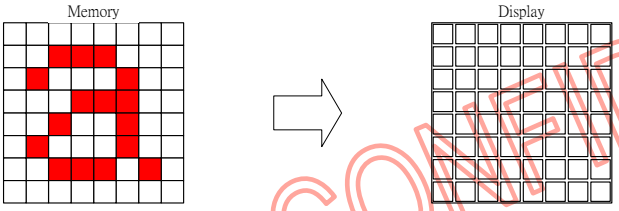
Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	0	W	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h)

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

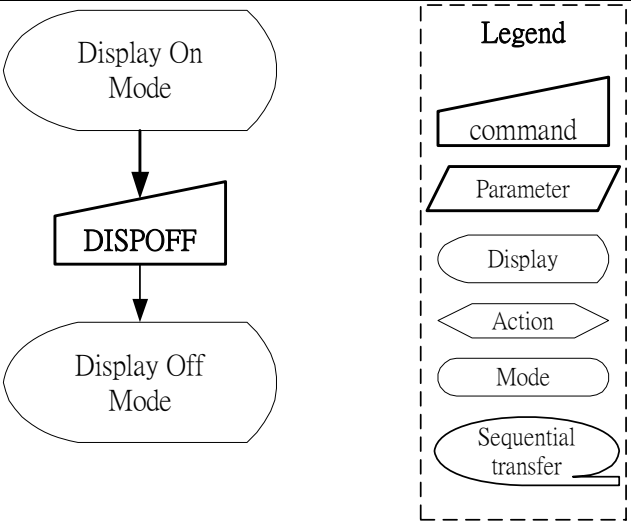
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



6.1.20 DISPON: Display On (29h)

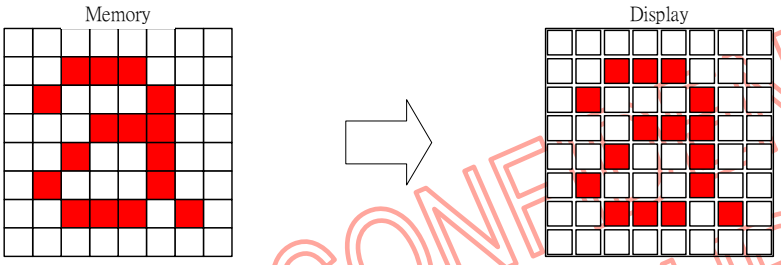
Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	0	W	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in Display On mode.

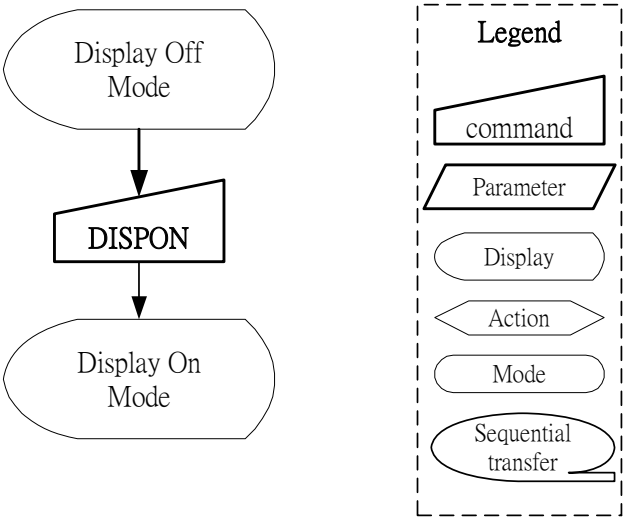
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



6.1.21 CASET: Column Address Set (2Ah)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CASET	0	W	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	W	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-
2nd parameter	1	W	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3rd parameter	1	W	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4th parameter	1	W	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

NOTE: "-" Don't care

Description

This command is used to define area of frame memory where MPU can access.
This command makes no change on the other driver status.
The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

Restriction

XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

For GM = "00" (240x432 display resolution)
When MV="0", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 239 (00EFh)
When MV="1", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 431 (01AFh)

For GM = "01" (240x400 display resolution)
When MV="0", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 239 (00EFh)
When MV="1", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 399 (018Fh)

For GM = "10" (240x320 display resolution)
When MV="0", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 239 (00EFh)
When MV="1", parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦ 319 (013Fh)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For GM = "00" (240x432 display resolution)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00EFh (239d)	
S/W Reset	0000h	00EFh (239d)	01AFh (431d)
H/W Reset	0000h	00EFh (239d)	

For GM = "01" (240x400 display resolution)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00EFh (239d)	
S/W Reset	0000h	00EFh (239d)	018Fh (399d)
H/W Reset	0000h	00EFh (239d)	

<table>
<tr><td></td><td>
For GM = “10” (240x320 display resolution)
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>XS [15:0]</th><th>XE [15:0] (MV=0)</th><th>XE [15:0] (MV=1)</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">00EFh (239d)</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>00EFh (239d)</td><td>013Fh (319d)</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td colspan="2">00EFh (239d)</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

6.1.22 RASET: Row Address Set (2Bh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RASET	0	W	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	W	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2nd parameter	1	W	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3rd parameter	1	W	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4th parameter	1	W	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

NOTE: "-" Don't care

Description

This command is used to define area of frame memory where MPU can access.
This command makes no change on the other driver status.
The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

Restriction

YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

For GM = "00" (240x432 display resolution)
When MV="0", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 431 (01AFh)
When MV="1", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 239 (00EFh)

For GM = "01" (240x400 display resolution)
When MV="0", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 399 (018Fh)
When MV="1", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 239 (00EFh)

For GM = "10" (240x320 display resolution)
When MV="0", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 319 (013Fh)
When MV="1", parameter range: 0 ≦ YS [15:0] ≦ YE [15:0] ≦ 239 (00EFh)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For GM = "00" (240x432 display resolution)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	01AFh (431d)	
S/W Reset	0000h	01AFh (431d)	00EFh (239d)
H/W Reset	0000h	01AFh (431d)	

For GM = "01" (240x400 display resolution)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	018Fh (399d)	
S/W Reset	0000h	018Fh (399d)	00EFh (239d)
H/W Reset	0000h	018Fh (399d)	

<table>
<tr><td></td><td>
For GM = “10” (240x320 display resolution)
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>YS [15:0]</th><th>YE [15:0] (MV=0)</th><th>YE [15:0] (MV=1)</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">013Fh (319d)</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>013Fh (319d)</td><td>00EFh (239d)</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td colspan="2">013Fh (319d)</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

6.1.23 RAMWR: Memory Write (2Ch)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	D[9:0]	Hex
RAMWR	0	W	0	0	1	0	1	1	0	0	-	2Ch
1st parameter	1	W	D1[17]	D1[16]	D1[15]	D1[14]	D1[13]	D1[12]	D1[11]	D1[10]	D1[9:0]	-
:	1	W	Dx[17]	Dx[16]	Dx[15]	Dx[14]	Dx[13]	Dx[12]	Dx[11]	Dx[10]	Dx[9:0]	-
Nth parameter	1	W	Dn[17]	Dn[16]	Dn[15]	Dn[14]	Dn[13]	Dn[12]	Dn[11]	Dn[10]	Dn[9:0]	-

NOTE: "-" Don't care

Description

This command is used to transfer data from MPU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting. (See 5.2.3)
Then D[17:0] is stored in frame memory and the column register and the row register incremented as in ***Fig 5.2.2***.
Sending any other command can stop Frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart

-

6.1.24 RAMRD: Memory Read (2Eh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	D[9:0]	Hex
RAMRD	0	W	0	0	1	0	1	1	1	0	-	2Eh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-	-
1st parameter	1	R	D1[17]	D1[16]	D1[15]	D1[14]	D1[13]	D1[12]	D1[11]	D1[10]	D1[9:0]	-
:	1	R	Dx[17]	Dx[16]	Dx[15]	Dx[14]	Dx[13]	Dx[12]	Dx[11]	Dx[10]	Dx[9:0]	-
Nth parameter	1	R	Dn[17]	Dn[16]	Dn[15]	Dn[14]	Dn[13]	Dn[12]	Dn[11]	Dn[10]	Dn[9:0]	-

NOTE: "-" Don't care

Description

This command is used to transfer data from frame memory to MPU.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 5.2.3)
Then D[17:0] is read back from the frame memory and the column register and the row register incremented as in Fig. 5.2.2.
Frame Read can be canceled by sending any other command.
See section 5.2.1 "Display Data Format" for color coding (18 bit cases), when there is used 8, 9, 16 or 18 data lines for image data.

Restriction

In all color modes, the Frame Read is always 18-bit and there is no restriction on length of parameters.
Note – Memory Read is only possible via the Parallel Interface.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart

6.1.25 RGBSET: Color Set for 65k or 4k-Color Display (2Dh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGBSET	0	W	0	0	1	0	1	1	0	1	2Dh
1st parameter	1	W	R007	R006	R005	R004	R003	R002	R001	R000	-
:	1	W	:	:	:	:	:	:	:	:	-
32th parameter	1	W	Ra7	Ra6	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0	-
33th parameter	1	W	G007	G006	G005	G004	G003	G002	G001	G000	-
:	1	W	:	:	:	:	:	:	:	:	-
96th parameter	1	W	Gb7	Gb6	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0	-
97th parameter	1	W	B007	B006	B005	B004	B003	B002	B001	B000	-
:	1	W	:	:	:	:	:	:	:	:	-
128th parameter	1	W	Bc7	Bc6	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0	-

NOTE: "-" Don't care

NOTE: a = 31, b = 63, c = 31

Description

This command is used to define the LUT for 12-bit-to-18bit / 16bit-to-18bit color depth conversations. 128-Bytes must be written to the LUT regardless of the color mode. Only the values in section 5.2.8 are referred.

262k-color used, LUT has R00[7:0] ~ R31[7:0] and G00[7:0] ~ G63[7:0], B00[7:0] ~ B31[7:0],. Set total through 128th parameter.

In this condition, 4K-color (4-4-4), 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.

This command has no effect on other commands/parameters and Contents of frame memory.

Visible change takes effect next time the Frame Memory is written to.

Restriction

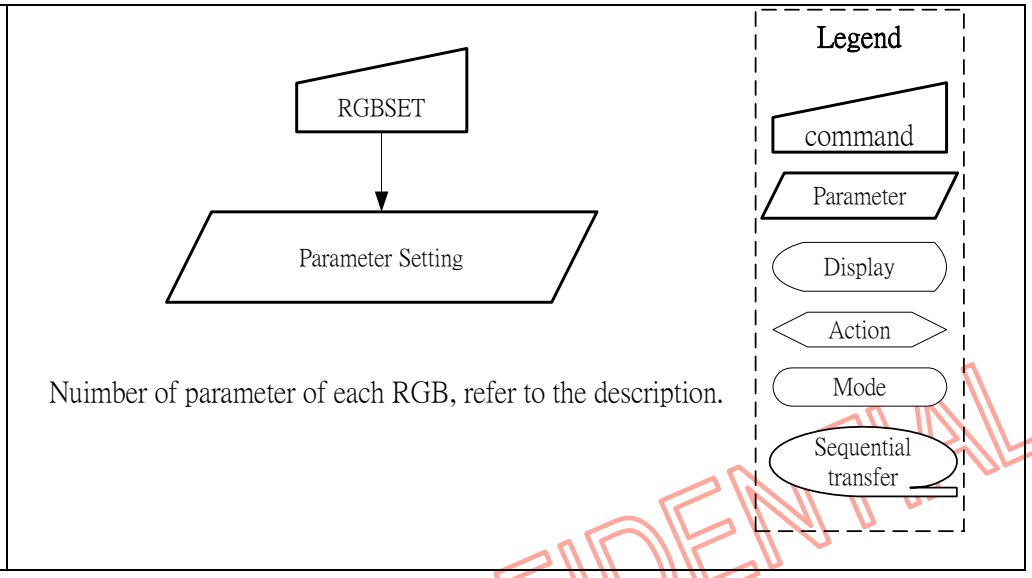
Do not send any command before the last data is sent or LUT is not defined correctly.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See section 5.2.8
S/W Reset	Contents of the look-up table protected

Flow Chart	

6.1.26 PTLAR: Partial Area (30h)

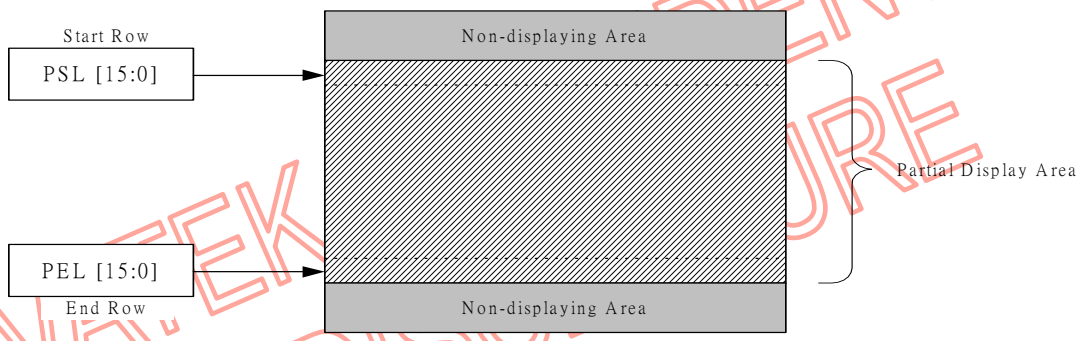
Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLAR	0	W	0	0	1	1	0	0	0	0	30h
1st parameter	1	W	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2nd parameter	1	W	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3rd parameter	1	W	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4th parameter	1	W	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

NOTE: "-" Don't care

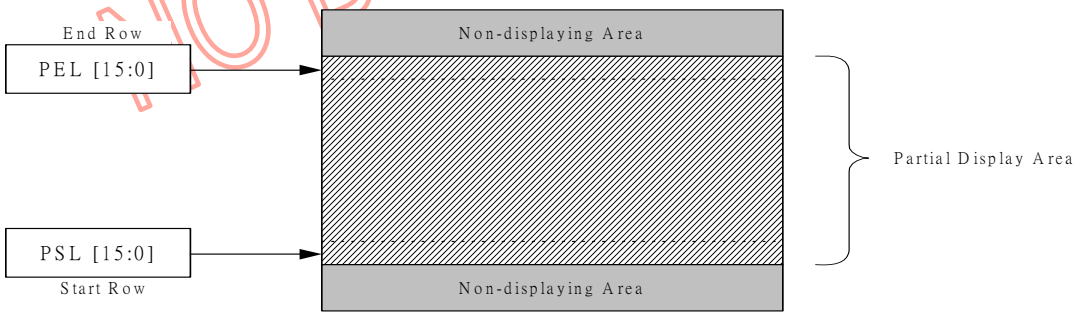
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

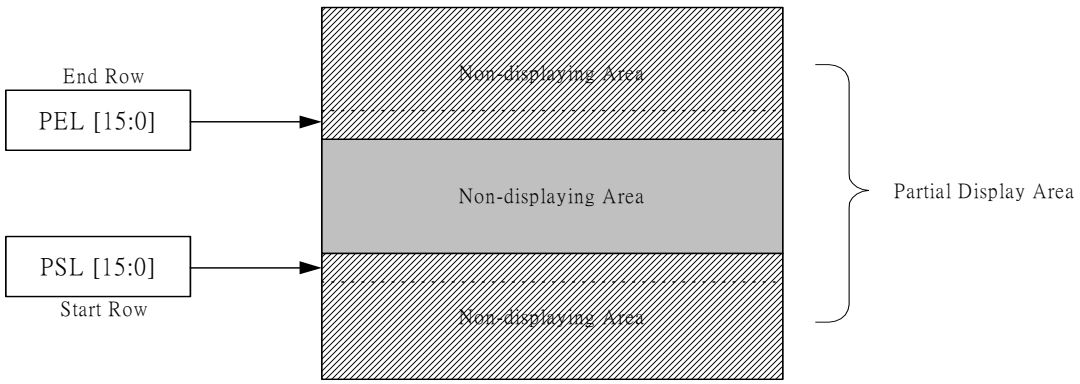
If End Row > Start Row when MADCTL ML=0:



If End Row > Start Row when MADCTL ML=1:



If End Row < Start Row when MADCTL ML=0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction

For GM = “00” (240x432 display resolution)
PSL[15:0] and PEL[15:0] should have below range
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 431 (01AFh))

For GM = “01” (240x400 display resolution)
PSL[15:0] and PEL[15:0] should have below range
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 399 (018Fh))

For GM = “10” (240x320 display resolution)
PSL[15:0] and PEL[15:0] should have below range
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 319 (013Fh))

Register Availability

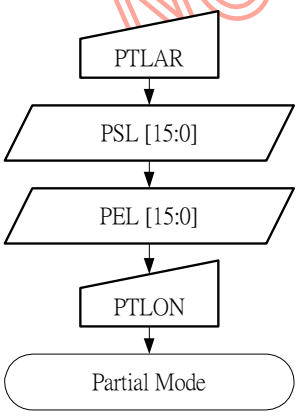
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

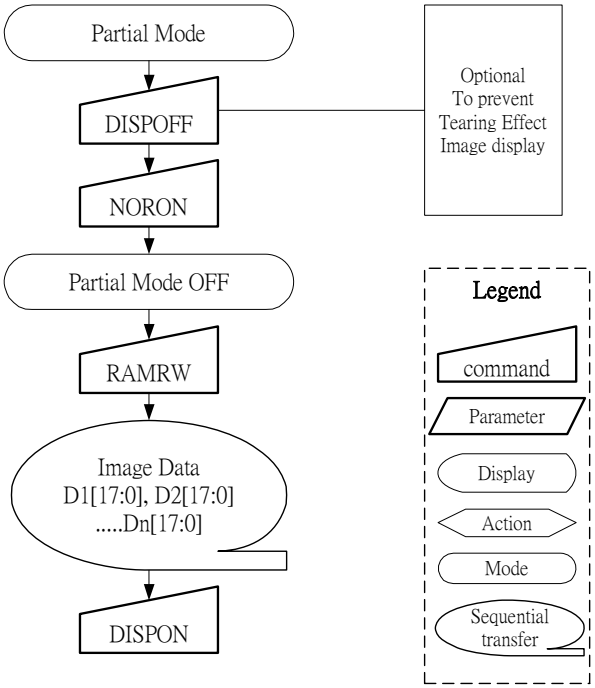
Status	Default Value			
	PSL[15:0]	PEL[15:0]		
		GM=”00”	GM=”01”	GM=”10”
Power On Sequence	0000h	1AFh	018Fh	13Fh
S/W Reset	0000h	1AFh	018Fh	13Fh
H/W Reset	0000h	1AFh	018Fh	13Fh

Flow Chart

1. To Enter Partial Mode



2. To Exit Partial Mode



6.1.27 SCRLAR: Scroll Area (33h)

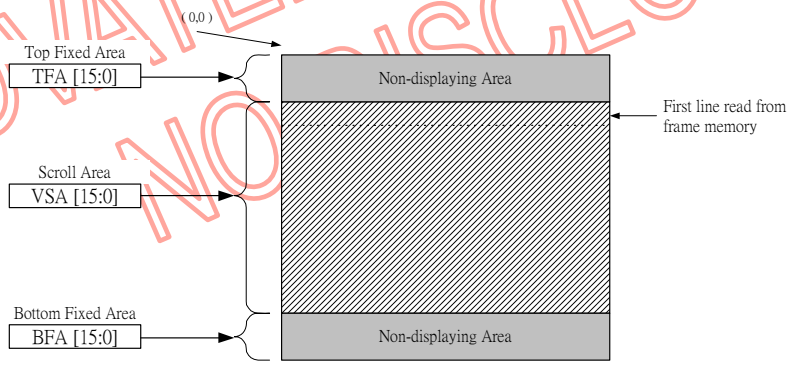
Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SCRLAR	0	W	0	0	1	1	0	0	1	1	33h
1st parameter	1	W	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-
2nd parameter	1	W	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
3rd parameter	1	W	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-
4th parameter	1	W	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
5th parameter	1	W	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-
6th parameter	1	W	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: "-" Don't care

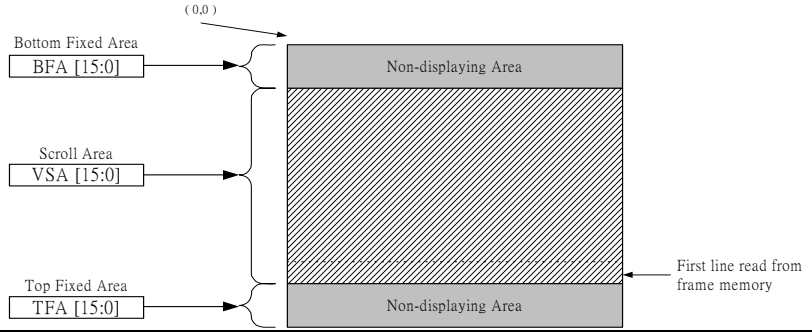
Description

This command defines the Vertical Scrolling Area of the display.

When MADCTL ML=0
TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
The first line appears immediately after the bottom most line of the Top Fixed Area.
BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory row address.



When MADCTL ML=1
TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
The first line appears immediately after the top most line of the Top Fixed Area.
BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



<table>
<tr><td></td><td>See Section 5.2.6 for details of the Memory to Display Mapping.</td></tr>
<tr><td>Restriction</td><td>For GM = “00” (240x432 display resolution)
The condition is (TFA+VSA+BFA) = 432, otherwise Scrolling mode is undefined.

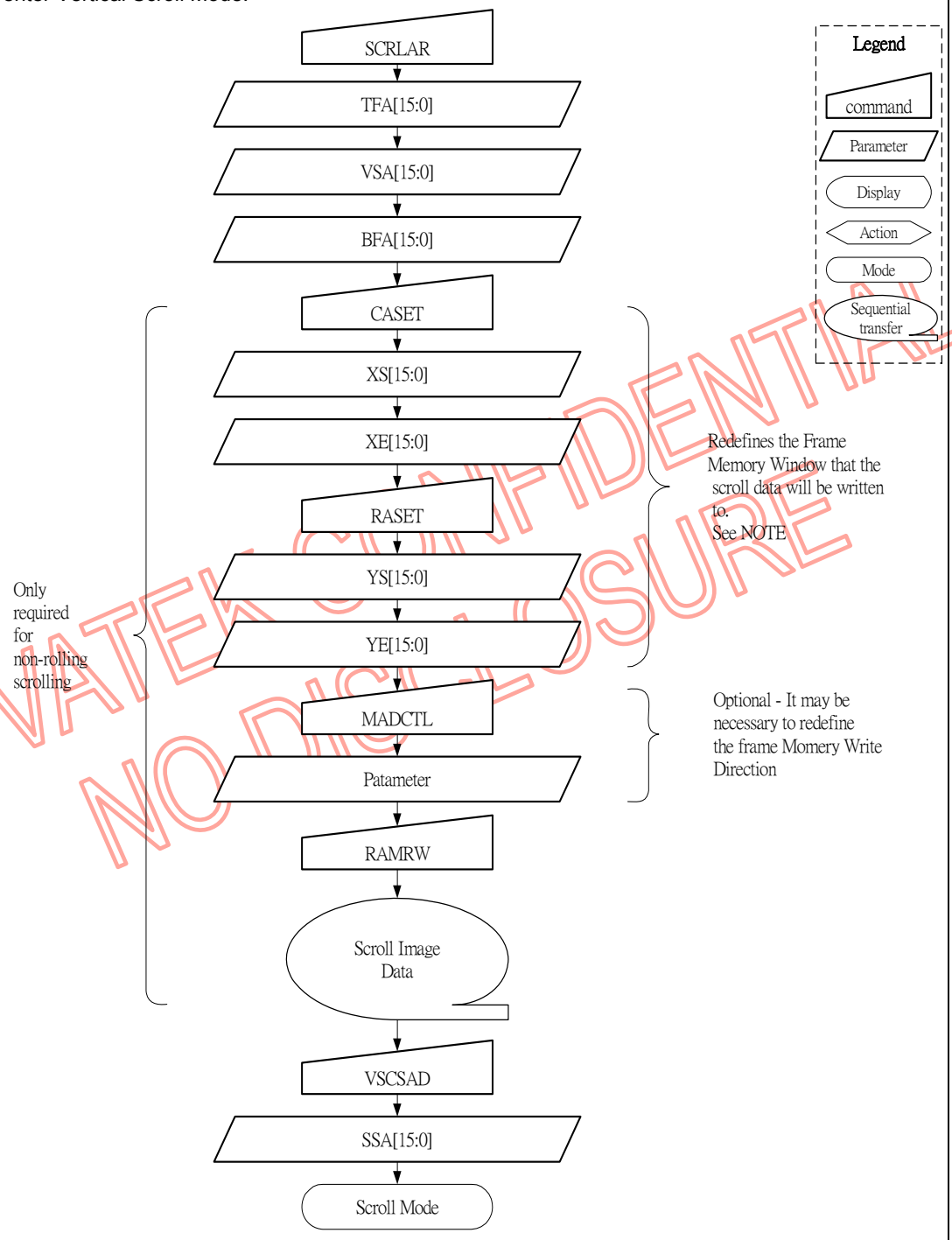
For GM = “01” (240x400 display resolution)
The condition is (TFA+VSA+BFA) = 400, otherwise Scrolling mode is undefined.

For GM = “10” (240x320 display resolution)
The condition is (TFA+VSA+BFA) = 320, otherwise Scrolling mode is undefined.

In Vertical Scroll Mode, MADCTL parameter MV should be set to ‘0’-this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>For GM = “00” (240x432 display resolution)
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>01B0h</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>01B0h</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>01B0h</td><td>0000h</td></tr>
</table>
For GM = “01” (240x400 display resolution)
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>0190h</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>0190h</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>0190h</td><td>0000h</td></tr>
</table>
For GM = “10” (240x320 display resolution)
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>0140h</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>0140h</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>0140h</td><td>0000h</td></tr>
</table>
</td></tr>
</table>

Flow Chart

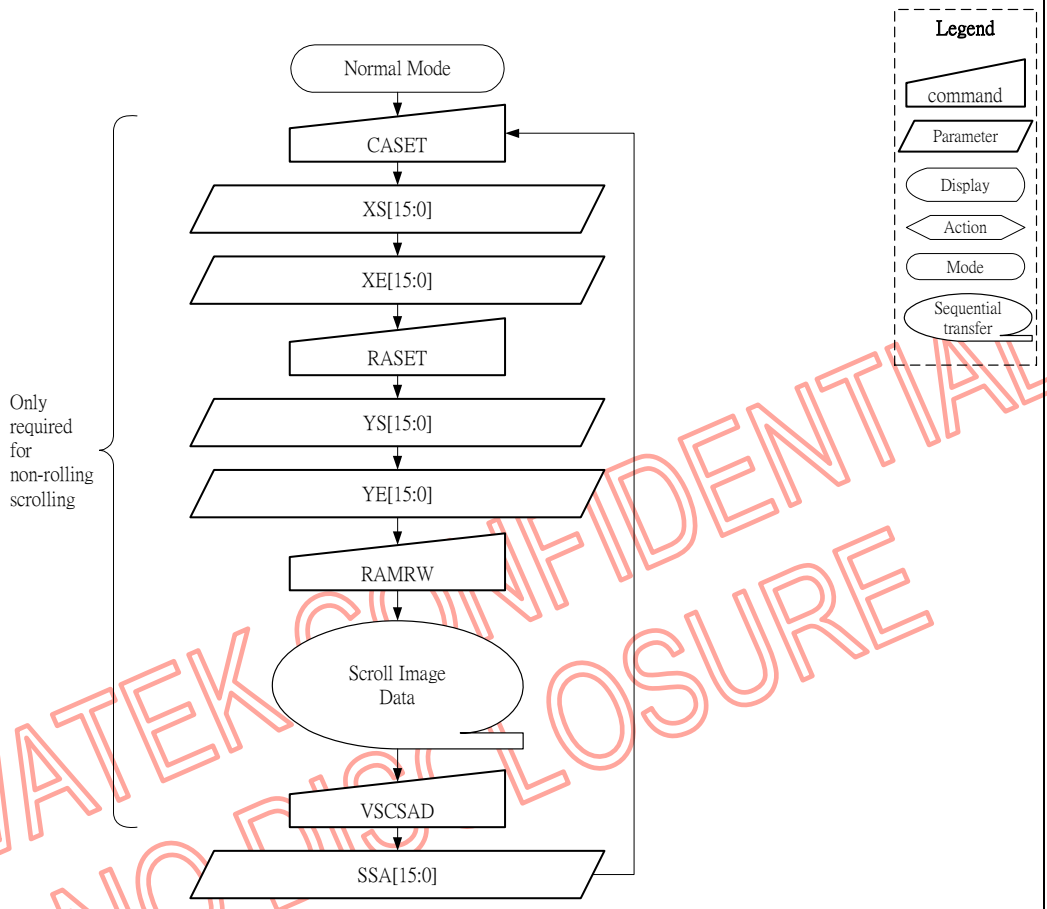
1.To enter Vertical Scroll Mode:



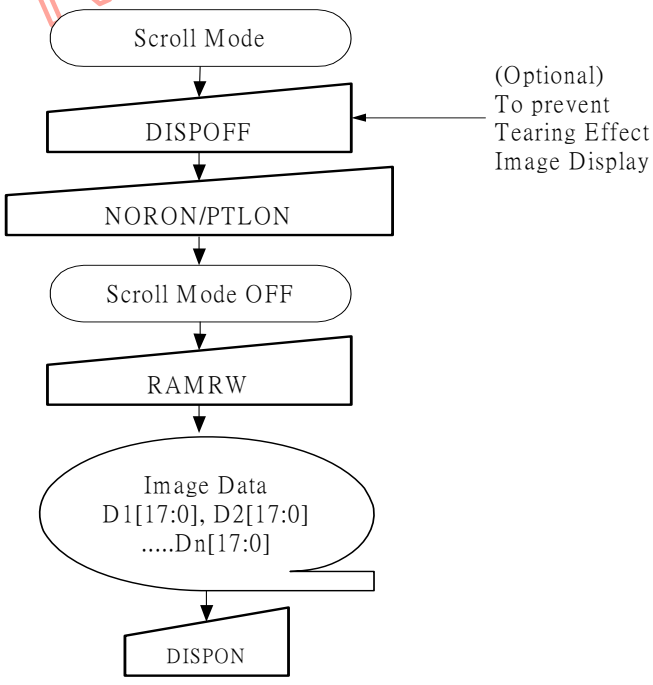
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

6.1.28 TEOFF: Tearing Effect Line OFF (34h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEOFF	0	W	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.

Restriction

This command has no effect when Tearing Effect output is already OFF.

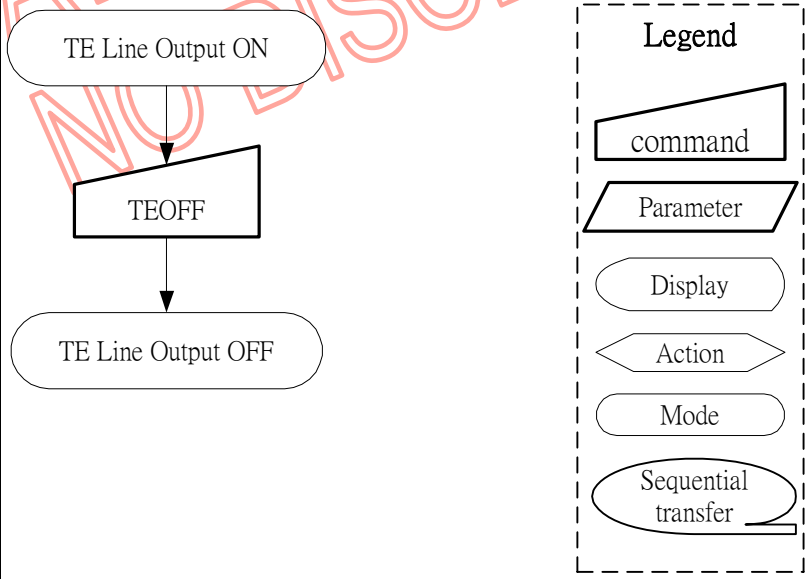
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



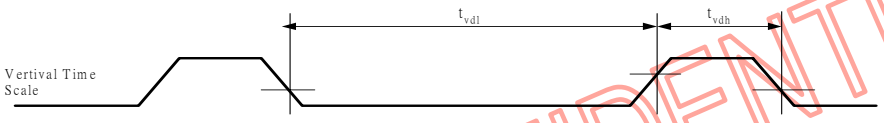
6.1.29 TEON: Tearing Effect Line ON (35h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEON	0	W	0	0	1	1	0	1	0	1	35h
Parameter	1	W	-	-	-	-	-	-	-	M	-

NOTE: "-" Don't care

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).
When M=0: The Tearing Effect Output line consists of V-Blanking information only.



When M=1: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.

See Section 5.2.7 for more information.
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already OFF.

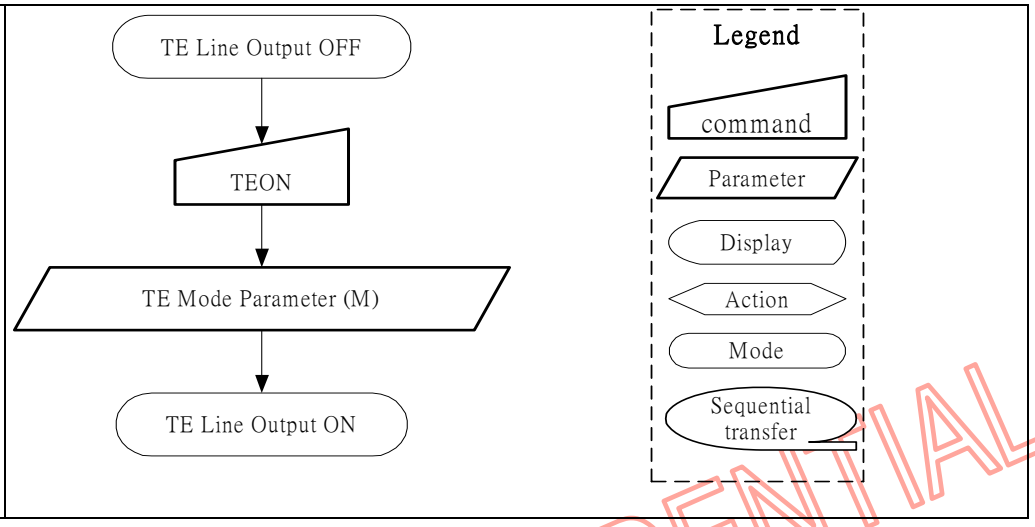
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



6.1.30 MADCTL: Memory Data Access Control (36h)

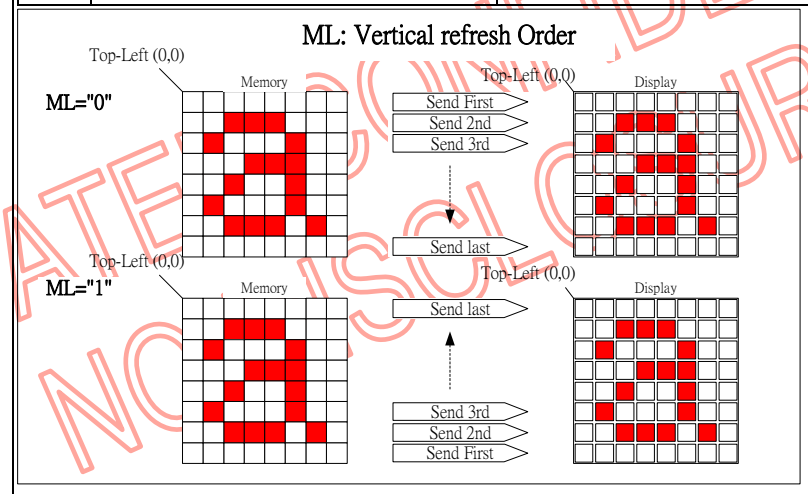
Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTR	0	W	0	0	1	1	0	1	1	0	36h
Parameter	1	W	MY	MX	MV	ML	RGB	MH	-	-	-

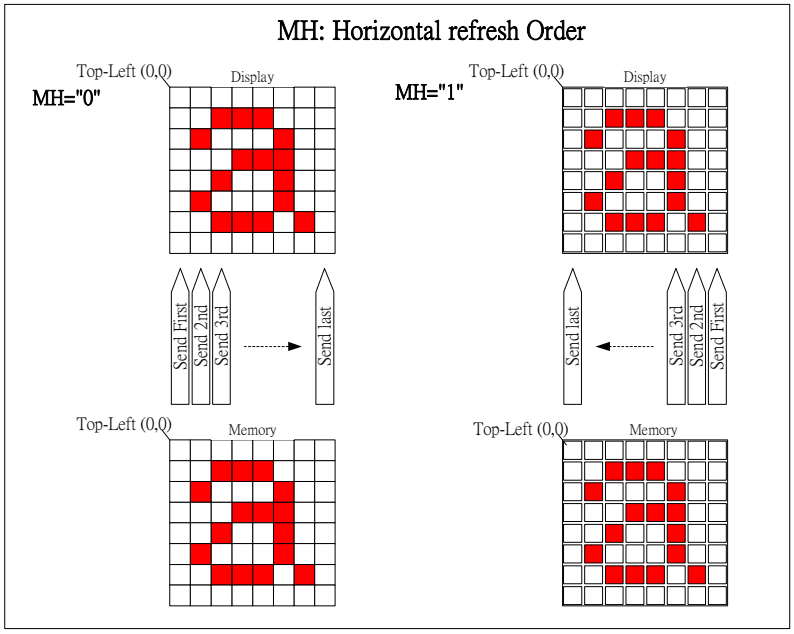
NOTE: "-" Don't care

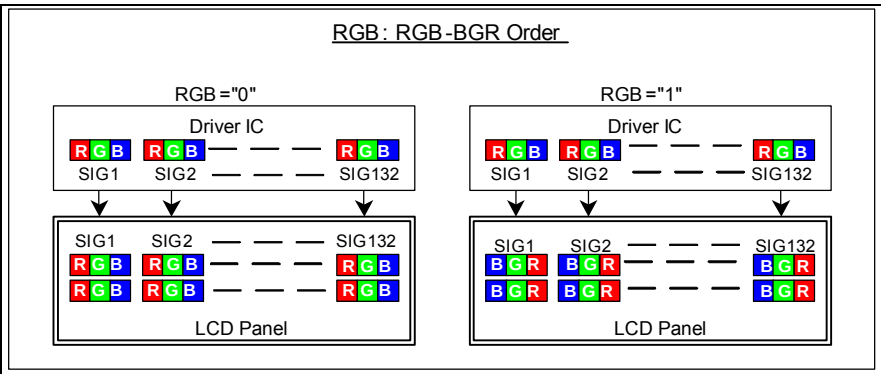
Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MPU to memory write/read direction. (See Section 5.2.3)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN EXCHANGE	
ML	Vertical refresh ORDER	LCD Vertical refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal refresh ORDER	LCD Horizontal refresh direction control







Restriction

D1 and D0 of the 1st parameter are set to '00'internally.

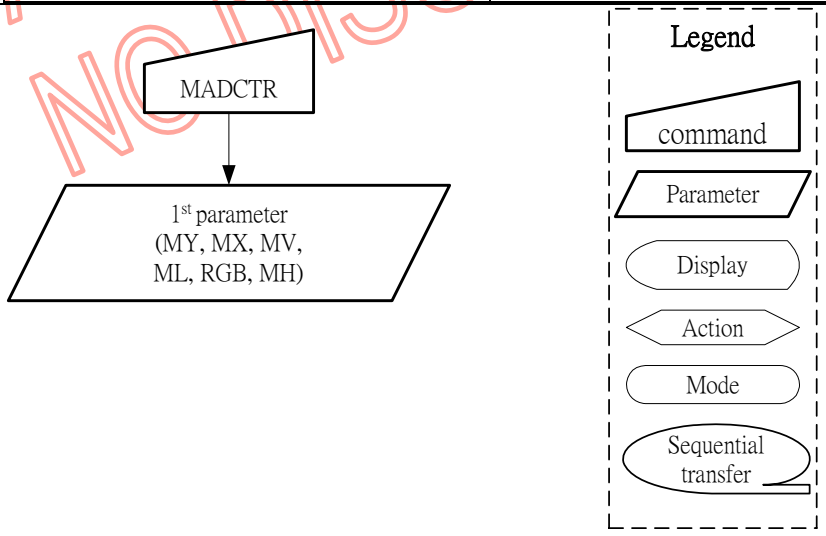
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0

Flow Chart



6.1.31 VSCSAD: Vertical Scroll Start Address of RAM (37h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VSCSAD	0	W	0	0	1	1	0	1	1	1	37h
1st parameter	1	W	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	-
2nd parameter	1	W	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	-

NOTE: "-" Don't care

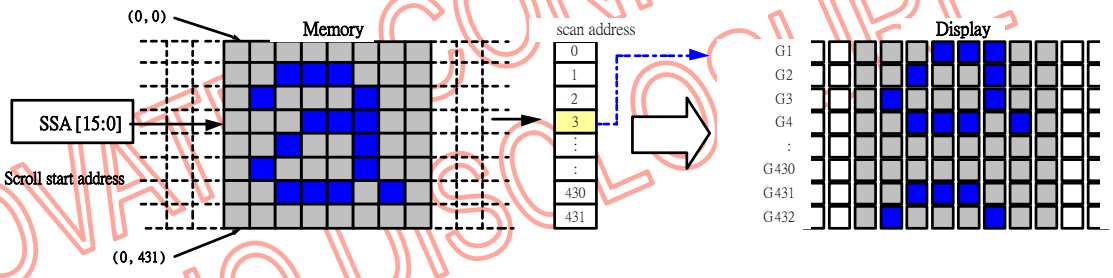
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
This command Start the scrolling.
Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML=0 (GM="00")

Example:

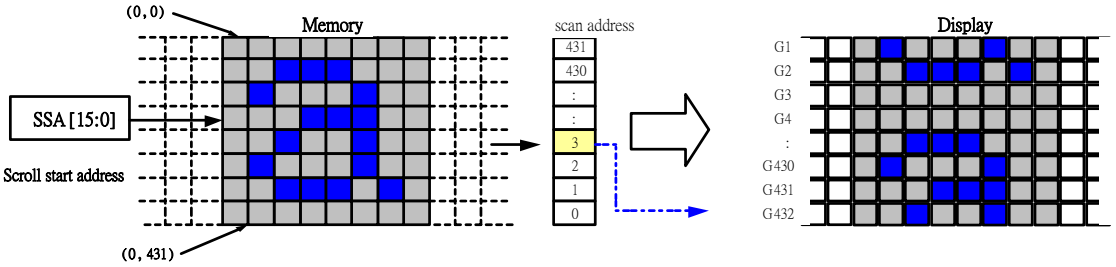
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=432 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML =1 (GM="00")

Example:

When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=432 and SSA='3'



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.
SSA[15:0] is based on 1-line unit.
SSA[15:0] = 0000h, 0001h, 0002h, 0003h, … , 01B0h

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.1.32 IDMOFF: Idle Mode Off (38h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMOFF	0	W	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter										

NOTE: "-" Don't care

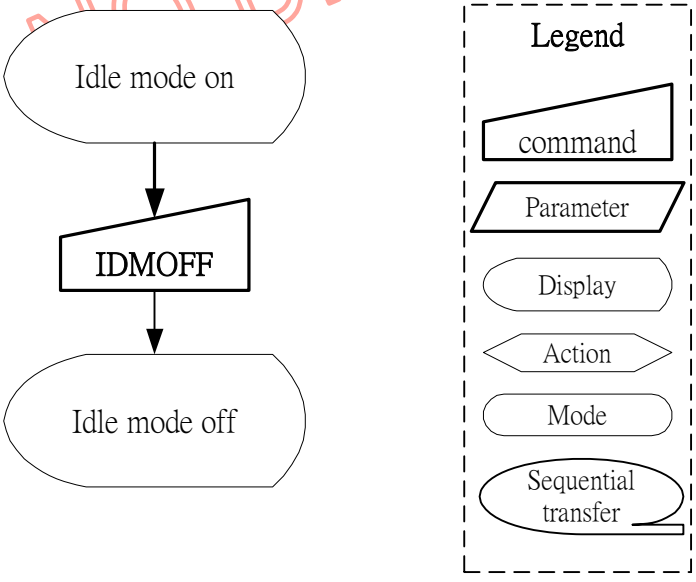
Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode, 1. LCD can display maximum 262k-colors. 2. Normal frame frequency is applied.
Restriction	This command has no effect when module is already in idle off mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off

Flow Chart



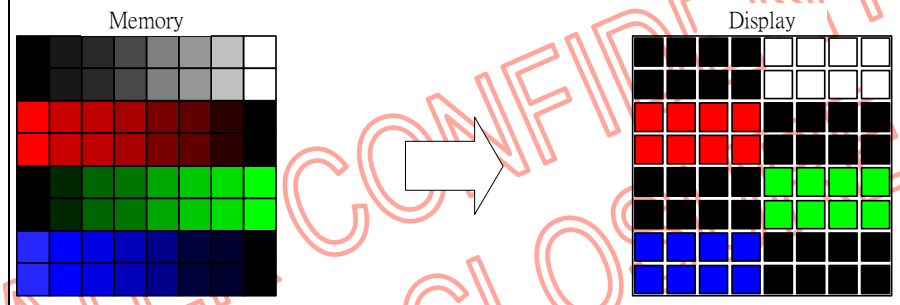
6.1.33 IDMON: Idle Mode On (39h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMON	0	W	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter										

NOTE: "-" Don't care

Description

This command is used to enter Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame rate is applied.
3. Exit from IDMON by Idle Mode Off (38h) command
(Example)



Color	$R_5R_4R_3R_2R_1R_0$	$G_5G_4G_3G_2G_1G_0$	$B_5B_4B_3B_4B_1B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

This command has no effect when module is already in idle on mode.

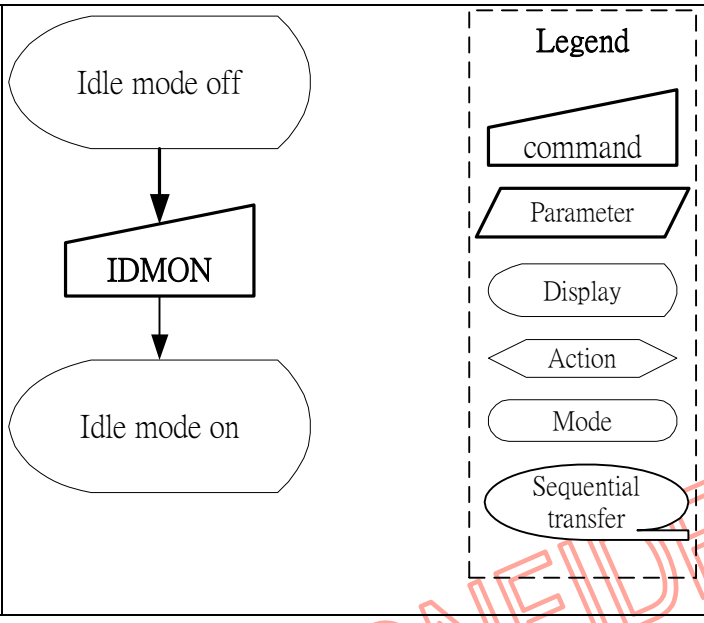
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off

Flow Chart



6.1.34 COLMOD: Interface Pixel Format (3Ah)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	0	W	0	0	1	1	1	0	1	0	3Ah
Parameter	1	W	VIPF3	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	-

NOTE: "-" Don't care

Description

IFPF[2:0]: This command is used to define the format of RGB picture data, which is to be transferred via the MPU Interface. The formats are shown in the table:

Interface Pixel Format	IFPF2	IFPF1	IFPF0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12Bit/Pixel	0	1	1
Not Defined	1	0	0
16Bit/Pixel	1	0	1
18Bit/Pixel	1	1	0
Not Defined	1	0	0

Note: In 12-bits/Pixel, 16-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

VIPF[3:0]: This command is used to define the format of RGB picture data, which is to be transferred via the RGB Interface. The formats are shown in the table:

RGB Interface Format	VIPF3	VIPF2	VIPF1	VIPF0
Not Defined	0	0	0	0
Not Defined	0	0	0	1
Not Defined	0	0	1	0
Not Defined	0	0	1	1
Not Defined	0	1	0	0
16Bit/Pixel (1 times data transfer)	0	1	0	1
18Bit/Pixel (1 times data transfer)	0	1	1	0
Not Defined	0	1	0	0
18Bit/Pixel (3 times data transfer)	1	x	x	x

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VIPF[3:0]	IFPF[2:0]
Power On Sequence	6h	6h
S/W Reset	No change	No change

Flow Chart

-

6.1.35 RDID1: Read ID1 Value (DAh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	0	W	1	1	0	1	1	0	1	0	DAh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
Parameter	1	R	0	0	1	1	1	0	0	0	38h

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module's manufacturer ID
The 1st parameter is dummy data
The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
NOTE: See command RDDID (04h), 2nd parameter.

Restriction

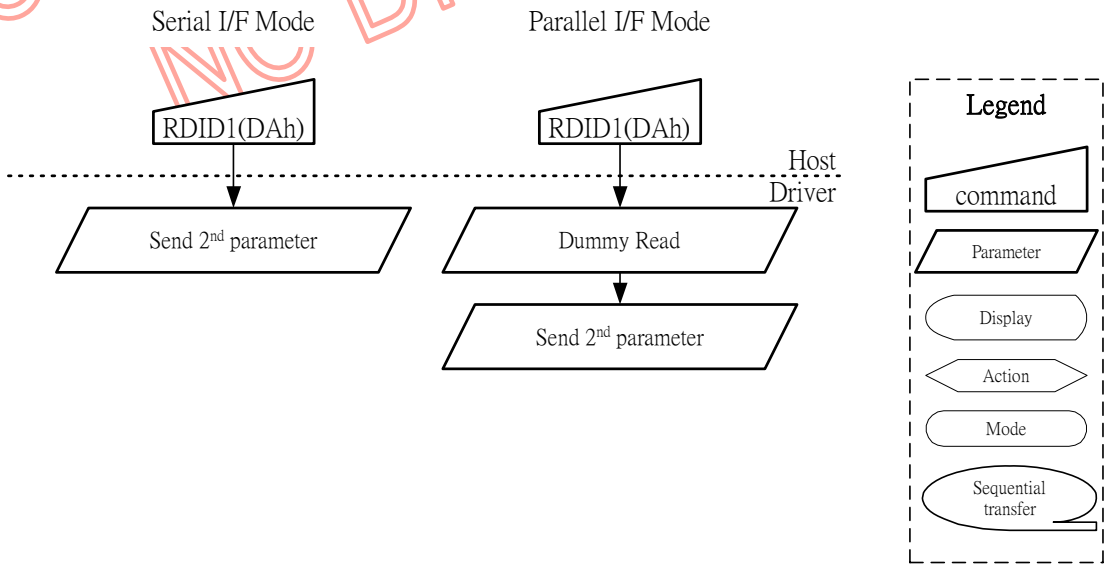
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	38h
S/W Reset	38h
H/W Reset	38h

Flow Chart



6.1.36 RDID2: Read ID2 Value (DBh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID2	0	W	1	1	0	1	1	0	1	1	DBh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
Parameter	1	R	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver version ID
The 1st parameter is dummy data
The 2nd parameter (ID26 to ID20): LCD module/driver version ID
Parameter Range: ID=80h to FFh
NOTE: See command RDDID (04h), 3rd parameter.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

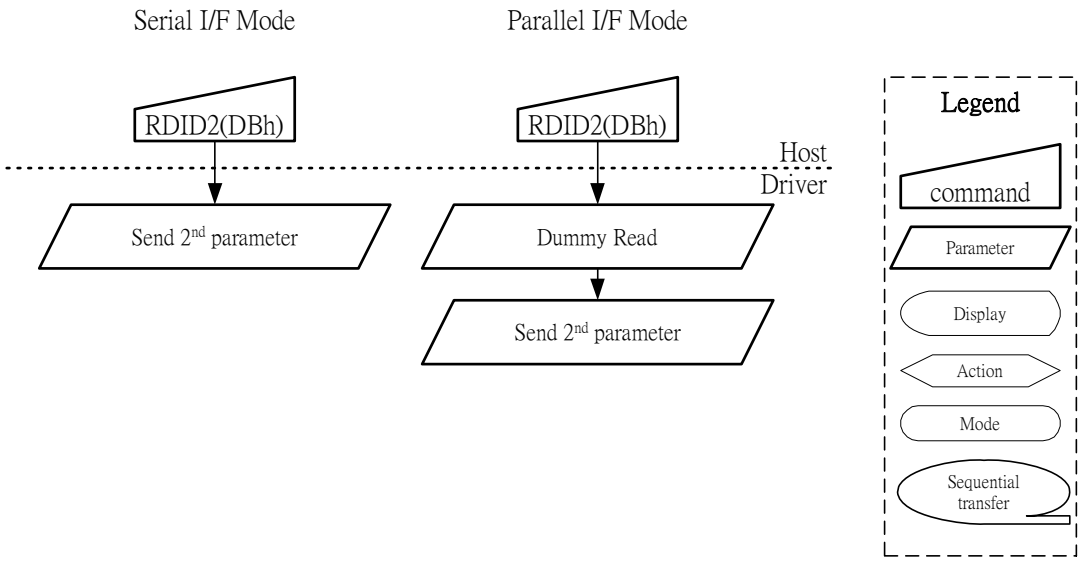
If ID2 MTP is not yet programmed:

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

If ID2 MTP was programmed:

Status	Default Value
Power On Sequence	(MTP value)
S/W Reset	(MTP value)
H/W Reset	(MTP value)

Flow Chart



6.1.37 RDID3: Read ID3 Value (DCh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID3	0	W	1	1	0	1	1	1	0	0	DCh
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
Parameter	1	R	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver ID.
The 1st parameter is dummy data
The 2nd parameter (ID37 to ID30): LCD module/driver ID.
NOTE: See command RDDID (04h), 4th parameter.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

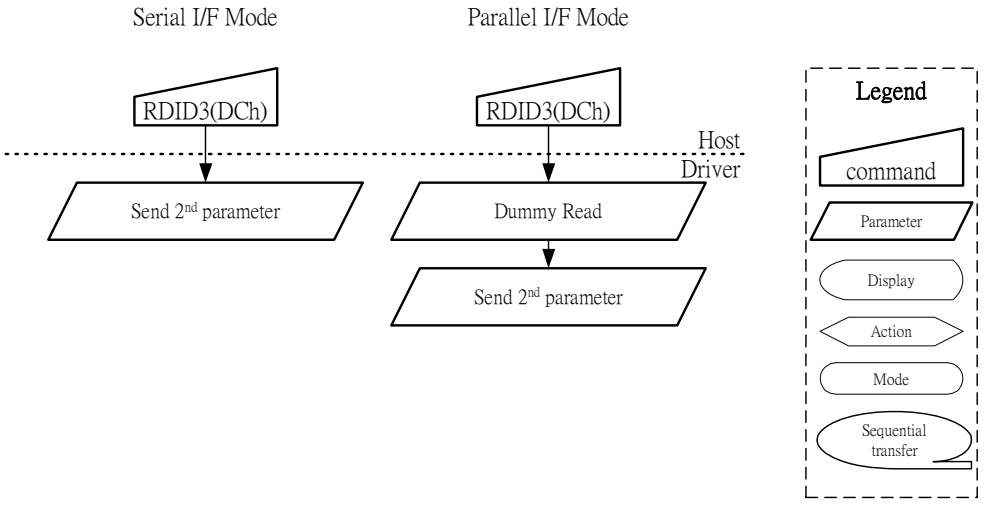
If ID3 MTP is not yet programmed:

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

If ID3 MTP is programmed:

Status	Default Value
Power On Sequence	(MTP value)
S/W Reset	(MTP value)
H/W Reset	(MTP value)

Flow Chart



6.2 Panel function Command List and Description

6.2.1 Panel Function Instruction Code Table

Table 6.2.1 Instruction Code

NO	Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1	IFMODE	0	W	1	0	1	1	0	0	0	0	(B0h)	Set Display I/F mode
		1	W	-	-	-	ICM	DP	EP	HSP	VSP		RGB signals polarity set
2	FRMCTR1	0	W	1	0	1	1	0	0	0	1	(B1h)	Division ratio- (full colors)
		1	R/W	-	-	-	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0		Division ratio
		1	R/W	-	VBPA6	VBPA5	VBPA4	VBPA3	VBPA2	VBPA1	VBPA0		V porch
3	FRMCTR2	0	W	1	0	1	1	0	0	1	0	(B2h)	Division ratio – (idle mode)
		1	R/W	-	-	-	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0		Division ratio
		1	R/W	-	VBPB6	VBPB5	VBPB4	VBPB3	VBPB2	VBPB1	VBPB0		V porch
4	FRMCTR3	0	W	1	0	1	1	0	0	1	1	(B3h)	Division ratio – (partial mode) + (full colors)
		1	R/W	-	-	-	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0		Division ratio
		1	R/W	-	VBPC6	VBPC5	VBPC4	VBPC3	VBPC2	VBPC1	VBPC0		V porch
5	INVCTR	0	W	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	R/W	-	-	-	-	-	NLA	NLB	NLC		set Line inversion
6	RESCTR	0	W	1	0	1	1	0	1	0	1	(B5h)	Display Resolution Control
		1	R/W							GM1	GM0		Set resolution
7	DISSET5	0	W	1	0	1	1	0	1	1	0	(B6h)	Display function setting
		1	R/W	-	-	NO1	NO0	SDT1	STD0	EQ1	EQ0		Panel timming setting
		1	R/W	-	-	ISCI3	ISCI2	ISCI1	ISCI0	PT1	PT0		PT: No display area source output control
8	PWCTR1	0	W	1	1	0	0	0	0	0	0	(C0h)	Power control setting
		1	R/W	-	-	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0		VRH: Set the GVDD voltage
9	PWCTR2	0	W	1	1	0	0	0	0	0	1	(C1h)	Power control setting
		1	R/W	-	-	-	-	-	BT2	BT1	BT0		BT: set AVDD/VCL/ VGH/ VGL voltage
		1	R/W	-	-	-	-	VRA3	VRA2	VRA1	VRA0		Step-up circuit setting
		1	R/W	-	-	-	-	-	GOT2	GOT1	GOT0		VGH voltage 2-level control
10	PWCTR3	0	W	1	1	0	0	0	0	1	0	(C2h)	Power control setting (Full colors)
		1	R/W	-	-	-	-	-	APA2	APA1	APA0		AP: adjust the operational amplifier
		1	R/W	-	-	-	-	-	DCA2	DCA1	DCA0		DC: adjust the booster circuit

Table 6.2.2 Instruction Code (Continue)

NO	Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
11	PWCTR4	0	W	1	1	0	0	0	0	1	1	(C3h)	Power control setting (8 olors)
		1	R/W	-	-	-	-	-	APB2	APB1	APB0		AP: adjust the operational amplifier
		1	R/W	-	-	-	-	-	DCB2	DCB1	DCB0		DC: adjust the booster circuit
12	PWCTR5	0	W	1	1	0	0	0	1	0	0	(C4h)	Power control setting (partial mode + Full colors)
		1	R/W	-	-	-	-	-	APC2	APC1	APC0		AP: adjust the operational amplifier
		1	R/W	-	-	-	-	-	DCC2	DCC1	DCC0		DC: adjust the booster circuit
13	VMCTR1	0	W	1	1	0	0	0	1	0	1	(C5)	VCOM control 1
		1	R/W	-	VMH6	VMH5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0		VCOMH voltage control
		1	R/W	-	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0		VCOML voltage control
14	VMFCTR	0	W	1	1	0	0	0	1	1	1	(C7h)	VCOM control 3
		1	W	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		VMF: VCOM offset control
15	RDVMF	0	W	1	1	0	0	1	0	0	0	(C8h)	VCOM control 4
		1	R	-	-	-	-	-	-	-	-		Dummy read
		1	R	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		VMF: VCOM offset control
16	WRID2	0	W	1	1	0	1	0	0	0	1	(D1h)	Write ID2
		1	W	-	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
17	WRID3	0	W	1	1	0	1	0	0	1	0	(D2h)	Write ID3
		1	W	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
18	RDID4	0	W	1	1	0	1	0	0	1	1	(D3h)	Read Vender code
		1	R	-	-	-	-	-	-	-	-	-	Dummy Clock Cycle
		1	R	0	0	0	0	0	0	0	1	-	Vender ID code
		1	R	0	0	1	0	0	1	0	1	25h	Chip ID code
		1	R	-	-	-	-	ID43	ID42	ID41	ID40	-	Chip Version code
19	RDNVF	0	W	1	1	0	1	0	1	0	0	(D4h)	
		1	R	-	-	-	-	-	-	-	-		
		1	R	NV_N3	NV_N2	NV_N1	NV_N0	0	NV_P	1	EXTC_F		
		1	R	-	-	-	-	-	-	-	NV_DF		
20	EPWRITE	0	W	1	1	0	1	1	1	1	0	(DEh)	MTP write
		1	W	0	1	0	1	0	1	0	1	55h	
		1	W	1	0	1	0	1	0	1	0	AAh	
		1	W	0	1	1	0	0	1	1	0	66h	
21	DNVRS	0	W	1	1	0	1	1	1	1	1	(DFh)	
		1	R/W	-	-	-	-	-	-	-	EN_PDT		
22	GMCTRP0	0	R/W	1	1	1	0	0	0	0	0	(E0h)	Set Red Positive Gamma
23	CMCTRN0	0	R/W	1	1	1	0	0	0	0	1	(E1h)	Set Red Negative Gamma
24	GMCTRP1	0	R/W	1	1	1	0	0	0	1	0	(E2h)	Set Green Positive Gamma
25	CMCTRN1	0	R/W	1	1	1	0	0	0	1	1	(E3h)	Set Green Negative Gamma
26	GMCTRP2	0	R/W	1	1	1	0	0	1	0	0	(E4h)	Set Blue Positive Gamma
27	GMCTRN2	0	R/W	1	1	1	0	0	1	0	1	(E5h)	Set Blue Negative Gamma
28	GAM_R_SEL	0	W	1	1	1	0	1	0	1	0	(EAh)	
		1	R/W	-	-	-	-	-	-	-	GAM_R_SEL		
29	TSTGVDD	0	W	1	1	1	0	1	0	1	1	(EBh)	
		1	R/W	-	-	-	-	-	-	-	TEST_GVDD		

6.2.2 IFMODE: Set Display Interface Mode (B0h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IFMODE	**0**	**W**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**(B0h)**
Parameter	**1**	**W**	**-**	**-**	**-**	**ICM**	**DP**	**EP**	**HSP**	**VSP**	**-**

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

ICM: RGB Interface clock selection ("0"=PCLK, "1"=internal clock)
DP: PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time)
EP: DE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)
HSP: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)
VSP: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ICM	DP/EP/HSP/VSP
Power On Sequence	0	0/0/0/0
S/W Reset	0	0/0/0/0

6.2.3 FRMCTR1: Set Division ratio for internal clocks of Normal mode (B1h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FRMCTR1	0	W	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	R/W	-	-	-	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	-
2nd parameter	1	R/W	-	VBPA6	VBPA5	VBPA4	VBPA3	VBPA2	VBPA1	VBPA0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the frame frequency of Normal mode.

DIVA[4:0]: Set the HCLK frequency for internal clocks when Normal mode.

DIVA[4:0]		HCLK	DIVA [4:0]		HCLK	DIVA [4:0]		HCLK	DIVA [4:0]		HCLK
00000	0	27,600	01000	8	38,640	10000	16	26,220	11000	24	15,180
00001	1	28,980	01001	9	40,020	10001	17	24,840	11001	25	13,800
00010	2	30,360	01010	10	41,400	10010	18	23,460	11010	26	12,420
00011	3	31,740	01011	11	42,780	10011	19	22,080	11011	27	11,040
00100	4	33,120	01100	12	44,160	10100	20	20,700	11100	28	9,660
00101	5	34,500	01101	13	45,540	10101	21	19,320	11101	29	8,280
00110	6	35,880	01110	14	46,920	10110	22	17,940	11110	30	6,900
00111	7	37,260	01111	15	48,300	10111	23	16,560	11111	31	5,520

VPA[6:0]: Vsync porch for internal clocks when normal mode.

VPA[6:0]		Vsync porch
0000000	0	Forbidden
0000001	1	Forbidden
0000010	2	2 line
…	…	…
1111110	126	126 lines
1111111	127	127 lines

In Normal mode, DIVA[4:0] =0, line=432, VPA[6:0]=28

$$Frame\_rate = \frac{HCLK}{(Line+VPA[8:0])} = 60Hz$$

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVA[4:0]	VPA[6:0]
Power On Sequence	00h	1Ch
S/W Reset	00h	1Ch
H/W Reset	00h	1Ch

NTOE: Default frame rate = 60Hz

6.2.4 FRMCTR2: Set Division ratio for internal clocks of Idle mode (B2h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FRMCTR2	0	W	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	R/W	-	-	-	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	-
2nd parameter	1	R/W	-	VBPB6	VBPB5	VBPB4	VBPB3	VBPB2	VBPB1	VBPB0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the frame frequency of Normal mode.

DIVB[4:0]: Set the HCLK frequency for internal clocks when Idle mode.

DIVB[4:0]		HCLK	DIVB [4:0]		HCLK	DIVB [4:0]		HCLK	DIVB [4:0]		HCLK
00000	0	27,600	01000	8	38,640	10000	16	26,220	11000	24	15,180
00001	1	28,980	01001	9	40,020	10001	17	24,840	11001	25	13,800
00010	2	30,360	01010	10	41,400	10010	18	23,460	11010	26	12,420
00011	3	31,740	01011	11	42,780	10011	19	22,080	11011	27	11,040
00100	4	33,120	01100	12	44,160	10100	20	20,700	11100	28	9,660
00101	5	34,500	01101	13	45,540	10101	21	19,320	11101	29	8,280
00110	6	35,880	01110	14	46,920	10110	22	17,940	11110	30	6,900
00111	7	37,260	01111	15	48,300	10111	23	16,560	11111	31	5,520

VPB[6:0]: Vsync porch for internal clocks when Idle mode.

VPB[6:0]		Vsync porch
0000000	0	Forbidden
0000001	1	Forbidden
0000010	2	2 line
…	…	…
1111110	126	126 lines
1111111	127	127 lines

In idle mode, DIVB[4:0] ="14h", line=432, VPB[6:0]=28

$$Frame\_rate = \frac{HCLK}{(Line+VPB[8:0])} = 45Hz$$

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVB[4:0]	VPB[6:0]
Power On Sequence	14h	1Ch
S/W Reset	14h	1Ch
H/W Reset	14h	1Ch

NTOE: Default frame rate = 45Hz

6.2.5 FRMCTR3: Set Division ratio for internal clocks of Partial mode (Idle mode off) (B3h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FRMCTR3	0	W	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	R/W	-	-	-	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	-
2nd parameter	1	R/W	-	VBPC6	VBPC5	VBPC4	VBPC3	VBPC2	VBPC1	VBPC0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the frame frequency of Normal mode.

DIVC[4:0]: Set the HCLK frequency for internal clocks when partial mode.

DIVC[4:0]		HCLK	DIVC [4:0]		HCLK	DIVC [4:0]		HCLK	DIVC [4:0]		HCLK
00000	0	27,600	01000	8	38,640	10000	16	26,220	11000	24	15,180
00001	1	28,980	01001	9	40,020	10001	17	24,840	11001	25	13,800
00010	2	30,360	01010	10	41,400	10010	18	23,460	11010	26	12,420
00011	3	31,740	01011	11	42,780	10011	19	22,080	11011	27	11,040
00100	4	33,120	01100	12	44,160	10100	20	20,700	11100	28	9,660
00101	5	34,500	01101	13	45,540	10101	21	19,320	11101	29	8,280
00110	6	35,880	01110	14	46,920	10110	22	17,940	11110	30	6,900
00111	7	37,260	01111	15	48,300	10111	23	16,560	11111	31	5,520

VPC[6:0]: Vsync porch for internal clocks when partial mode.

VPC[6:0]		Vsync porch
0000000	0	Forbidden
0000001	1	Forbidden
0000010	2	2 line
…	…	…
1111110	126	126 lines
1111111	127	127 lines

In partial mode, DIVC[4:0] =0, line=432, VPC[6:0]=28

$$Frame\_rate = \frac{HCLK}{(Line+VPC[8:0])} = 60Hz$$

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVC[4:0]	VPC[6:0]
Power On Sequence	00h	1Ch
S/W Reset	00h	1Ch
H/W Reset	00h	1Ch

NTOE: Default frame rate = 60Hz

6.2.6 INVCTR: Inversion Control (B4h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVCTR	**0**	**W**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**(B4h)**
Parameter	**1**	**R/W**	**-**	**-**	**-**	**-**	**-**	**NLA**	**NLB**	**NLC**	**-**

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Display inversion mode set

NLA: Inversion setting in full colors normal mode (Normal mode on)

NLB: Inversion setting in Idle mode (Idle mode on)

NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLA / NLB / NLC	Inversion
0	Line inversion
1	Frame inversion

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	NLA	NLB	NLC
Power On Sequence	0	1	0
S/W Reset	0	1	0
H/W Reset	0	1	0

6.2.7 RESCTR: Display Resolution Control (B5h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RESCTR	0	W	1	0	1	1	0	1	0	1	(B5h)
Parameter	1	W	-	-	-	-	-	-	GM1	GM0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

GM1-0: Set the display resolution.

GM[1:0]		Display resolution
00	0	240xRGB(H)x432(V)
01	1	240xRGB(H)x400(V)
10	2	240xRGB(H)x320(V)
11	3	Setting disabled

-The display resolution can be selected by either H/W pin or Command. When Power On or H/W reset, the function follow H/W pin setting first.

-If the register is not changed, the GM H/W pin is always valid. If the register is changed, display resolution should follow the register setting.

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	03h
S/W Reset	03h

6.2.8 DISSET5: Display Function set 5 (B6h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISSET5	0	W	1	0	1	1	0	1	1	0	(B6h)
1st parameter	1	R/W	-	-	NO1	NO0	SDT1	STD0	EQ1	EQ0	-
2nd parameter	1	R/W	-	-	ISCI3	ISCI2	ISCI1	ISCI0	PT1	PT0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

NO[1:0]: Sets amount of non-overlap of the gate output.

NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	8 clock cycle
01	1	2 clock cycle	16 clock cycle
10	2	3 clock cycle	24 clock cycle
11	3	4 clock cycle	32 clock cycle

SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

SDT[1:0]		Amount of non-overlap of the source output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	8 clock cycle
01	1	2 clock cycle	16 clock cycle
10	2	3 clock cycle	24 clock cycle
11	3	4 clock cycle	32 clock cycle

EQ1-0: Sets the equalizing period

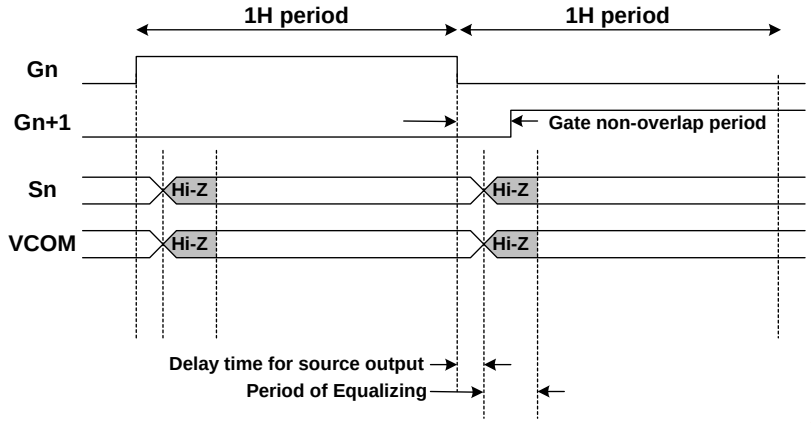
EQ[1:0]		EQ period	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle

ISCI[3:0]: Determine Gate output in a non-display area in the partial display mode.

ISCI[3:0]		Gate output in a non-display area
0000	0	(Full scan)
0001	1	Interval Scan Rate = 3
0010	2	Interval Scan Rate = 5
0011	3	Interval Scan Rate = 7
0100	4	Interval Scan Rate = 9
0101	5	Interval Scan Rate = 11
0110	6	Interval Scan Rate = 13
0111	7	Interval Scan Rate = 15
1000~1111	8	(Fix to VGL)

PT[1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND



Restriction: -

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	NO[1:0]	STD[1:0]	EQ[1:0]	ISCI[3:0]	PT[1:0]
Power On Sequence	0h	0h	1h	0h	2h
S/W Reset	0h	0h	1h	0h	2h
H/W Reset	0h	0h	1h	0h	2h

Flow Chart

6.2.9 PWCTR1: Power Control 1(C0h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTR1	0	W	1	1	0	0	0	0	0	0	(C0h)
Parameter	1	R/W	-	-	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the GVDD regulator output voltage

VRH[5:0]: set the GVDD regulator output voltage.

VRH[5:0]		GVDD	VRH[5:0]		GVDD	VRH[5:0]		GVDD	VRH[5:0]		GVDD
000000	0	5.000V	010000	16	4.600V	100000	32	4.200V	110000	48	3.800V
000001	1	4.975V	010001	17	4.575V	100001	33	4.175V	110001	49	3.775V
000010	2	4.950V	010010	18	4.550V	100010	34	4.150V	110010	50	3.750V
000011	3	4.925V	010011	19	4.525V	100011	35	4.125V	110011	51	3.725V
000100	4	4.900V	010100	20	4.500V	100100	36	4.100V	110100	52	3.700V
000101	5	4.875V	010101	21	4.475V	100101	37	4.075V	110101	53	3.675V
000110	6	4.850V	010110	22	4.450V	100110	38	4.050V	110110	54	3.650V
000111	7	4.825V	010111	23	4.425V	100111	39	4.025V	110111	55	3.625V
001000	8	4.800V	011000	24	4.400V	101000	40	4.000V	111000	56	3.600V
001001	9	4.775V	011001	25	4.375V	101001	41	3.975V	111001	57	3.575V
001010	10	4.750V	011010	26	4.350V	101010	42	3.950V	111010	58	3.550V
001011	11	4.725V	011011	27	4.325V	101011	43	3.925V	111011	59	3.525V
001100	12	4.700V	011100	28	4.300V	101100	44	3.900V	111100	60	3.500V
001101	13	4.675V	011101	29	4.275V	101101	45	3.875V	111101	61	3.475V
001110	14	4.650V	011110	30	4.250V	101110	46	3.850V	111110	62	3.450V
001111	15	4.625V	011111	31	4.225V	101111	47	3.825V	111111	63	3.425V

-The step voltage = 25mV

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value of VRH[5:0]
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart

6.2.10 PWCTR2: Power Control 2(C1h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTR2	0	W	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	R/W	-	-	-	-	-	BT2	BT1	BT0	-
2nd parameter	1	R/W	-	-	-	-	VRA3	VRA2	VRA1	VRA0	-
3rd parameter	1	R/W	-	-	-	-	-	GOT2	GOT1	GOT0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

BT[2:0] : Set the AVDD, VCL, VGH and VGL supply power level

BT[2:0]		AVDD	VCL	VGH	VGL
000	0	VCI x 2	- VCI x 1	VR x 3	- VR x 2 – VCI
001	1				- VR x 2
010	2				- VR – VCI
011	3			VR x 2 + VCI	- VR x 2 – VCI
100	4				- VR x 2
101	5				- VR – VCI
110	6			VR x 2	- VR x 2
111	7				- VR – VCI

VRA[3:0]: Set the VR regulator output voltage.

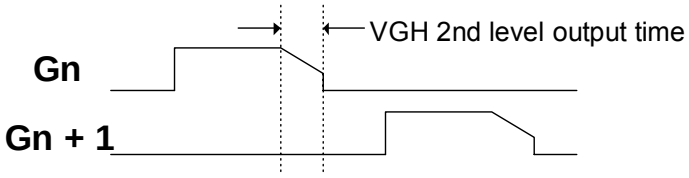
VRA[3:0]		VR voltage	VRA[3:0]		VR voltage
0000	0	4.1V	1000	8	4.9V
0001	1	4.2V	1001	9	5.0V
0010	2	4.3V	1010	10	5.1V
0011	3	4.4V	1011	11	5.2V
0100	4	4.5V	1100	12	5.3V
0101	5	4.6V	1101	13	5.4V
0110	6	4.7V	1110	14	5.5V
0111	7	4.8V	1111	15	Hi-Z

-The step voltage = 100mV

Note : The VR regulator output is the reference voltage of VGH/VGL. When VRA = "1111", the driver IC turns off the VR regulator and the VGH/VGL reference the AVDD instead.

GOT[2:0]: Set the VGH 2nd level output time range

GOT[2:0]		VGH2_Time
000	0	0.0us
001	1	2.0us
010	2	4.0us
011	3	6.0us
100	4	8.0us
101	5	10.0us
110	6	12.0us
111	7	14.0us



Note: The VGH 2nd level output voltage =VCI

<table>
<tr><td>Restriction</td><td>-If this register not using the register need be reserved.
-The deviation value of VGH/ VGL between with Measurement and Specification: Max: VGH-VGL<=1V
-VGH-VGL <= 25V
-The VGH 2nd level output voltage =10.0V</td></tr>
<tr><td>Register Available</td><td>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>BT[2:0]</th><th>VRA[3:0]</th><th>GOT[2:0]</th></tr>
<tr><td>Power On Sequence</td><td>0h</td><td>Bh</td><td>0h</td></tr>
<tr><td>S/W Reset</td><td>0h</td><td>Bh</td><td>0h</td></tr>
<tr><td>H/W Reset</td><td>0h</td><td>Bh</td><td>0h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

6.2.11 PWCTR3: Power Control 3 (in Normal mode/ Full colors) (C2h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTR3	0	W	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	R/W	-	-	-	-	-	APA2	APA1	APA0	-
2nd parameter	1	R/W	-	-	-	-	-	DCA2	DCA1	DCA0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the amount of current in Operational amplifier in normal mode/full colors.

APA[2:0]: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APA[2:0]		Op-amp power
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Small to Medium
011	3	Medium
100	4	Medium to large
101	5	Large
110	6	Reserved
111	7	Reserved

DCA[2:0]: set the operating frequency of the step-up circuit for Normal mode

DCA[2:0]		Step-up cycle for step-up circuit 1/4	Step-up cycle for step-up circuit 2/3
000	0	DCCLK/1	DCCLK/2
001	1	DCCLK/1	DCCLK/4
010	2	DCCLK/1	DCCLK/16
011	3	DCCLK/2	DCCLK/4
100	4	DCCLK/2	DCCLK/16
101	5	DCCLK/4	DCCLK/16
110	6	DCCLK/4	DCCLK/32
111	7	DCCLK/8	DCCLK/32

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APA[2:0]	DCA[2:0]
Power On Sequence	4h	3h
S/W Reset	4h	3h
H/W Reset	4h	3h

Flow Chart

6.2.12 PWCTR4: Power Control 4 (in Idle mode/ 8-colors) (C3h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTR4	0	W	1	1	0	0	0	0	1	1	(C3h)
1st parameter	1	R/W	-	-	-	-	-	APB2	APB1	APB0	-
2nd parameter	1	R/W	-	-	-	-	-	DCB2	DCB1	DCB0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the amount of current in Operational amplifier in Idle mode/ 8-colors.

APB[2:0]: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APB[2:0]		Op-amp power
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Small to Medium
011	3	Medium
100	4	Medium to large
101	5	Large
110	6	Reserved
111	7	Reserved

DCB[2:0]: set the operating frequency of the step-up circuit for Idle mode

DCB[2:0]		Step-up cycle for step-up circuit 1/4	Step-up cycle for step-up circuit 2/3
000	0	DCCLK/1	DCCLK/2
001	1	DCCLK/1	DCCLK/4
010	2	DCCLK/1	DCCLK/16
011	3	DCCLK/2	DCCLK/4
100	4	DCCLK/2	DCCLK/16
101	5	DCCLK/4	DCCLK/16
110	6	DCCLK/4	DCCLK/32

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APB[2:0]	DCB[2:0]
Power On Sequence	2h	5h
S/W Reset	2h	5h
H/W Reset	2h	5h

Flow Chart

6.2.13 PWCTR5: Power Control 5 (in Partial mode/ full-colors) (C4h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTR5	0	W	1	1	0	0	0	1	0	0	(C4h)
1st parameter	1	R/W	-	-	-	-	-	APC2	APC1	APC0	-
2nd parameter	1	R/W	-	-	-	-	-	DCC2	DCC1	DCC0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

Set the amount of current in Operational amplifier in Partial mode/ full-colors.

APC[2:0]: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APC[2:0]		Op-amp power
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Small to Medium
011	3	Medium
100	4	Medium to large
101	5	Large
110	6	Reserved
111	7	Reserved

DCC[2:0]: set the operating frequency of the step-up circuit for Partial mode

DCC[2:0]		Step-up cycle for step-up circuit 1/4	Step-up cycle for step-up circuit 2/3
000	0	DCCLK/1	DCCLK/2
001	1	DCCLK/1	DCCLK/4
010	2	DCCLK/1	DCCLK/16
011	3	DCCLK/2	DCCLK/4
100	4	DCCLK/2	DCCLK/16
101	5	DCCLK/4	DCCLK/16
110	6	DCCLK/4	DCCLK/32

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	2h	4h
S/W Reset	2h	4h
H/W Reset	2h	4h

Flow Chart

6.2.14 VMCTR1: VCOM Control (C5h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VMCTR1	0	W	1	1	0	0	0	1	0	1	(C5)
1st parameter	1	R/W	-	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	-
2nd parameter	1	R/W	-	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

-Set VCOMH Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500V	0011011	27	3.175V	0110110	54	3.850V	1010001	81	4.525V
0000001	1	2.525V	0011100	28	3.200V	0110111	55	3.875V	1010010	82	4.550V
0000010	2	2.550V	0011101	29	3.225V	0111000	56	3.900V	1010011	83	4.575V
0000011	3	2.575V	0011110	30	3.250V	0111001	57	3.925V	1010100	84	4.600V
0000100	4	2.600V	0011111	31	3.275V	0111010	58	3.950V	1010101	85	4.625V
0000101	5	2.625V	0100000	32	3.300V	0111011	59	3.975V	1010110	86	4.650V
0000110	6	2.650V	0100001	33	3.325V	0111100	60	4.000V	1010111	87	4.675V
0000111	7	2.675V	0100010	34	3.350V	0111101	61	4.025V	1011000	88	4.700V
0001000	8	2.700V	0100011	35	3.375V	0111110	62	4.050V	1011001	89	4.725V
0001001	9	2.725V	0100100	36	3.400V	0111111	63	4.075V	1011010	90	4.750V
0001010	10	2.750V	0100101	37	3.425V	1000000	64	4.100V	1011011	91	4.775V
0001011	11	2.775V	0100110	38	3.450V	1000001	65	4.125V	1011100	92	4.800V
0001100	12	2.800V	0100111	39	3.475V	1000010	66	4.150V	1011101	93	4.825V
0001101	13	2.825V	0101000	40	3.500V	1000011	67	4.175V	1011110	94	4.850V
0001110	14	2.850V	0101001	41	3.525V	1000100	68	4.200V	1011111	95	4.875V
0001111	15	2.875V	0101010	42	3.550V	1000101	69	4.225V	1100000	96	4.900V
0010000	16	2.900V	0101011	43	3.575V	1000110	70	4.250V	1100001	97	4.925V
0010001	17	2.925V	0101100	44	3.600V	1000111	71	4.275V	1100010	98	4.950V
0010010	18	2.950V	0101101	45	3.625V	1001000	72	4.300V	1100011	99	4.975V
0010011	19	2.975V	0101110	46	3.650V	1001001	73	4.325V	1100100	100	5.000V
0010100	20	3.000V	0101111	47	3.675V	1001010	74	4.350V	1100101	101	Reserved
0010101	21	3.025V	0110000	48	3.700V	1001011	75	4.375V	:	:	
0010110	22	3.050V	0110001	49	3.725V	1001100	76	4.400V	1111111	127	
0010111	23	3.075V	0110010	50	3.750V	1001101	77	4.425V			
0011000	24	3.100V	0110011	51	3.775V	1001110	78	4.450V			
0011001	25	3.125V	0110100	52	3.800V	1001111	79	4.475V			
0011010	26	3.150V	0110101	53	3.825V	1010000	80	4.500V			

-The step voltage = 25mV

-Set VCOML Voltage

VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML
0000000	0	-2.500V	0011011	27	-1.825V	0110110	54	-1.150V	1010001	81	-0.475V
0000001	1	-2.475V	0011100	28	-1.800V	0110111	55	-1.125V	1010010	82	-0.450V
0000010	2	-2.450V	0011101	29	-1.775V	0111000	56	-1.100V	1010011	83	-0.425V
0000011	3	-2.425V	0011110	30	-1.750V	0111001	57	-1.075V	1010100	84	-0.400V
0000100	4	-2.400V	0011111	31	-1.725V	0111010	58	-1.050V	1010101	85	-0.375V
0000101	5	-2.375V	0100000	32	-1.700V	0111011	59	-1.025V	1010110	86	-0.350V
0000110	6	-2.350V	0100001	33	-1.675V	0111100	60	-1.000V	1010111	87	-0.325V
0000111	7	-2.325V	0100010	34	-1.650V	0111101	61	-0.975V	1011000	88	-0.300V
0001000	8	-2.300V	0100011	35	-1.625V	0111110	62	-0.950V	1011001	89	-0.275V
0001001	9	-2.275V	0100100	36	-1.600V	0111111	63	-0.925V	1011010	90	-0.250V
0001010	10	-2.250V	0100101	37	-1.575V	1000000	64	-0.900V	1011011	91	-0.225V

0001011	11	-2.225V	0100110	38	-1.550V	1000001	65	-0.875V	1011100	92	-0.200V
0001100	12	-2.200V	0100111	39	-1.525V	1000010	66	-0.850V	1011101	93	-0.175V
0001101	13	-2.175V	0101000	40	-1.500V	1000011	67	-0.825V	1011110	94	-0.150V
0001110	14	-2.150V	0101001	41	-1.475V	1000100	68	-0.800V	1011111	95	-0.125V
0001111	15	-2.125V	0101010	42	-1.450V	1000101	69	-0.775V	1100000	96	-0.100V
0010000	16	-2.100V	0101011	43	-1.425V	1000110	70	-0.750V	1100001	97	-0.075V
0010001	17	-2.075V	0101100	44	-1.400V	1000111	71	-0.725V	1100010	98	-0.050V
0010010	18	-2.050V	0101101	45	-1.375V	1001000	72	-0.700V	1100011	99	-0.025V
0010011	19	-2.025V	0101110	46	-1.350V	1001001	73	-0.675V	1100100	100	0.000V
0010100	20	-2.000V	0101111	47	-1.325V	1001010	74	-0.650V	1100101	101	Reserved
0010101	21	-1.975V	0110000	48	-1.300V	1001011	75	-0.625V	:	:	
0010110	22	-1.950V	0110001	49	-1.275V	1001100	76	-0.600V	1111111	127	
0010111	23	-1.925V	0110010	50	-1.250V	1001101	77	-0.575V			
0011000	24	-1.900V	0110011	51	-1.225V	1001110	78	-0.550V			
0011001	25	-1.875V	0110100	52	-1.200V	1001111	79	-0.525V			
0011010	26	-1.850V	0110101	53	-1.175V	1010000	80	-0.500V			

-The step voltage = 25mV

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Dedault Value	
	VMH[6:0]	VML[6:0]
Power On Sequence	50h	34h
S/W Reset	50h	34h
H/W Reset	50h	34h

Flow Chart

6.2.15 VMFCTR: VCOM offset control (C7h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VMFCTR	0	W	1	1	0	0	0	1	1	1	(C7h)
Parameter	1	W	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	-

NOTE: "-" Don't care

Description

nVM: nVM equals to "0" after power on reset and VCOM offset equals to programmed MTP value. When nVM set to "1", setting of VMF6-0 becomes valid and VCOMH/VCOML can be adjusted.

VMF[6:0]: set the VCOM offset voltage.

VMF[6:0]	VMH[6:0] (internal)	VML[6:0] (internal)
00h(default)	VMH	VML
01h	VMH-63	VML-63
02h	VMH-62	VML-62
:	:	:
3Fh	VMH-1	VML-1
40h	VMH	VML
41h	VMH+1	VML+1
:	:	:
7Dh	VMH+61	VML+61
7Eh	VMH+62	VML+62
7Fh	VMH+63	VML+63

-The step voltage is 25mV

-The VCOMH Voltage Range = 2.5V ~ 5.0V

-The VCOML Voltage Range = -2.5V ~ 0V

Restriction: To control VCOM voltage with VMF command, nVM bit should be set to "1"

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	nVM	VMF[6:0]
Power On Sequence	0	00h
S/W Reset	0	00h
H/W Reset	0	00h

Flow Chart

6.2.16 RDVMF: Read VCOM offset value (C8h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDVMF	0	W	1	1	0	0	1	0	0	0	(C8h)
Dummy Clock	1	R	-	-	-	-	-	-	-	-	-
Parameter	1	R	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	-

NOTE: "-" Don't care

Description: Read VCOM offset value.

Restriction: -

Register Available:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value	
	nVM	VMF[6:0]
Power On Sequence	0	00h
S/W Reset	0	00h
H/W Reset	0	00h

Flow Chart

6.2.17 WRID2: Write ID2 for MTP program (D1h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRID2	0	W	1	1	0	1	0	0	0	1	(D1h)
Parameter	1	W	-	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description	Write 7-bit LCD module/driver version ID to save it to MTP. ID2[6:0]: LCD module/driver version ID(specified by module supplier).
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	-

6.2.18 WRID3: Write ID3 for MTP program (D2h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRID3	0	W	1	1	0	1	0	0	1	0	(D2h)
Parameter	1	W	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description	Write 8-bit project ID to save it to MTP. ID3[7:0]: project ID (specified by handset company).
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

6.2.19 RDID4: Read ID4 for IC Vender Code (D3h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID4	**0**	**W**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**(D3h)**
Dummy Clock	**1**	**R**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
1st parameter	**1**	**R**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**01h**
2nd parameter	**1**	**R**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**25h**
3rd parameter	**1**	**R**	**-**	**-**	**-**	**-**	**ID43**	**ID42**	**ID41**	**ID40**	**-**

NOTE: "-" Don't care

Description

Read IC vender code.
1st parameter : Dummy read
2nd parameter: Vender ID code. "01" means *Novatek.*
3rd parameter: Chip ID code. "25" means NT39125.
ID43-ID40: Chip version code.

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	ID4 Default Value
Power On Sequence	0h (cut1)
S/W Reset	0h (cut1)
H/W Reset	0h (cut1)

Flow Chart

6.2.20 RDVNT: Read NV Memory Flag Status (D4h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDNVF	**0**	**W**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**(D4h)**
Dummy Clock	**1**	**R**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
1st parameter	**1**	**R**	NV_N3	NV_N2	NV_N1	NV_N0	0	NV_P	**1**	EXTC_F	
2nd parameter	**1**	**R**	-	-	-	-	-	-	-	NV_DF	

NOTE: "-" Don't care

Description

-This command indicates the current status of the NV memory as described in the table below:

Flag	Description	Value
EXTC_F	EXTC Flag Status	'0' = EXTC is Ground level, '1' = EXTC is VDDI level,
NV_P	NV Memory Program Finish Status	'0' = NV Memory Program unready, '1' = NV Memory Program finish,

-NV_N[2:0]: Record NV Memory Program Times

NV_N3	NV_N2	NV_N1	NV_N0	NV Memory Program Times
0	0	0	0	0 time(Default)
0	0	0	1	1 time
0	0	1	1	2 times
0	1	1	1	3 times
1	1	1	1	4 times

-NV_DF:The current status of the NV memory programmed.

NV_DF	Current Status
0	Normal
1	Abnormal EXTC

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	NV_N[3:0]	NV_DF	NV_P	EXTC_F
Power On Sequence	0	0	0	0
S/W Reset	0	0	0	0
H/W Reset	0	0	0	0

6.2.21 EPWRITE: MTP write command (DEh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPWRITE	0	W	1	1	0	1	1	1	1	0	(DEh)
1st parameter	1	W	0	1	0	1	0	1	0	1	55h
2nd parameter	1	W	1	0	1	0	1	0	1	0	AAh
3rd parameter	1	W	0	1	1	0	0	1	1	0	66h

NOTE: "-" Don't care

Description

MTP write command.
Please see ***6.4 MTP Access sequence for program (Data write)*** for more detail.

Restriction

-

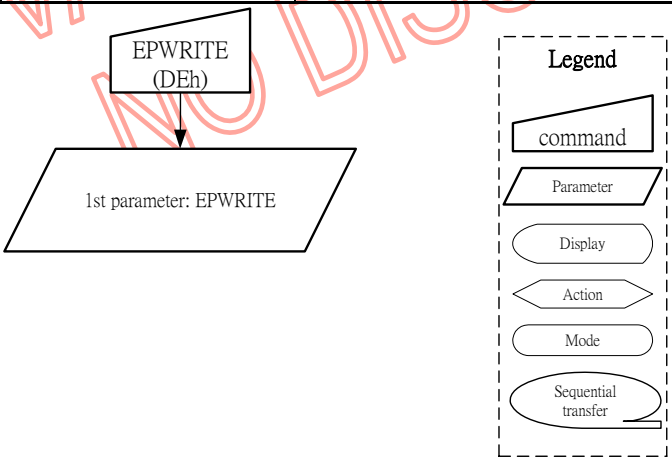
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



6.2.22 DNVRS: NV Memory Control (DFh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DNVRS	0	W	1	1	0	1	1	1	1	1	(DFh)
1st parameter	1	W	-	-	-	-	-	-	-	EN_PDT	

NOTE: "-" Don't care

Description	Enable NV memory programming. 0: Disable 1: Enable
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0
S/W Reset	0
H/W Reset	0

6.2.23 GMCTRP0 : Positive RED Gamma Control (E0h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRP0	0	W	1	1	1	0	0	0	0	0	(E0h)
1st parameter	1	R/W	-	-	VP0[5:0]						
2nd parameter	1	R/W	-	-	VP1[5:0]						
3rd parameter	1	R/W	-	-	VP2[5:0]						
4th parameter	1	R/W	-	-	VP4[5:0]						
5th parameter	1	R/W	-	-	VP6[5:0]						
6th parameter	1	R/W	-	-	-	VP13[4:0]					
7th parameter	1	R/W	-	-	VP20[5:0]						
8th parameter	1	R/W	VP36[3:0]				VP27[3:0]				
9th parameter	1	R/W	-	-	VP43[5:0]						
10th parameter	1	R/W	-	-	-	VP50[4:0]					
11th parameter	1	R/W	-	-	VP57[5:0]						
12th parameter	1	R/W	-	-	VP59[5:0]						
13th parameter	1	R/W	-	-	VP61[5:0]						
14th parameter	1	R/W	-	-	VP62[5:0]						
15th parameter	1	R/W	-	-	VP63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	R-Gamma adjustment registers for the Positive polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
S/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
H/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C

6.2.24 GMCTRN0 : Negative RED Gamma Control (E1h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRN0	0	W	1	1	1	0	0	0	0	1	(E1h)
1st parameter	1	R/W	-	-	VN0[5:0]						
2nd parameter	1	R/W	-	-	VN1[5:0]						
3rd parameter	1	R/W	-	-	VN2[5:0]						
4th parameter	1	R/W	-	-	VN4[5:0]						
5th parameter	1	R/W	-	-	VN6[5:0]						
6th parameter	1	R/W	-	-	-	VN13[4:0]					
7th parameter	1	R/W	-	-	VN20[5:0]						
8th parameter	1	R/W	VN36[3:0]				VN27[3:0]				
9th parameter	1	R/W	-	-	VN43[5:0]						
10th parameter	1	R/W	-	-	-	VN50[4:0]					
11th parameter	1	R/W	-	-	VN57[5:0]						
12th parameter	1	R/W	-	-	VN59[5:0]						
13th parameter	1	R/W	-	-	VN61[5:0]						
14th parameter	1	R/W	-	-	VN62[5:0]						
15th parameter	1	R/W	-	-	VN63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	R-Gamma adjustment registers for the Negative polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
S/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
H/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C

6.2.25 GMCTRP1 : Positive GREEN Gamma Control (E2h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRP1	0	W	1	1	1	0	0	0	1	0	(E2h)
1st parameter	1	R/W	-	-	VP0[5:0]						
2nd parameter	1	R/W	-	-	VP1[5:0]						
3rd parameter	1	R/W	-	-	VP2[5:0]						
4th parameter	1	R/W	-	-	VP4[5:0]						
5th parameter	1	R/W	-	-	VP6[5:0]						
6th parameter	1	R/W	-	-	-	VP13[4:0]					
7th parameter	1	R/W	-	-	VP20[5:0]						
8th parameter	1	R/W	VP36[3:0]				VP27[3:0]				
9th parameter	1	R/W	-	-	VP43[5:0]						
10th parameter	1	R/W	-	-	-	VP50[4:0]					
11th parameter	1	R/W	-	-	VP57[5:0]						
12th parameter	1	R/W	-	-	VP59[5:0]						
13th parameter	1	R/W	-	-	VP61[5:0]						
14th parameter	1	R/W	-	-	VP62[5:0]						
15th parameter	1	R/W	-	-	VP63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	G-Gamma adjustment registers for the Positive polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
S/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
H/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C

6.2.26 GMCTRN1 : Negative GREEN Gamma Control (E3h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRN1	0	W	1	1	1	0	0	0	1	1	(E3h)
1st parameter	1	R/W	-	-	VN0[5:0]						
2nd parameter	1	R/W	-	-	VN1[5:0]						
3rd parameter	1	R/W	-	-	VN2[5:0]						
4th parameter	1	R/W	-	-	VN4[5:0]						
5th parameter	1	R/W	-	-	VN6[5:0]						
6th parameter	1	R/W	-	-	-	VN13[4:0]					
7th parameter	1	R/W	-	-	VN20[5:0]						
8th parameter	1	R/W	VN36[3:0]				VN27[3:0]				
9th parameter	1	R/W	-	-	VN43[5:0]						
10th parameter	1	R/W	-	-	-	VN50[4:0]					
11th parameter	1	R/W	-	-	VN57[5:0]						
12th parameter	1	R/W	-	-	VN59[5:0]						
13th parameter	1	R/W	-	-	VN61[5:0]						
14th parameter	1	R/W	-	-	VN62[5:0]						
15th parameter	1	R/W	-	-	VN63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	G-Gamma adjustment registers for the Negative polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
S/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
H/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C

6.2.27 GMCTRP2 : Positive BLUE Gamma Control (E4h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRP2	0	W	1	1	1	0	0	1	0	0	(E4h)
1st parameter	1	R/W	-	-	VP0[5:0]						
2nd parameter	1	R/W	-	-	VP1[5:0]						
3rd parameter	1	R/W	-	-	VP2[5:0]						
4th parameter	1	R/W	-	-	VP4[5:0]						
5th parameter	1	R/W	-	-	VP6[5:0]						
6th parameter	1	R/W	-	-	-	VP13[4:0]					
7th parameter	1	R/W	-	-	VP20[5:0]						
8th parameter	1	R/W	VP36[3:0]				VP27[3:0]				
9th parameter	1	R/W	-	-	VP43[5:0]						
10th parameter	1	R/W	-	-	-	VP50[4:0]					
11th parameter	1	R/W	-	-	VP57[5:0]						
12th parameter	1	R/W	-	-	VP59[5:0]						
13th parameter	1	R/W	-	-	VP61[5:0]						
14th parameter	1	R/W	-	-	VP62[5:0]						
15th parameter	1	R/W	-	-	VP63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	B-Gamma adjustment registers for the Positive polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
S/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C
H/W Reset	00	07	0C	0B	13	15	0C	7A	16	07	12	17	0F	26	2C

6.2.28 GMCTRN2 : Negative BLUE Gamma Control (E5h)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GMCTRN2	0	W	1	1	1	0	0	1	0	1	(E5h)
1st parameter	1	R/W	-	-	VN0[5:0]						
2nd parameter	1	R/W	-	-	VN1[5:0]						
3rd parameter	1	R/W	-	-	VN2[5:0]						
4th parameter	1	R/W	-	-	VN4[5:0]						
5th parameter	1	R/W	-	-	VN6[5:0]						
6th parameter	1	R/W	-	-	-	VN13[4:0]					
7th parameter	1	R/W	-	-	VN20[5:0]						
8th parameter	1	R/W	VN36[3:0]				VN27[3:0]				
9th parameter	1	R/W	-	-	VN43[5:0]						
10th parameter	1	R/W	-	-	-	VN50[4:0]					
11th parameter	1	R/W	-	-	VN57[5:0]						
12th parameter	1	R/W	-	-	VN59[5:0]						
13th parameter	1	R/W	-	-	VN61[5:0]						
14th parameter	1	R/W	-	-	VN62[5:0]						
15th parameter	1	R/W	-	-	VN63[5:0]						

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description	B-Gamma adjustment registers for the Negative polarity. *Note: See section 5.9 for details of the setting method.*
Restriction	-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value														
	1'st	2'nd	3'rd	4'th	5'th	6'th	7'th	8'th	9'th	10'th	11'th	12'th	13'th	14'th	15'th
Power On Sequence	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
S/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C
H/W Reset	10	16	2D	18	1D	18	26	58	30	0A	1C	24	30	35	3C

6.2.29 GAM_R_SEL : Gamma Selection (EAh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GAM_R_SEL	0	W	1	1	1	0	1	0	1	0	(EAh)
Parameter	1	R/W	-	-	-	-	-	-	-	GAM_R_SEL	

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

GAM_R_SEL: Gamma selection
0: Gamma control by GC0~GC3 default value. (Cooperate with R26h register)
1: Gamma control by RE0 ~ RE5 registers value.

Gamma control by	GAM_R_SEL=1	GAM_R_SEL=0
EXTC=Low	GC0~GC3 default value.	GC0~GC3 default value.
EXTC=High	RE0 ~ RE5 registers value.	GC0~GC3 default value.

Restriction

-

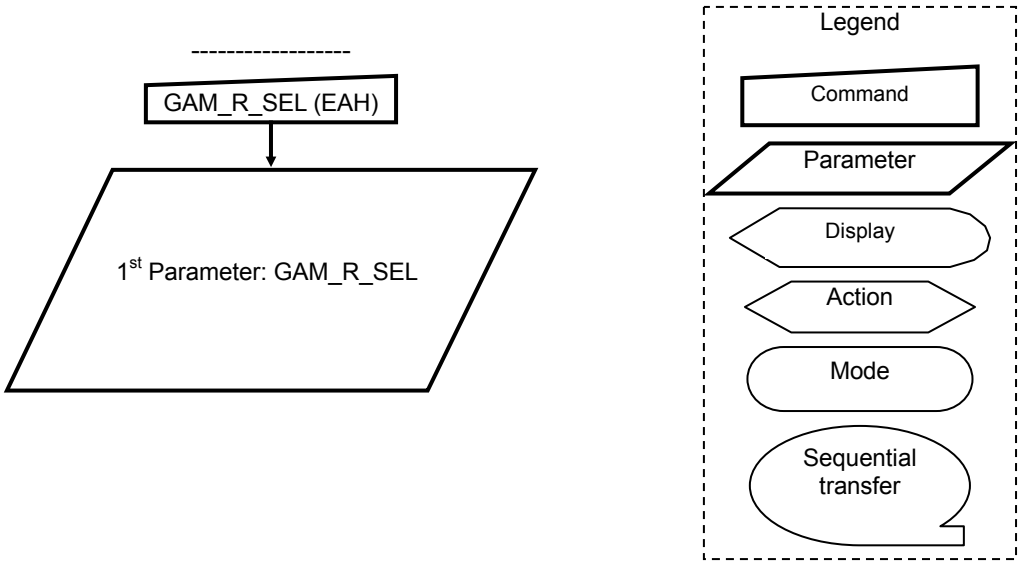
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GAM_R_SEL
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



6.2.30 TSTGVDD : GVDD output control (EBh)

Instruction	D/CX	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TSTGVDD	**0**	**W**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**(EBh)**
Parameter	**1**	**R/W**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**TEST_GVDD**	

NOTE: "-" Don't care

NOTE: The dummy clock must be inserted when read the parameters

Description

TEST_GVDD :
0: pin "GVDD" output = Hi-Z (default)
1: pin "GVDD" output = internal GVDD

Restriction

-

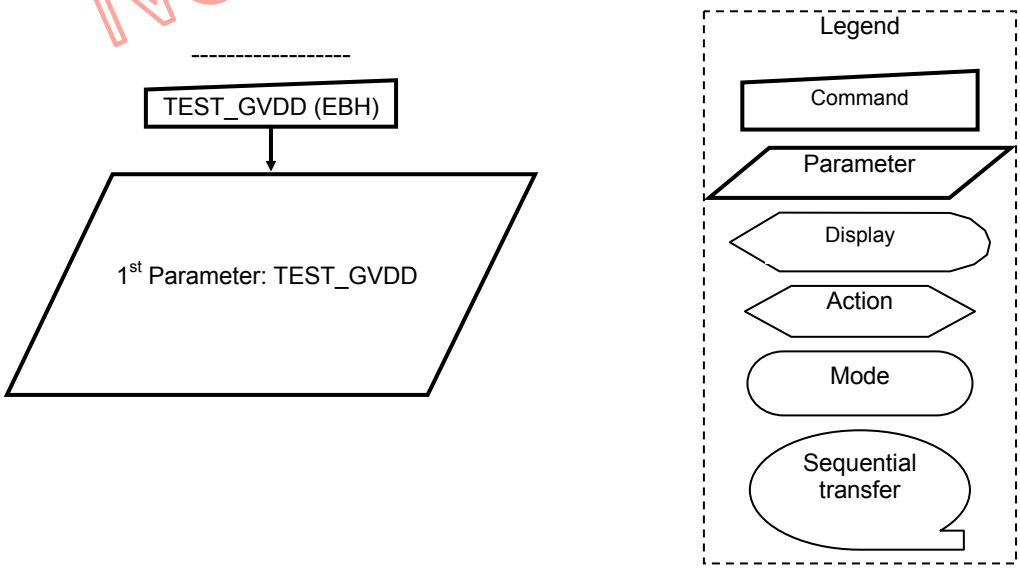
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	TEST_GVDD
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



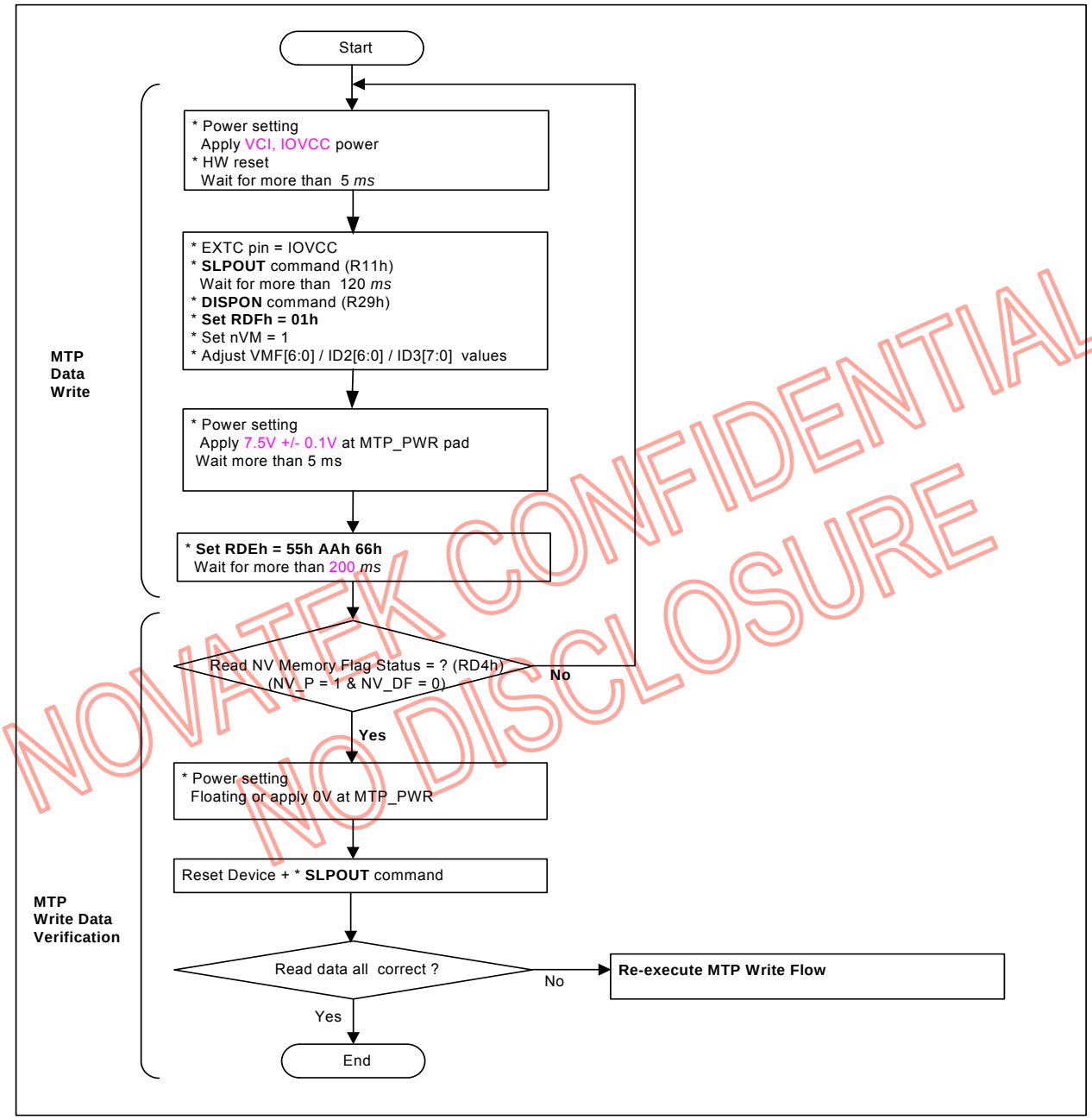
6.2.31 Testing Commands (F0~FFh)

Those instructions are testing instructions for Novatek. Please do not use it.

6.3 RESET TABLE (Default value)

Item		After Power On	After Hardware Reset	After Software Reset
Frame memory		Random	No Change	No Change
Sleep In/Out		In	In	In
Display On/Off		Off	Off	Off
Display mode (normal/partial)		Normal	Normal	Normal
Display Inversion On/Off		Off	Off	Off
Display Idle Mode On/Off		Off	Off	Off
Column: Start Address (XS)		0000h	0000h	0000h
Column: End Address (XE)	GM="00"	00EFh (239d)	00EFh (239d)	00EFh (239d) (when MV=0) 01AFh (431d) (when MV=1)
	GM="01"	00EFh (239d)	00EFh (239d)	00EFh (239d) (when MV=0) 018Fh (399d) (when MV=1)
	GM="10"	00EFh (239d)	00EFh (239d)	00EFh (239d) (when MV=0) 013Fh (319d) (when MV=1)
Row: Start Address (YS)		0000h	0000h	0000h
Row: End Address (YE)	GM="00"	01AFh (431d)	01AFh (431d)	01AFh (431d) (when MV=0) 00EFh (239d) (when MV=1)
	GM="01"	018Fh (399d)	018Fh (399d)	018Fh (399d) (when MV=0) 00EFh (239d) (when MV=1)
	GM="10"	013Fh (319d)	013Fh (319d)	013Fh (319d) (when MV=0) 00EFh (239d) (when MV=1)
Partial: Start Address (PSL)		0000h	0000h	0000h
Partial: End Address (PEL)		01AFh	01AFh	01AFh
Scroll: Vertical scrolling		Off	Off	Off
Scroll: Top Fixed Area (TFA)		0000h	0000h	0000h
Scroll: Scroll Area (VSA)	GM="00"	01B0h	01B0h	01B0h
	GM="01"	0190h	0190h	0190h
	GM="10"	0140h	0140h	0140h
Scroll: Bottom Fixed Area (BFA)		0000h	0000h	0000h
Scroll Start Address (SSA)		0000h	0000h	0000h
Tearing: On/Off		Off	Off	Off
Tearing Effect Mode		00h (Mode1)	00h (Mode1)	00h (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)		0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format (3Ah)		6d(18-Bits/Pixel)	6d(18-Bits/Pixel)	No Change
RDDPM (0Ah)		08h	08h	08h
RDDMADCTR (0Bh)		00h	00h	No Change
RDDCOLMOD (0Ch)		6h(18-Bits/Pixel)	6h(18-Bits/Pixel)	No Change
RDDIM (0Dh)		00h	00h	00h
RDDSM (0Eh)		00h	00h	00h
ID1 (DAh)		38h	38h	38h
ID2 (DBh)		MTP value	MTP value	MTP value
ID3 (DCh)		MTP value	MTP value	MTP value

6.4 MTP Access Sequence for Program (Data write)



6.5 INSTRUCTION SETUP FLOW

6.5.1 Initializing with the Built-in Power Supply Circuits

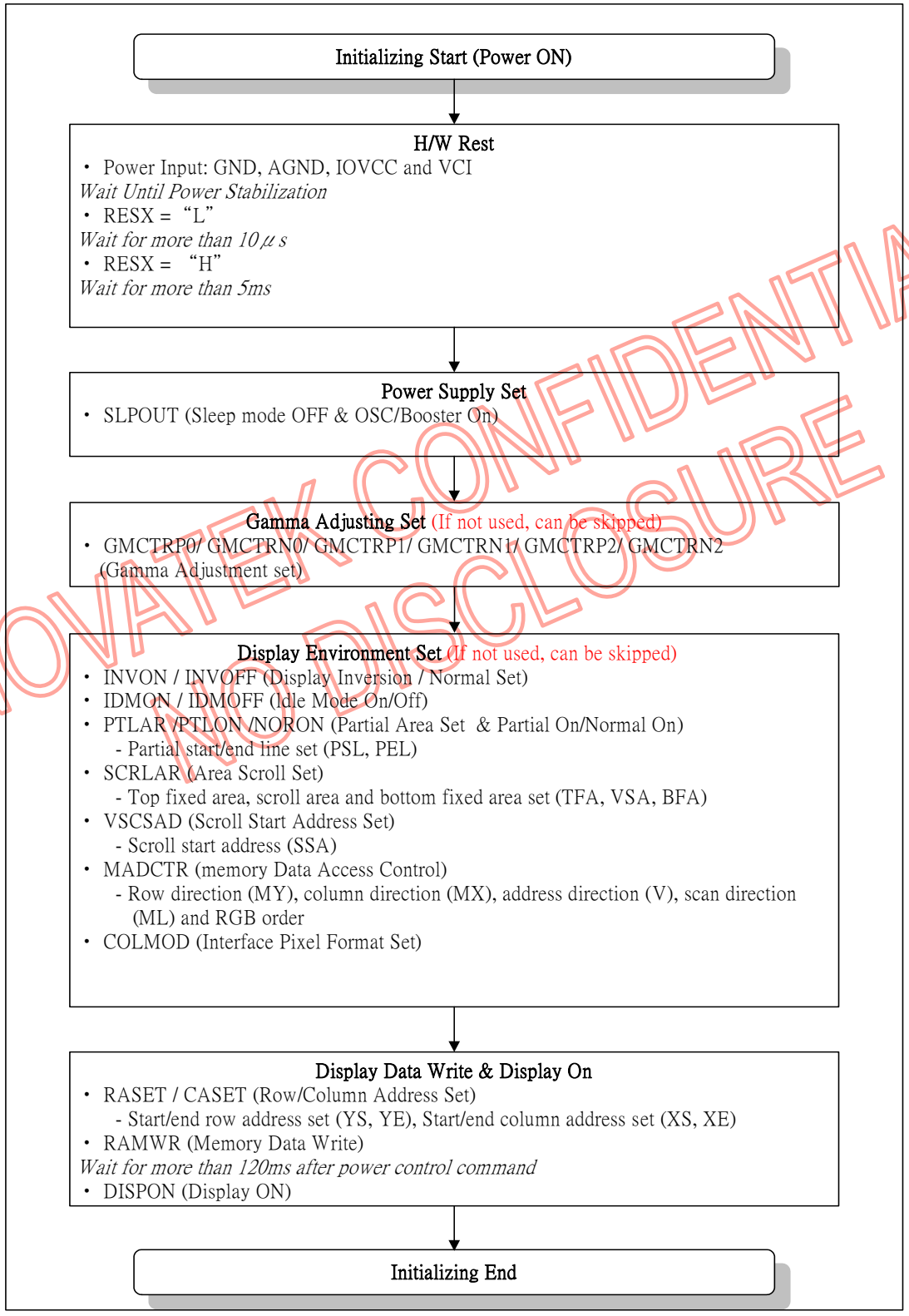


Fig. 6.5.1 Initializing with the built-in power supply circuits

6.5.2 Power OFF Sequence

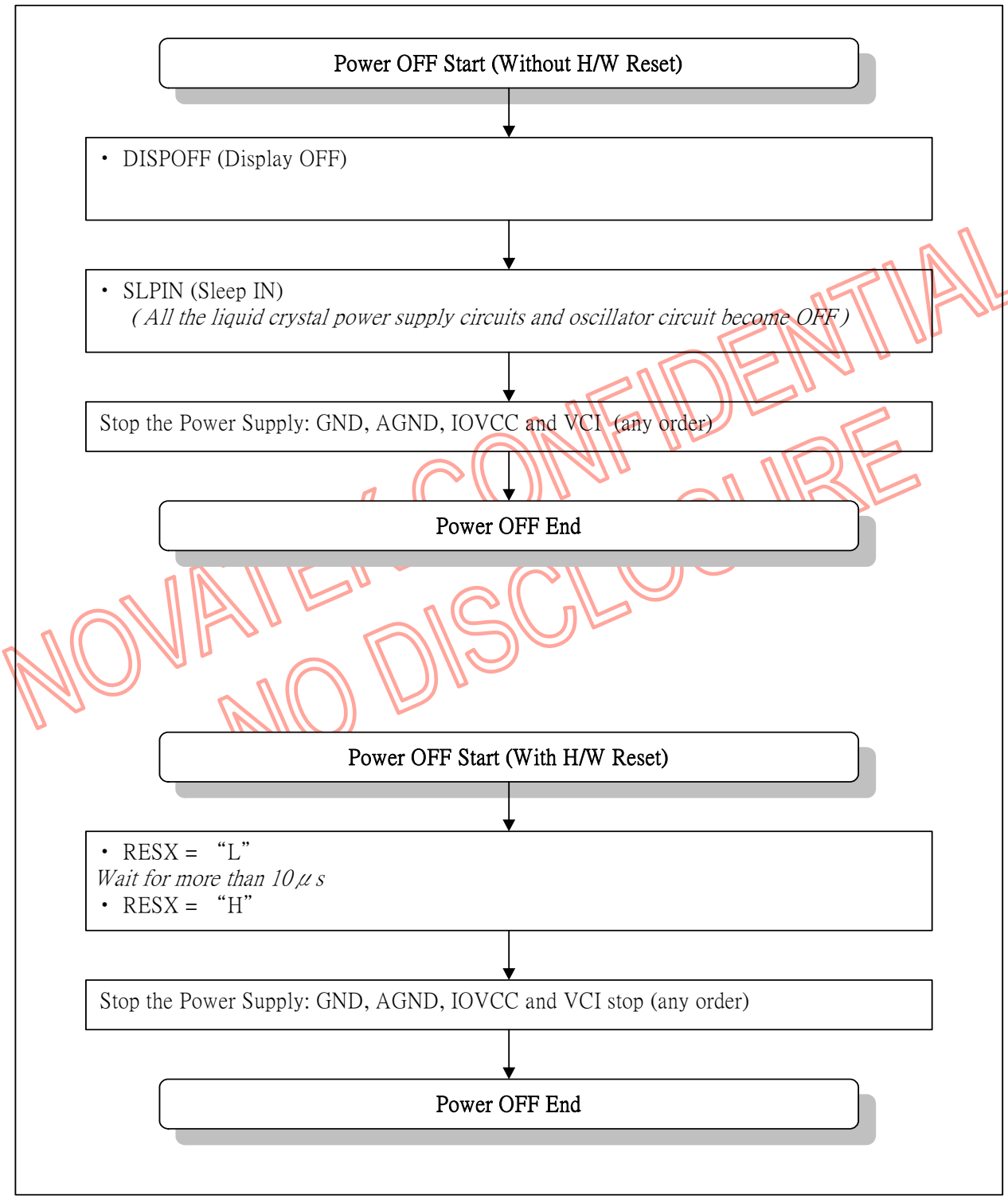


Fig. 6.5.2 Power OFF sequence

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	VCI	-0.3 ~ +4.6	V
Supply voltage (Logic)	IOVCC	- 0.3 ~ +4.6	V
Supply voltage (Digital)	VDD	-0.3 ~ +4.6	V
Driver supply Voltage	VGH-VGL	-0.3 ~ +33.0	V
Logic Input voltage range	V_{IN}	- 0.3 ~ IOVCC + 0.3	V
Logic Output voltage range	V_O	- 0.3 ~ IOVCC + 0.3	V
Operating temperature range	T_{OPR}	-40 ~ +85	℃
Storage Temperature range	T_{STG}	-55 ~ +125	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 ESD PROTECTION LEVEL

Table 7.2.1 ESD models.

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2500	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 250	V

7.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

7.4 LIGHT SENSITIVITY

The operation of the IC will not be materially altered by incident light.

7.5 MAXIMUM SERIES RESISTANCE

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in ***Table 7.5.1.***

Table 7.5.1 Maximum series resistance on module.

Name	Type	Maximum Series Resistance	Unit
VCI	Power supply	10	Ω
VCILVL	Power supply	20	Ω
VR	Power supply	10	Ω
VDD	Power supply	20	Ω
IOVCC	Power supply	20	Ω
AGND	Power supply	10	Ω
GND	Power supply	20	Ω
RGND	Power supply	20	Ω
MTP_PWR	Power supply	10	Ω
GM1-0, IM2-0, P68, 4WSPI,	Input	200	Ω
EXTC, RCM	Input	100	Ω
RESX	Input	100	Ω
CSX (SCEX)	Input	100	Ω
D/CX	Input	100	Ω
WRX	Input	100	Ω
RDX	Input	100	Ω
TE	Output	100	Ω
D17 to D0	Input / Output	100	Ω
SDA	Input / Output	100	Ω
PCLK, DE, VS, HS	Input	100	Ω
SMX, SMY, SRGB, SHUT, IDM, REV, RL, TB	Input	100	Ω
GVDD	Capacitor connection	20	Ω
VREF	Capacitor connection	20	Ω
VCOMH, VCOML	Capacitor connection	20	Ω
AVDD	Capacitor connection	20	Ω
VGH	Capacitor connection	20	Ω
VGL	Capacitor connection	20	Ω
VCL	Capacitor connection	20	Ω
C11+/-, C12+/-	Capacitor connection	20	Ω
C13+/-, C21+/-, C22+/-, C23+/-	Capacitor connection	20	Ω

7.6 DC CHARACTERISTICS

7.6.1 Basic Characteristics

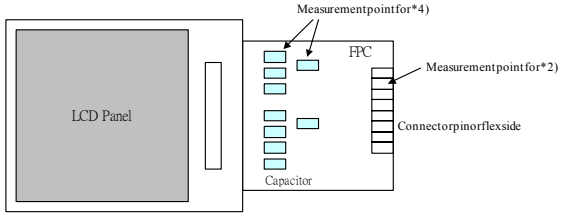
Parameter	Symbol	Conditions	Specification TYP			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI, VCILVL	Operating Voltage	2.5	2.75	3.1	V	(*1)
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.1	V	(*1)
Digital Operating voltage	VDD	Digital supply voltage	1.5	1.8	2.0	V	(*1)
Input /Output							
Logic High level input voltage	VIH		0.7*IOVCC	-	IOVCC	V	(*1, *2, *3)
Logic Low level input voltage	VIL	-	GND	-	0.3*IOVCC	V	(*1, *2, *3)
Logic High level output voltage	VOH	IOH = -1.0mA	0.8*IOVCC	-	IOVCC	V	(*1, *2, *3)
Logic Low level output voltage	VOL	IOL = 1.0mA	GND	-	0.2*IOVCC	V	(*1, *2, *3)
Logic High level input current	IIH				1	uA	(*1, *2, *3)
Logic Low level input current	IIL		-1			uA	(*1, *2, *3)
Logic Input leakage current	IIL	Vin = IOVCC or GND	-0.1	-	+0.1	uA	(*1, *2, *3)
VCOM Operation							
VCOM High voltage	VCOMH	Ccom=61nF	2.5		5.0	V	(*2)
VCOM Low voltage	VCOML		-2.5		0.0	V	(*2)
VCOM Amplitude voltage	|VCOMH-VCOML|		4.0		6.0	V	(*2)
Source Driver							
Source output range	VS		0.1		AVDD-0.1	V	(*4)
Gamma reference voltage	GVDD		3.425		5.0	V	(*4)
Source output settling time	Tr	Below with 99% precision		12	20	us	(*4)
Output deviation voltage (Source output channel)	V,dev	Sout >= 4.2V, Sout <= 0.8V			30	mV	(*4)
		4.2V>Sout>0.8V			20	mV	
Output offset voltage	VOFSET				35	mV	(*4)
Booster Operation							
1st Booster (AVDD) voltage	AVDD		5.0		6.0	V	(*1, *2)
1st Booster (AVDD) drop voltage	At VCI = 2.8V	loading=1mA			5	%	(*1, *2)
2nd Booster (VGH) voltage	VGH		10		15	V	(*1, *2)
2nd Booster (VGH) drop voltage	At VCI = 2.8V	loading=0.1mA			5	%	(*1, *2)
2nd Booster (VGL) voltage	VGL		-12.5		-4.5	V	(*1, *2)
2nd Booster (VGL) drop voltage	At VCI = 2.8V	loading=0.1mA			5	%	(*1, *2)
2nd Booster (VCL) voltage	VCL		-2.5		-3.1	V	(*1, *2)
2nd Booster (VCL) drop voltage	At VCI = 2.8V	loading=0.1mA			5	%	(*1, *2)

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)

Note 2, When the measurements are performed with LCD module, Measurement Points are like below.

Note 3: CSX, RDX, WRX, D[17:0], D/CX, RESX, IM2, IM1, IM0, TE

Note 4, Source channel loading= 40pF/channel, Gate channel loading= 100pF/channel,



7.6.2 Current Consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						IOVCC (mA)	VCI (mA)	IOVCC (mA)	VCI (mA)
Host interface NOT active	- Normal Mode On - Partial- Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	TBD	Note 1	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 2	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 3	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 4	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 5	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	45Hz	TBD	Note 5	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode Off - Partial Mode On (64 lines) - Idle Mode Off - Sleep Out Mode	60Hz	TBD	Grey Levels	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode Off - Partial Mode On(64 lines) - Idle Mode On - Sleep Out Mode	45Hz	TBD	Note 6	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 7	X;X;X	TBD	TBD	TBD	TBD
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	TBD	TBD	TBD	TBD
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	TBD	262k Colors NOTE 8 CPU Access @ 15fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
					1;1;1	TBD	TBD	TBD	TBD
				262k Colors NOTE 8 CPU Access @ 25fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
					1;1;1	TBD	TBD	TBD	TBD

NOTE: X Do not care

1. All pixels black

2. Checker board one by one

3. Checker board 4 by 4

4. Grey-scale from top to bottom

5. 20% Black, 80%White

6. Black & White Checker board 8 by 8.

7. Absolute Worst Case Patterns: Defined by Display Supplier

8. Absolute Worst Case Patterns and Sequences: Defined by Display Supplier

9. Absolute worst case VCI current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

10. Absolute worst case IOVCC current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

11. Inrush currents are not included in current consumption values

Typical Case:	Worst Case
TA = 25ºC	TA = -30ºC to 70ºC
VCI = 2.75V	VCI =2.5V to 3.1V
IOVCC = 1.8V	IOVCC=1.65V to 3.1V
	Includes Process Variation

7.7 AC CHARACTERISTICS

7.7.1 Parallel Interface Characteristics (80-series MPU)

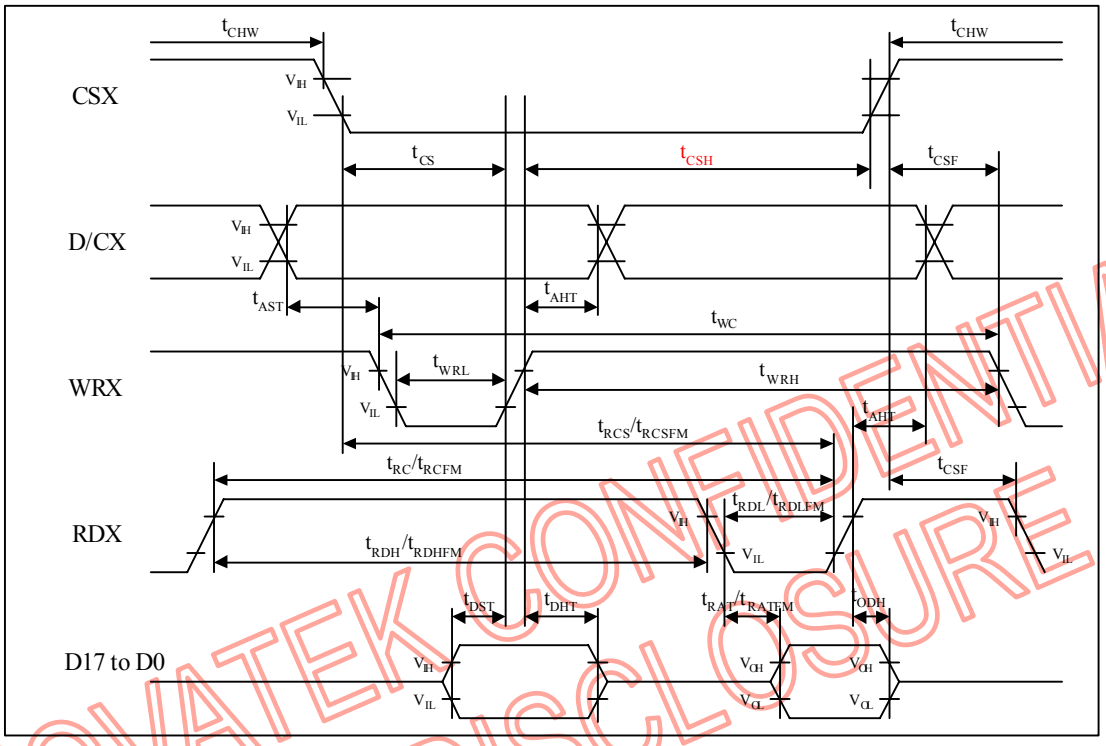


Fig. 7.7.1 Parallel Interface characteristics (80-series MPU)

Table .7.7.1: AC Characteristics for Parallel Interface 18, 9, 16, 8-bits bus (80-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	tAST	Address setup time	0		ns	-
	tAHT	Address hold time (Write/Read)	2		ns	
CSX	tCHW	Chip select "H" pulse width	0		ns	
	tCS	Chip select setup time (Write)	20		ns	
	tRCS	Chip select setup time (Read ID)	35		ns	
	tRCSFM	Chip select setup time (Read FM)	320		ns	
	tCSF	Chip select wait time (Write/Read)	10		ns	
	tCSH	Chip select hold time	10		ns	
WRX	tWC	Write cycle	65		ns	
	tWRH	Control pulse "H" duration	18		ns	
	tWRL	Control pulse "L" duration	35		ns	
RDX (ID)	tRC	Read cycle (ID)	160		ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90		ns	
	tRDL	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	tRCFM	Read cycle (FM)	450		ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	250		ns	
	tRDLFM	Control pulse "L" duration (FM)	170		ns	
D[23:0]	tDST	Data setup time	25		ns	
	tDHT	Data hold time	10		ns	
	tRAT	Read access time (ID)		40	ns	
	tRATFM	Read access time (FM)		150	ns	
	tODH	Output disable time	20	80	ns	

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.7.2 Parallel Interface Characteristics (68-series MPU)

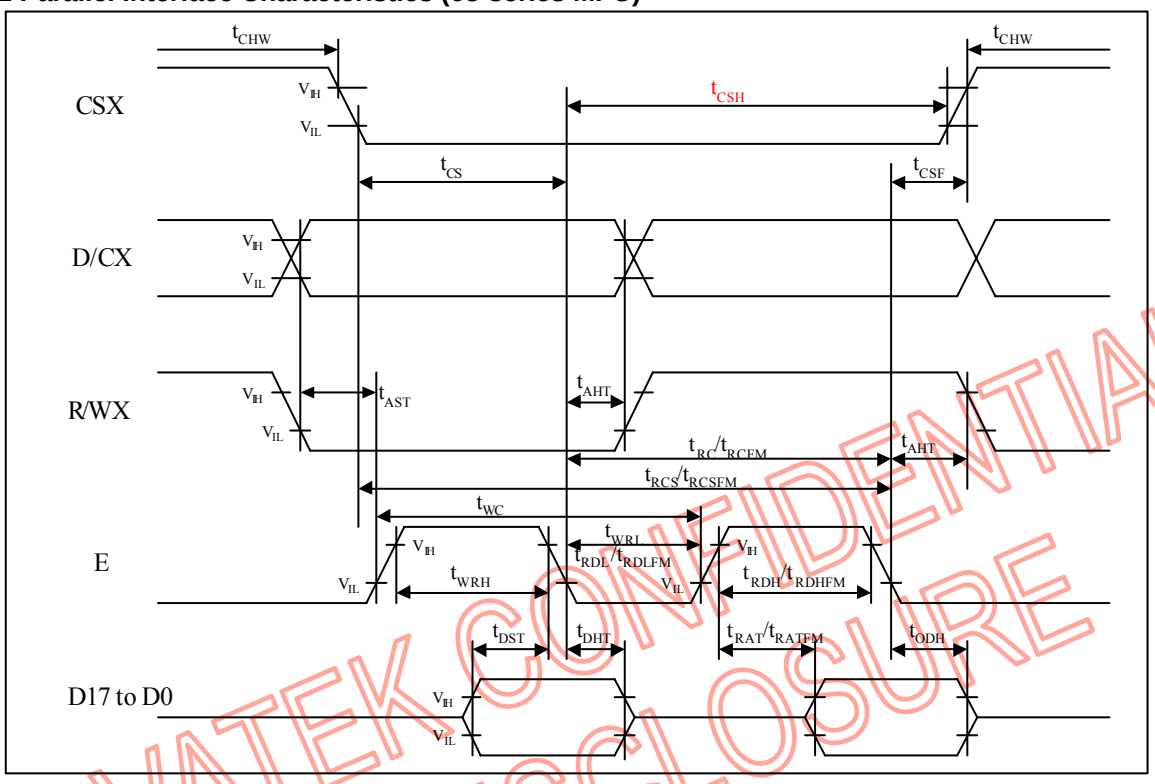


Fig. 7.7.2 Parallel Interface characteristics (68-series MPU)

Table .7.7.2: AC Characteristics for Parallel Interface 18, 9, 16, 8-bits bus (68-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	tAST	Address setup time	0		ns	-
	tAHT	Address hold time (Write/Read)	2		ns	
CSX	tCHW	Chip select "H" pulse width	0		ns	
	tCS	Chip select setup time (Write)	20		ns	
	tRCS	Chip select setup time (Read ID)	35		ns	
	tRCSFM	Chip select setup time (Read FM)	320		ns	
	tCSF	Chip select wait time (Write/Read)	10		ns	
	tCSH	Chip select hold time	10		ns	
WRX	tWC	Write cycle	65		ns	
	tWRH	Control pulse "H" duration	35		ns	
	tWRL	Control pulse "L" duration	18		ns	
RDX (ID)	tRC	Read cycle (ID)	160		ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	45		ns	
	tRDL	Control pulse "L" duration (ID)	90		ns	
RDX (FM)	tRCFM	Read cycle (FM)	450		ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	170		ns	
	tRDLFM	Control pulse "L" duration (FM)	250		ns	
D[23:0]	tDST	Data setup time	25		ns	
	tDHT	Data hold time	10		ns	
	tRAT	Read access time (ID)		40	ns	
	tRATFM	Read access time (FM)		150	ns	
	tODH	Output disable time	20	80	ns	

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.7.3 Serial Interface Characteristics (3-Pin Serial)

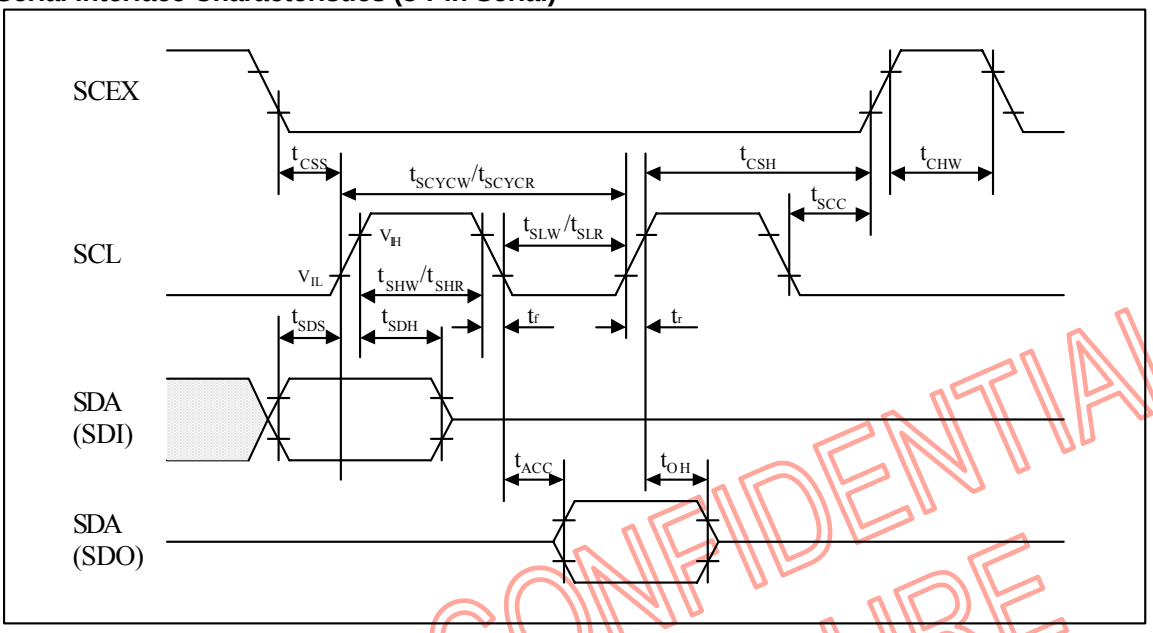


Fig. 7.7.3 3-pin serial interface characteristics

Table .7.7.3: AC Characteristics for Serial Interface (3-pin)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	tCSS	Chip select setup time	20		ns	
	tCSH	Chip select hold time	60		ns	
	tSCC	Chip select delay time	20		ns	
	tCHW	Chip H" pulse width	40		ns	
SCL	tSCYCW	Serial clock cycle (Write)	100		ns	
	TSHW	SCL H" pulse width (Write)	40		ns	
	tSLW	SCL L" pulse width (Write)	40		ns	
	tSCYCR	Serial clock cycle (Read GRAM)	350		ns	
	TSHR	SCL H" pulse width (Read GRAM)	150		ns	
	tSLR	SCL L" pulse width (Read GRAM)	150		ns	
	tSCYCR	Serial clock cycle (Read ID)	100		ns	
	TSHR	SCL H" pulse width (Read ID)	40		ns	
	tSLR	SCL L" pulse width (Read ID)	40		ns	
SDA (DIN) (DOUT)	tSDS	Data setup time	30		ns	
	tSDH	Data hold time	30		ns	
	tACC	Access time		130	ns	
	tOH	Output disable time	5		ns	

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.7.4 Serial Interface Characteristics (4-Pin Serial)

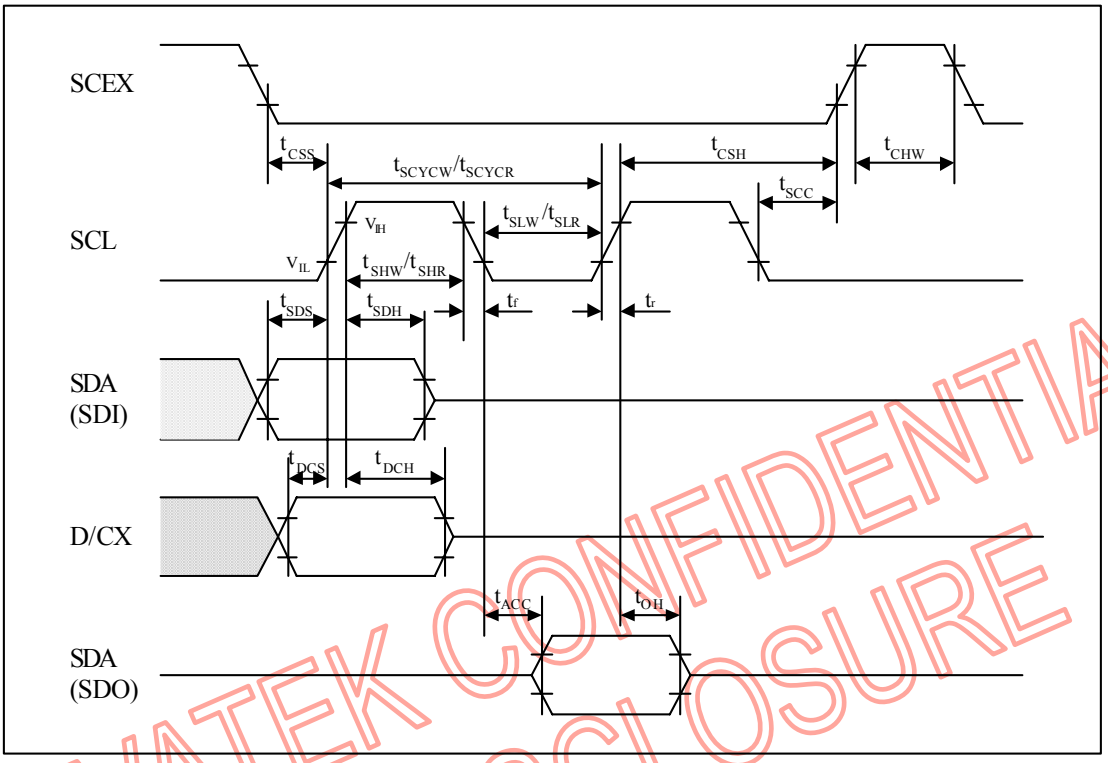


Fig. 7.7.4 4-pin serial interface characteristics

Table .7.7.4: AC Characteristics for Serial Interface (4-pin)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	tCSS	Chip select setup time	20		ns	
	tCSH	Chip select hold time	60		ns	
	tSCC	Chip select delay time	20		ns	
	tCHW	Chip H" pulse width	40		ns	
SCL	tSCYCW	Serial clock cycle (Write)	100		ns	
	TSHW	SCL H" pulse width (Write)	40		ns	
	tSLW	SCL L" pulse width (Write)	40		ns	
	tSCYCR	Serial clock cycle (Read GRAM)	350		ns	
	TSHR	SCL H" pulse width (Read GRAM)	150		ns	
	tSLR	SCL L" pulse width (Read GRAM)	150		ns	
	tSCYCR	Serial clock cycle (Read ID)	100		ns	
	TSHR	SCL H" pulse width (Read ID)	40		ns	
	tSLR	SCL L" pulse width (Read ID)	40		ns	
D/CX	tDCS	D/CX setup time	30		ns	
	tDCH	D/CX hold time	30		ns	
SDA (DIN) (DOUT)	tSDS	Data setup time	30		ns	
	tSDH	Data hold time	30		ns	
	tACC	Access time		130	ns	
	tOH	Output disable time	5		ns	

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.7.5 RGB Interface Characteristics

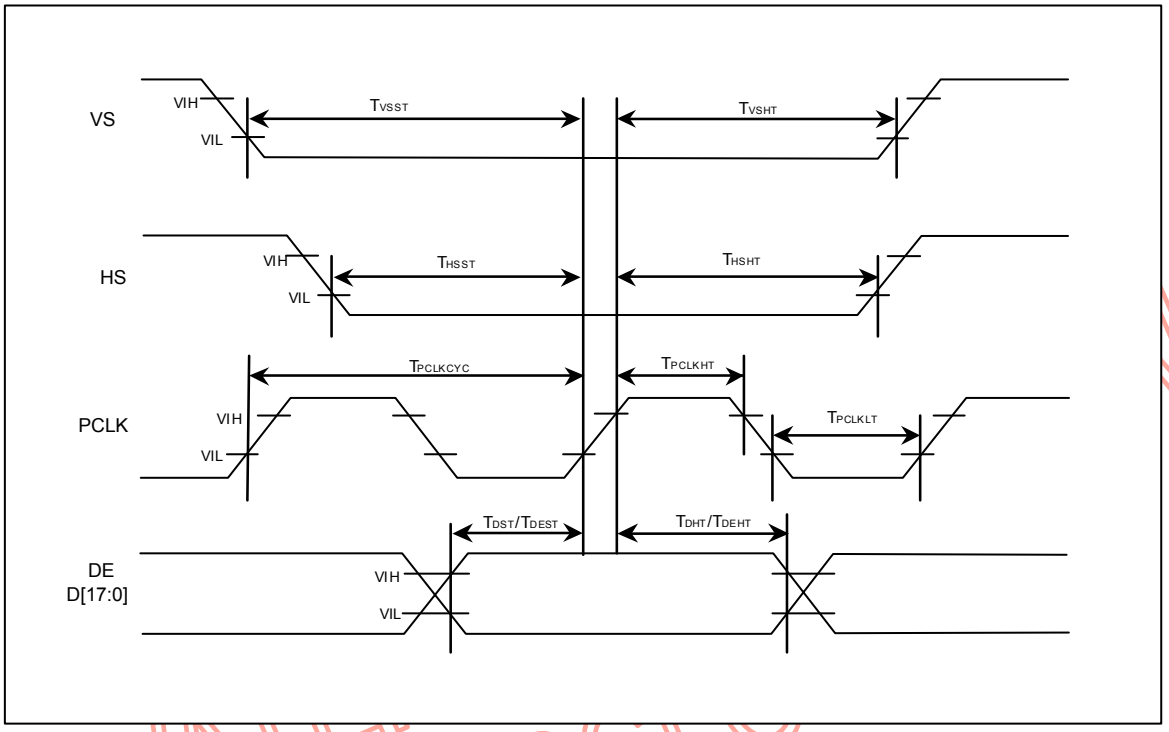


Fig. 7.7.5 RGB Interface characteristics

Table .7.7.5: General Timing for RGB Interface

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VS	TVSST	Vertical sync. setup time	0		ns	
	TVSHT	Vertical sync. hold time	10		ns	
HS	THSST	Horizontal sync. setup time	0		ns	
	THSHT	Horizontal sync. hold time	10		ns	
DE	TDEST	Data enable setup time	10		ns	
	TDEHT	Data enable hold time	25		ns	
D[17:0]	TDST	Data setup time	10		ns	
	TDHT	Data hold time	25		ns	
PCLK (1-transfer/pixel)	TPCLKCYC	Pixel clock cycle	100		ns	
	TPCLKHT	Pixel clock high pulse width	25		ns	
	TPCLKLT	Pixel clock low pulse width	25		ns	
PCLK (3-transfer/pixel)	TPCLKCYC	Pixel clock cycle	60		ns	
	TPCLKHT	Pixel clock high pulse width	25		ns	
	TPCLKLT	Pixel clock low pulse width	25		ns	

Note 1: IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

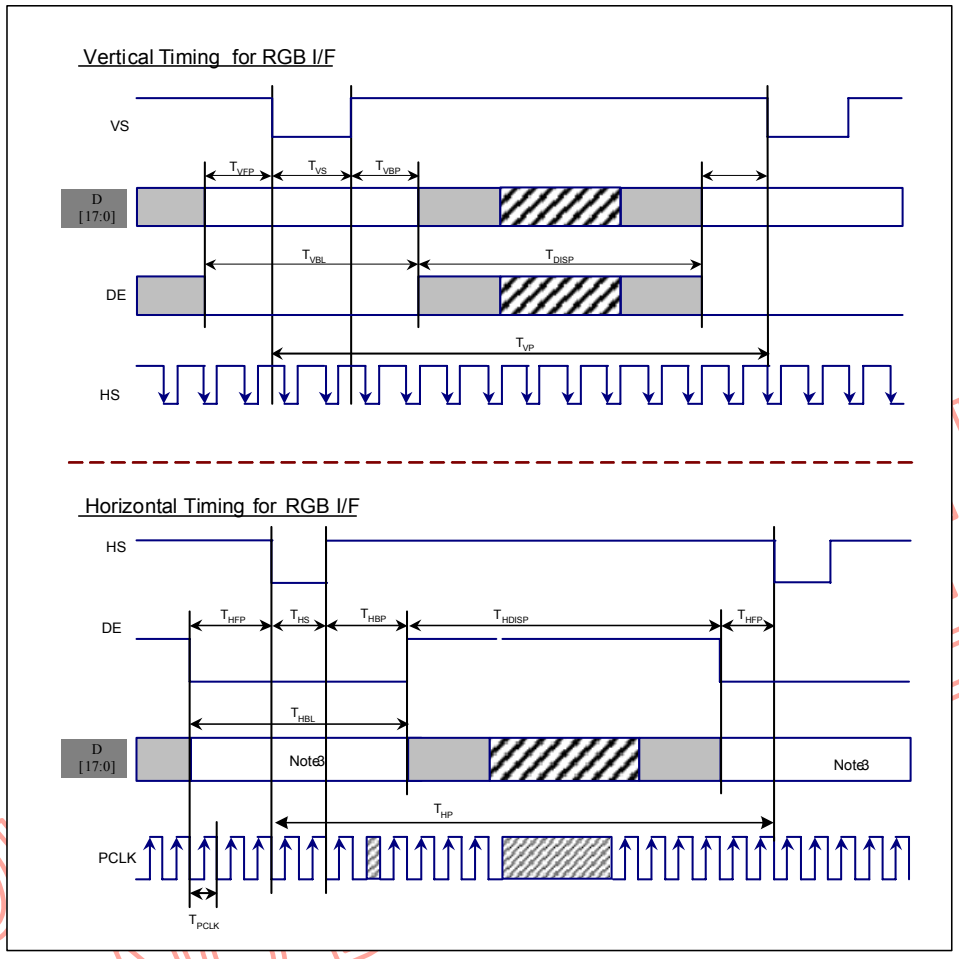


Fig 7.7.6 Vertical and Horizontal timing for RGB I/F

Table .7.7.6: Vertical and Horizontal Timing for RGB Interface

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}		438		442	HS
Vertical low pulse width	T_{VS}		2		4	HS
Vertical front porch	T_{VFP}		2		4	HS
Vertical back porch	T_{VBP}		2		4	HS
Vertical data start line		$T_{VS} + T_{VBP}$	4		8	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6		10	HS
Vertical active area	T_{VDISP}			432		HS
Vertical refresh rate	TVRR	Frame rate		55		Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}		272		512	PCLK
Horizontal low pulse width	T_{HS}		2		256	PCLK
Horizontal front porch	T_{HFP}		2		256	PCLK
Horizontal back porch	T_{HBP}		2		256	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	30		256	PCLK
		$ff_{HS} + f_{HBP}$	1.0			μs
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	32		256	PCLK
Horizontal active area	T_{HDISP}			240		PCLK
Pixel clock cycle	$T_{PCLKCYC}$		80		150	ns
When TVRR=55Hz	$f_{PCLKCYC}$		6.55		12.45	MHz

Note 1. IOVCC=1.65 to 3.1V, VCI=2.5 to 3.1V, AGND=GND=RGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.

7.7.6 Reset Input Timing

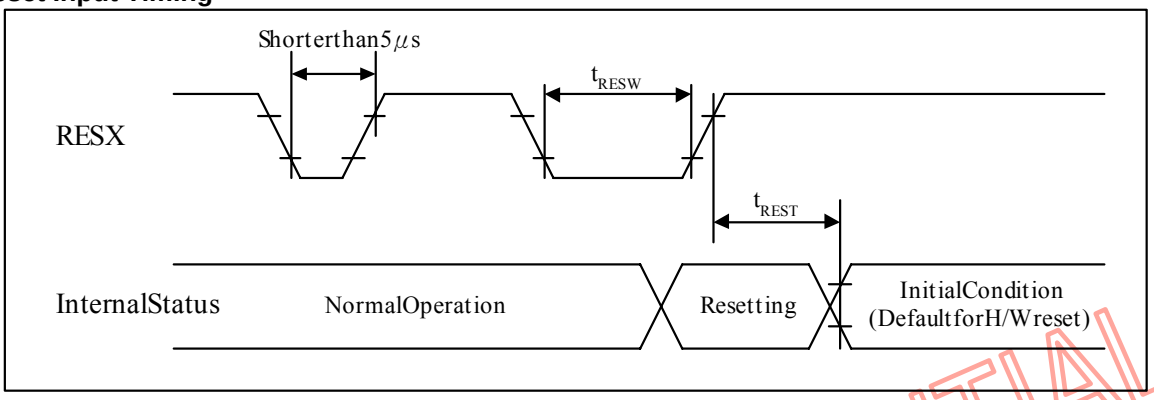


Fig. 7.7.8 Reset input timing

(AGND=CGND=VGS=

GND=0V, IOVCC=1.6V to 3.0V, VCI=2.6V to 3.0V,Ta = -30 to 70° C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	μs
tREST	*2) Reset complete time	RESX	-	-	5	When reset applied during Sleep In mode	ms
		RESX		-	120	When reset applied during Sleep Out mode	ms

NOTE:

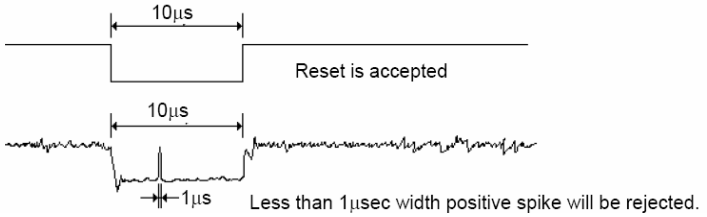
1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5μs	*Reset Rejected*
Longer than 10μs	*Reset*
Between 5μs and 10μs	*Reset Start*

2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

3) During Reset Complete Time, ID2,ID3 and VCM[5:0] value in MTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

4) Spike Rejection also applies during a valid reset pulse as shown below:

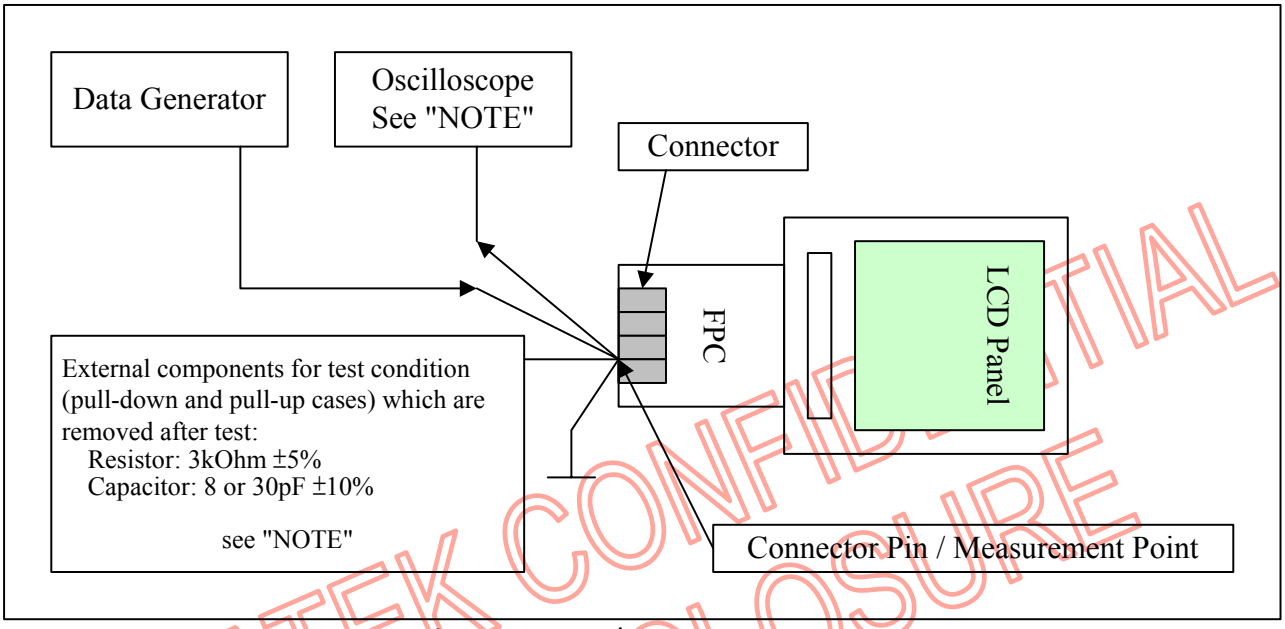


5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7.7.7 Measurement Conditions

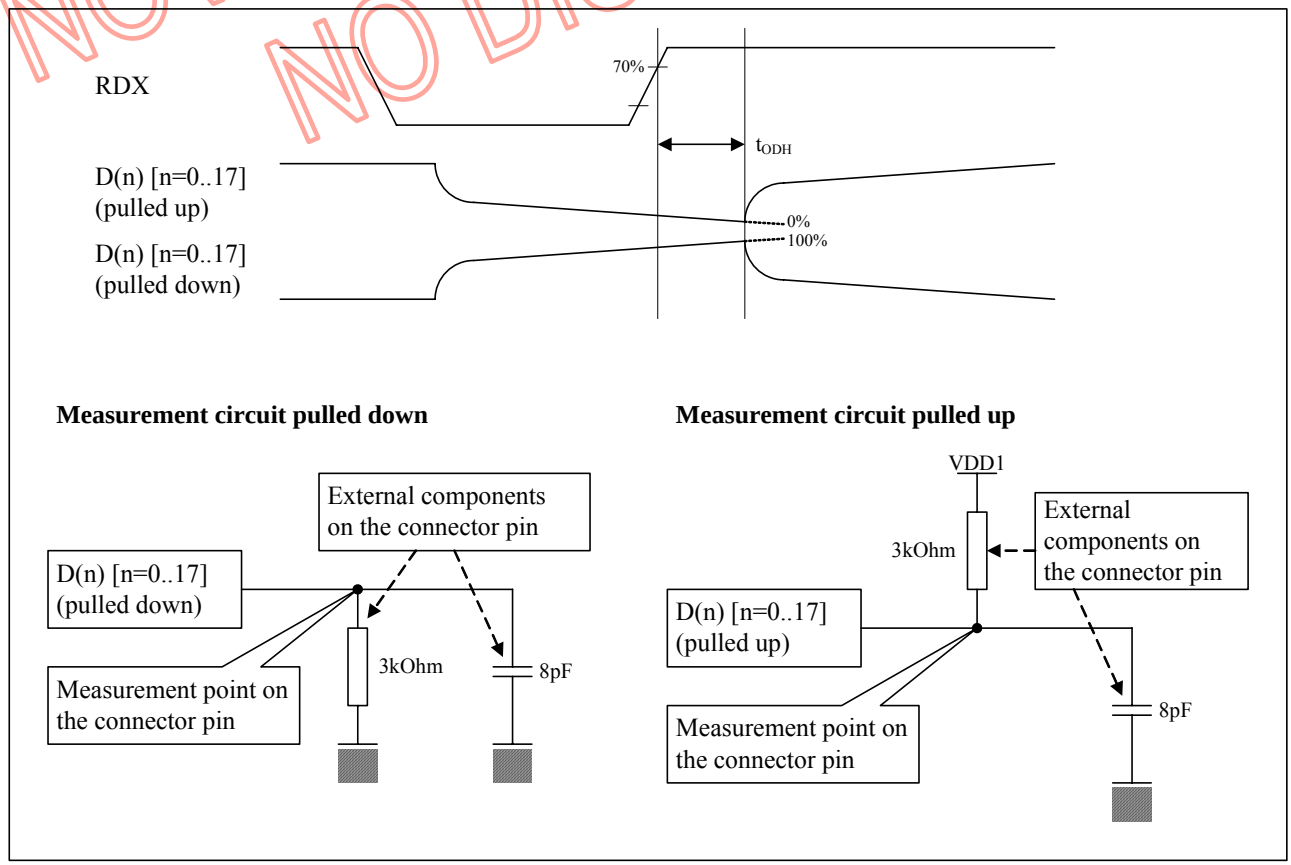
7.7.7.1 TRAT, TRATFM, TODH MEASUREMENT CONDITION

Measurement Condition Set-up

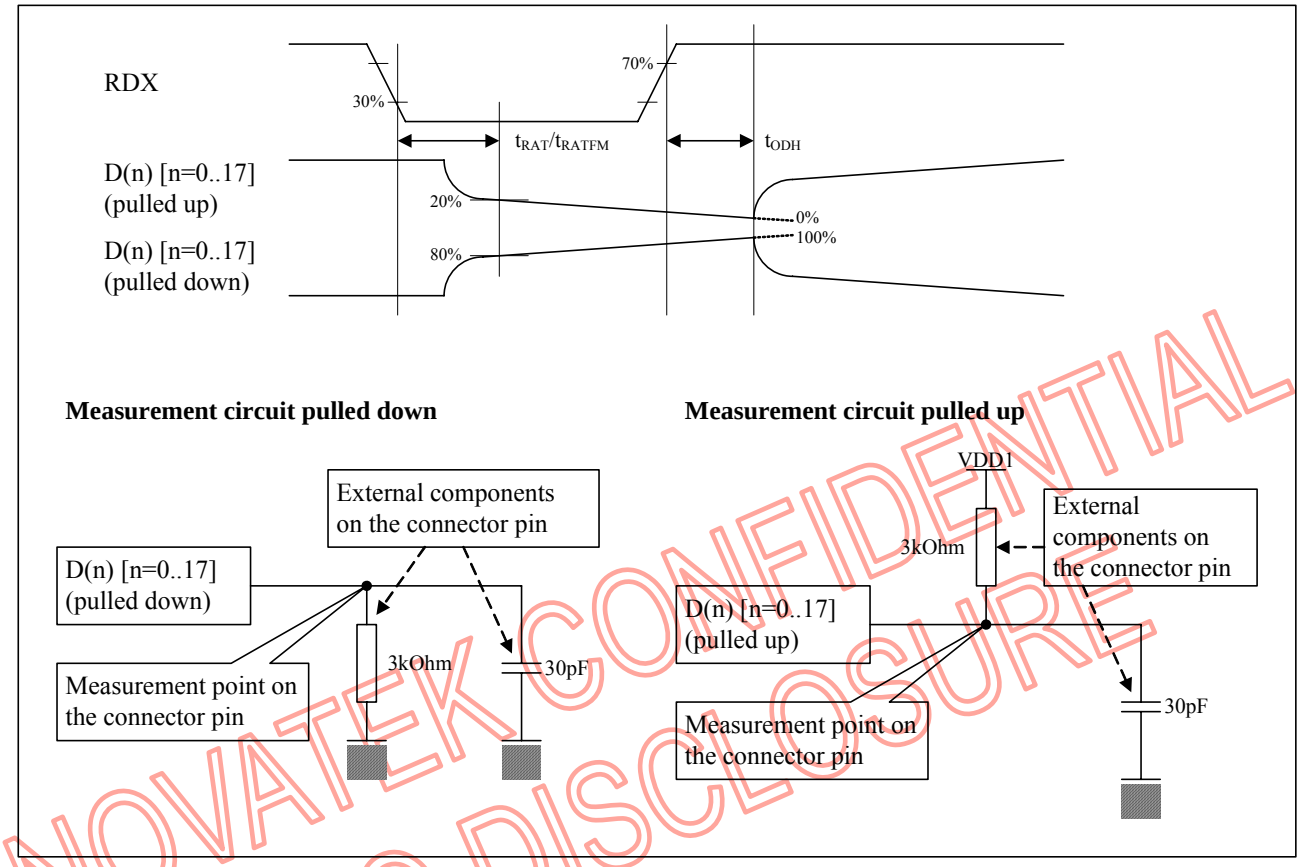


NOTE: Capacitances and resistances of the oscilloscope's probe must be include externals components in these measurements

Minimum Value Measurement

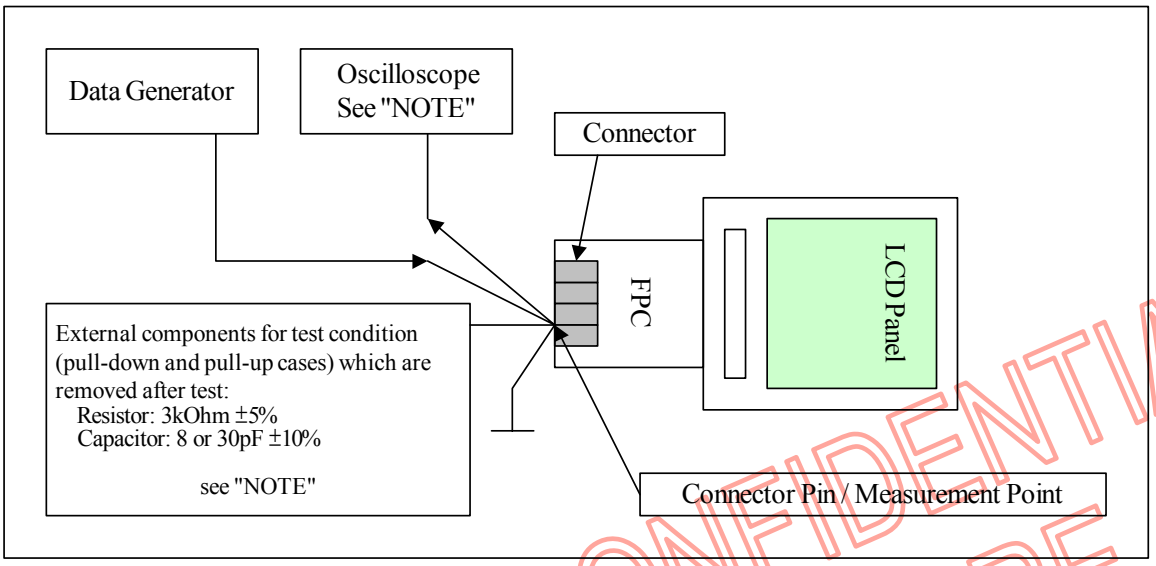


Maximum Value Measurement



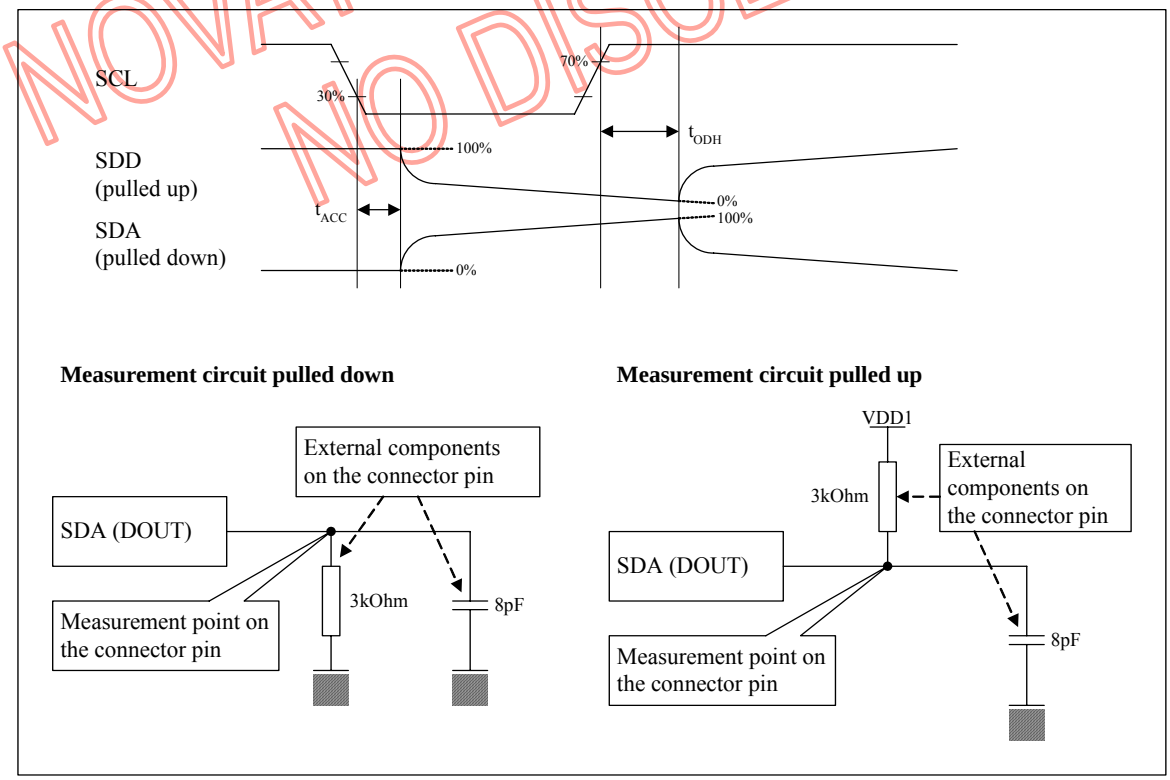
7.7.7.2 TACC, TOH MEASUREMENT CONDITION

Measurement Condition Set-up

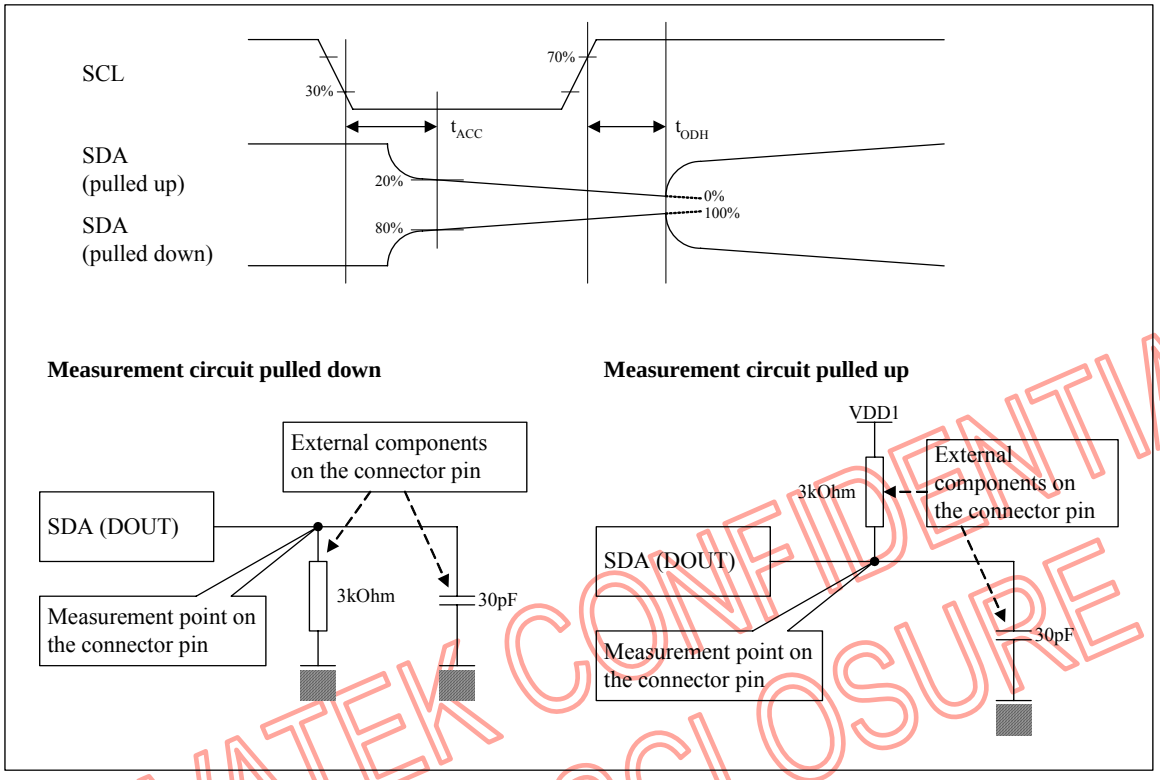


NOTE: Capacitances and resistances of the oscilloscope probe must be include externals components in these measurements

Minimum Value Measurement



Maximum Value Measurement



8 REFERENCE APPLICATIONS

8.1 MICROPROCESSOR INTERFACE

8.1.1 Interfacing with 80-series MPU 18-Bit Bus (P68='0', IM2,IM1,IM0='000', RCM='0')

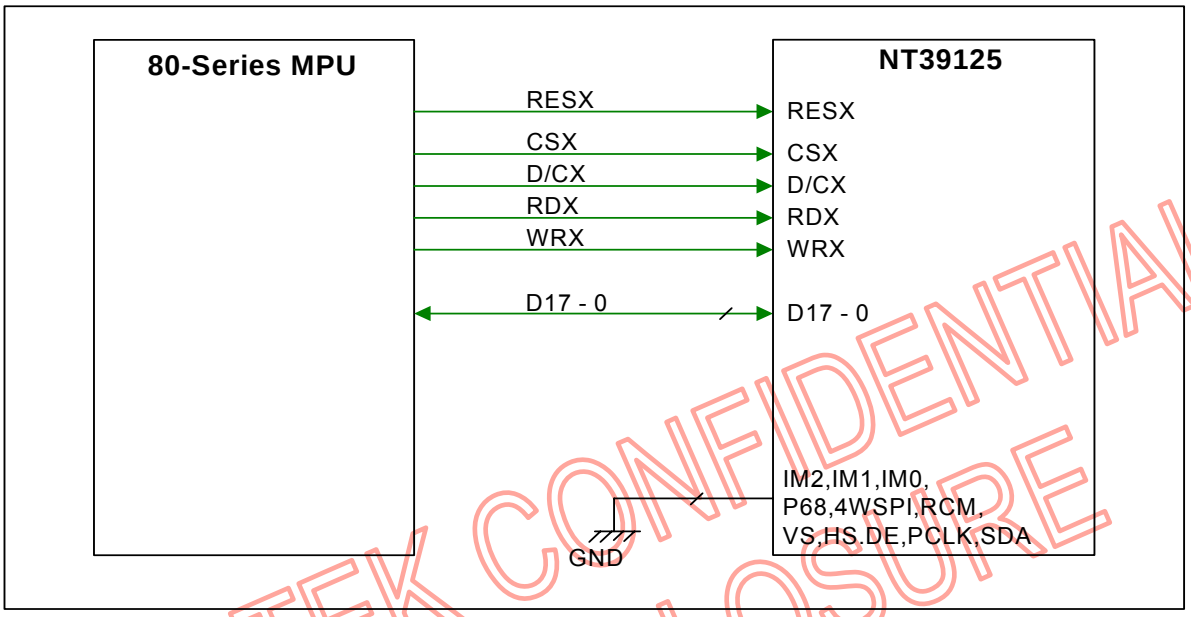


Fig. 8.1.1 Interfacing with 18-bit 80-series

8.1.2 Interfacing with 68-series MPU 18-Bit Bus (P68='1', IM2,IM1,IM0='000', RCM='0')

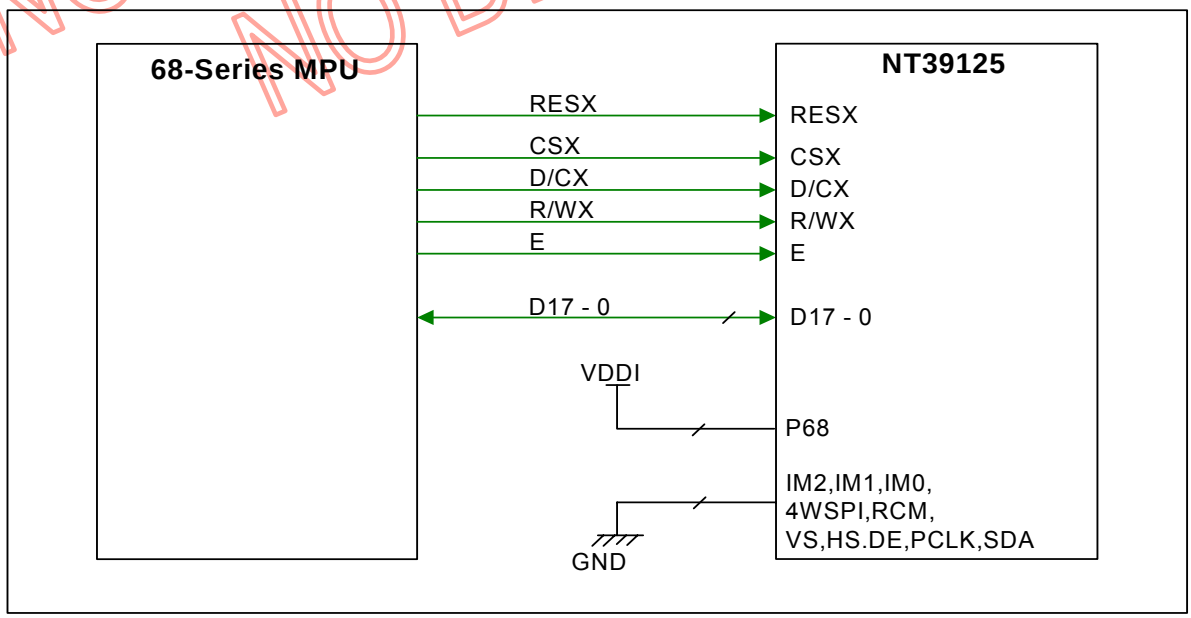


Fig. 8.1.2 Interfacing with 18-bit 68-series

8.1.3 Interfacing with 80-series MPU 9-Bit Bus (P68='0', IM2,IM1,IM0='001', RCM='0')

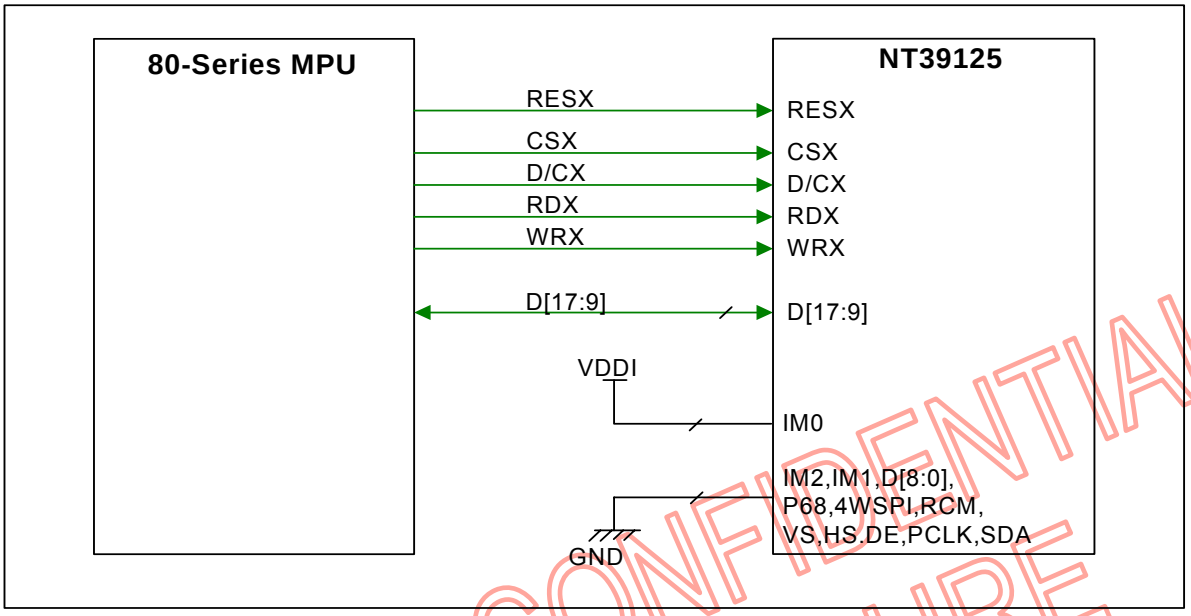


Fig. 8.1.3 Interfacing with 9-bit 80-series

8.1.4 Interfacing with 68-series MPU 9-Bit Bus (P68='1', IM2,IM1,IM0='001', RCM='0')

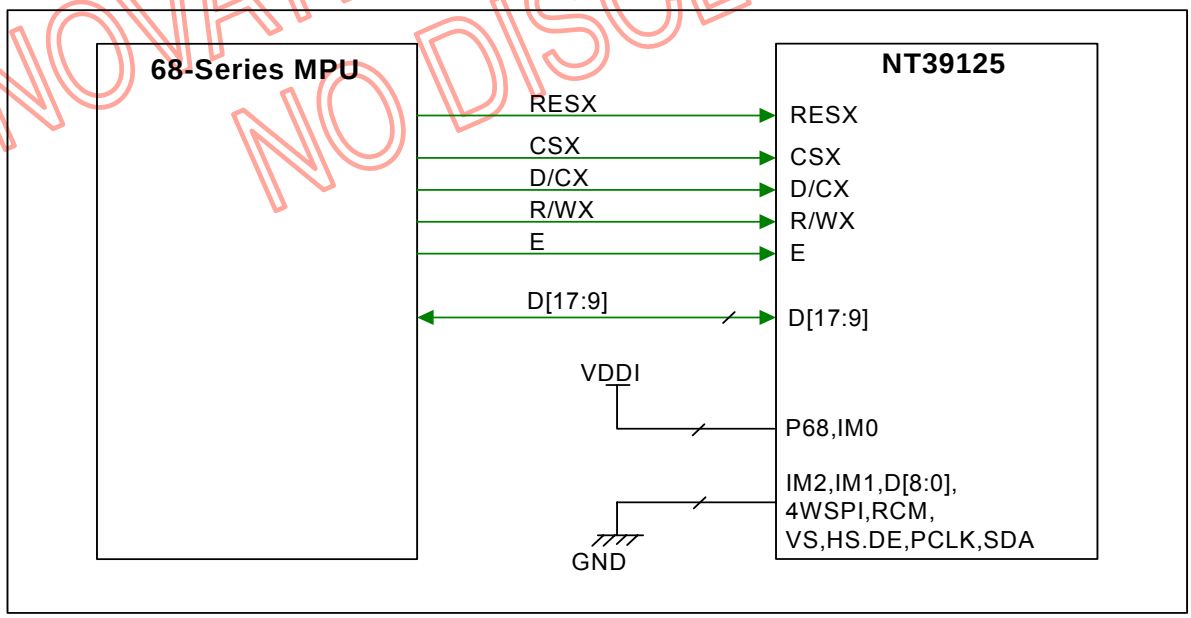


Fig. 8.1.4 Interfacing with 9-bit 68-series

8.1.5 Interfacing with 80-series MPU 16-Bit Bus (P68='0', IM2,IM1,IM0='010', RCM='0')

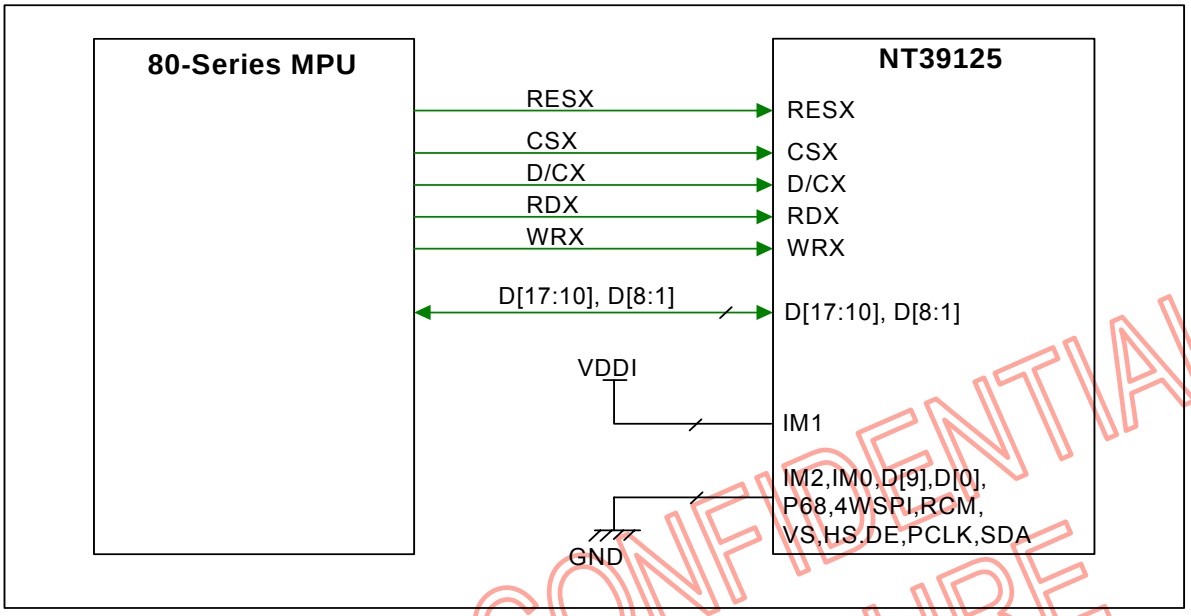


Fig. 8.1.5 Interfacing with 16-bit 80-series

8.1.6 Interfacing with 68-series MPU 16-Bit Bus (P68='1', IM2,IM1,IM0='010', RCM='0')

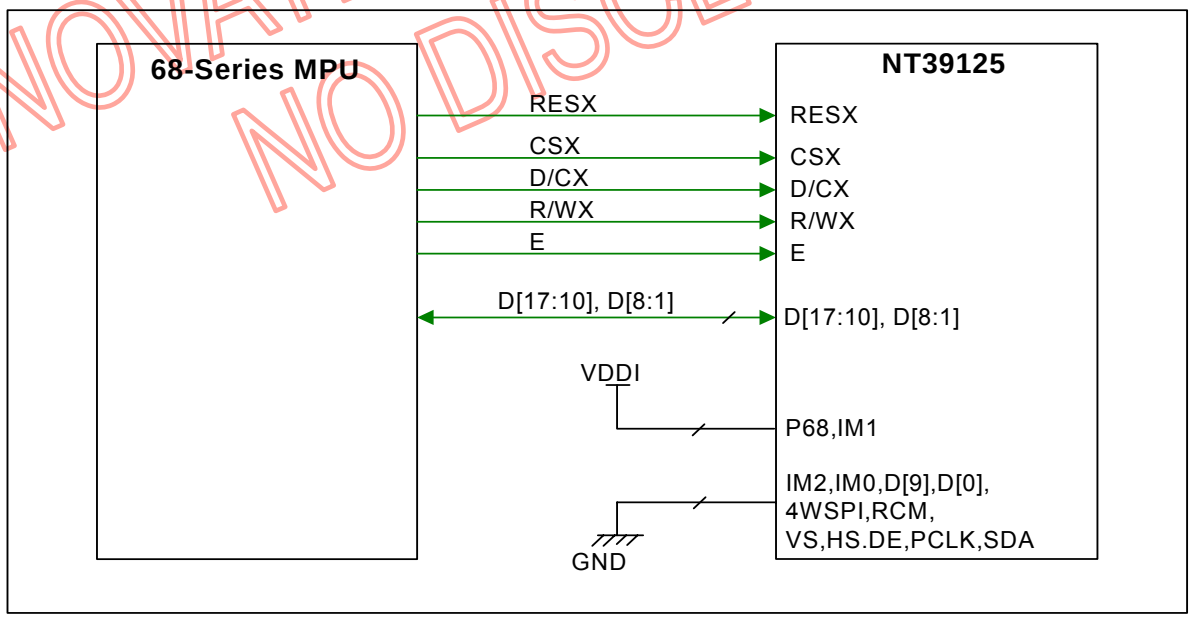


Fig. 8.1.6 Interfacing with 16-bit 68-series

8.1.7 Interfacing with 80-series MPU 8-Bit Bus (P68='0', IM2,IM1,IM0='010', RCM='0')

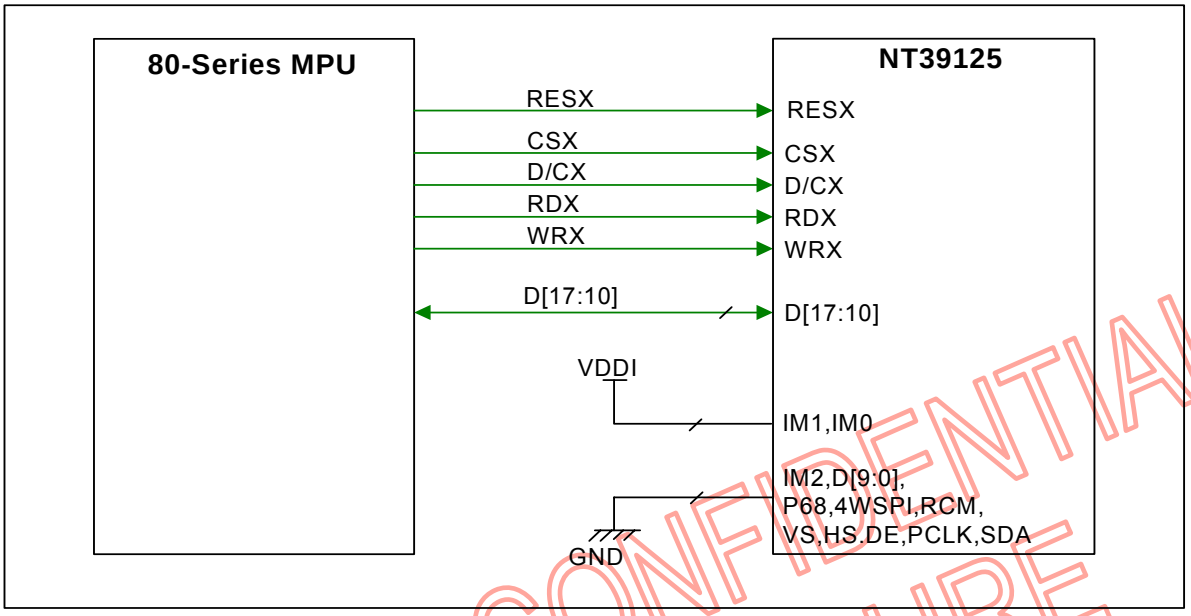


Fig. 8.1.7 Interfacing with 8-bit 80-series

8.1.8 Interfacing with 68-series MPU 8-Bit Bus (P68='1', IM2,IM1,IM0='010', RCM='0')

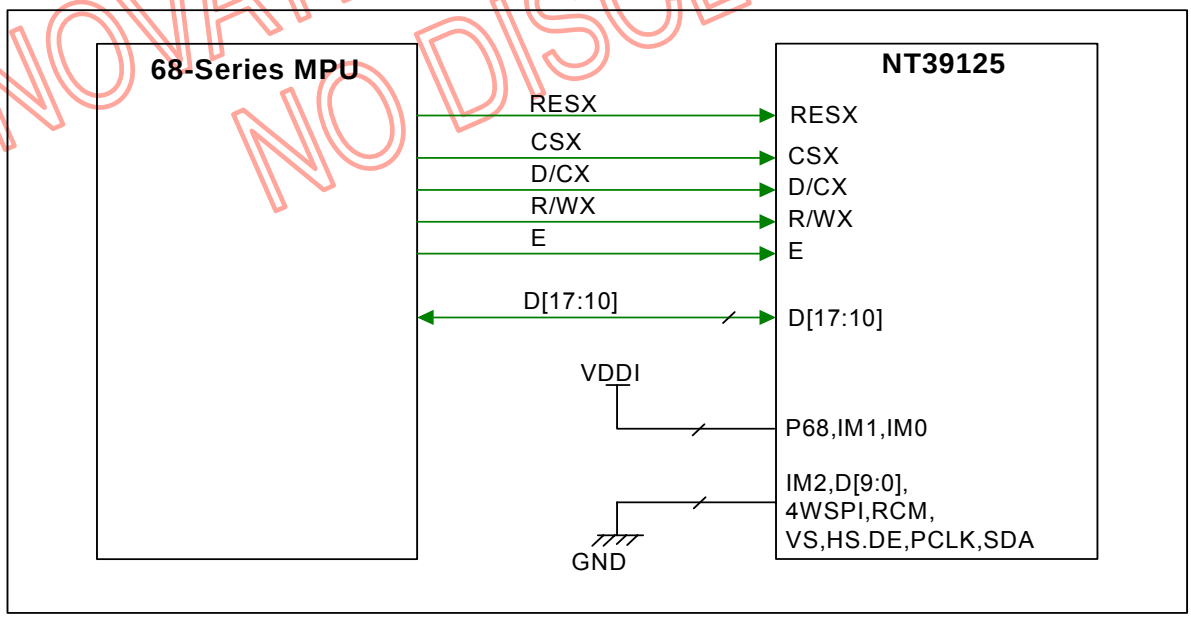


Fig. 8.1.8 Interfacing with 8-bit 68-series

8.1.9 Interfacing with 3-Pin Serial Mode (IM2,IM1,IM0='10x', RCM='0', 4WSPI='0')

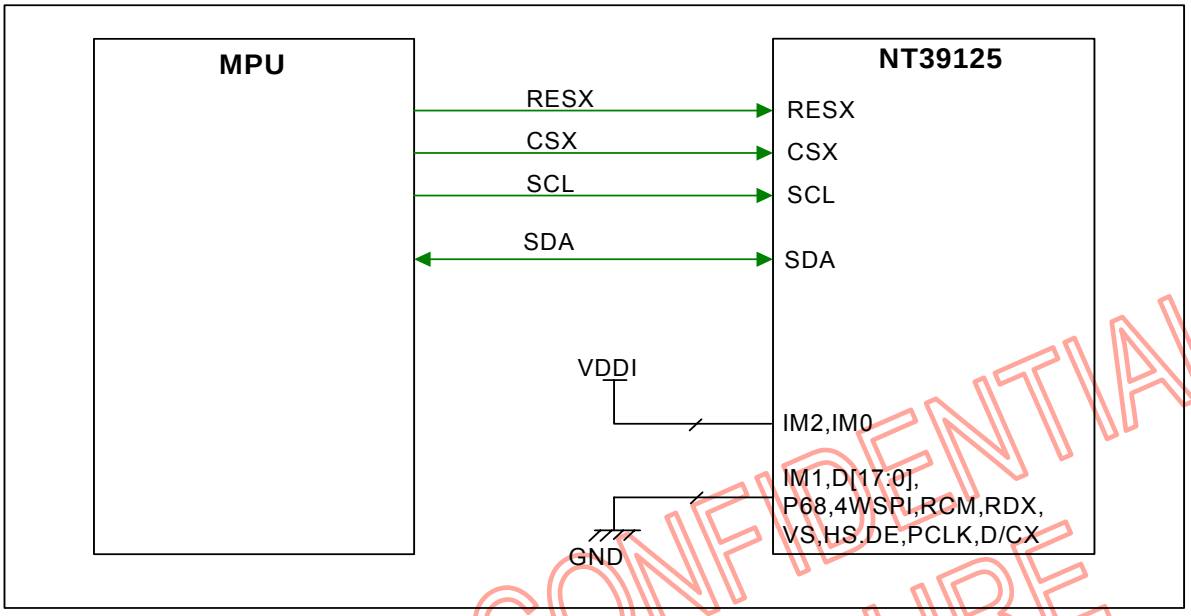


Fig. 8.1.9 Interfacing with 3-Pin Serial Mode

8.1.10 Interfacing with 4-Pin Serial Mode (IM2,IM1,IM0='10x', RCM='0', 4WSPI='1')

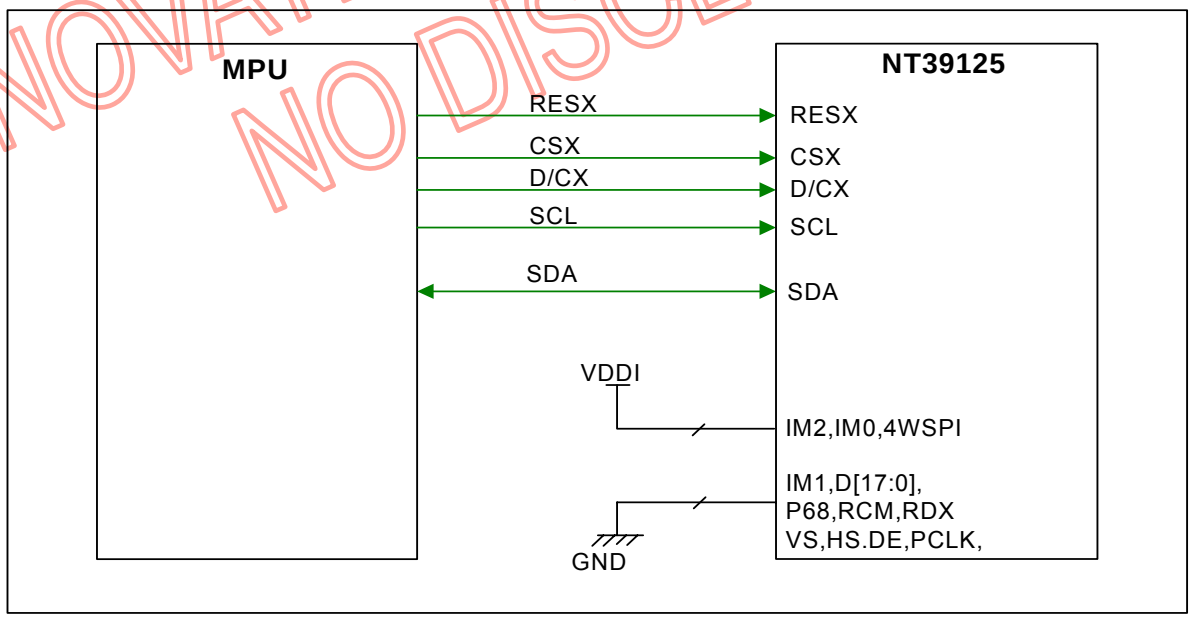


Fig. 8.1.10 Interfacing with 4-Pin Serial Mode

8.1.11 Interfacing with RGB mode (RCM='1')

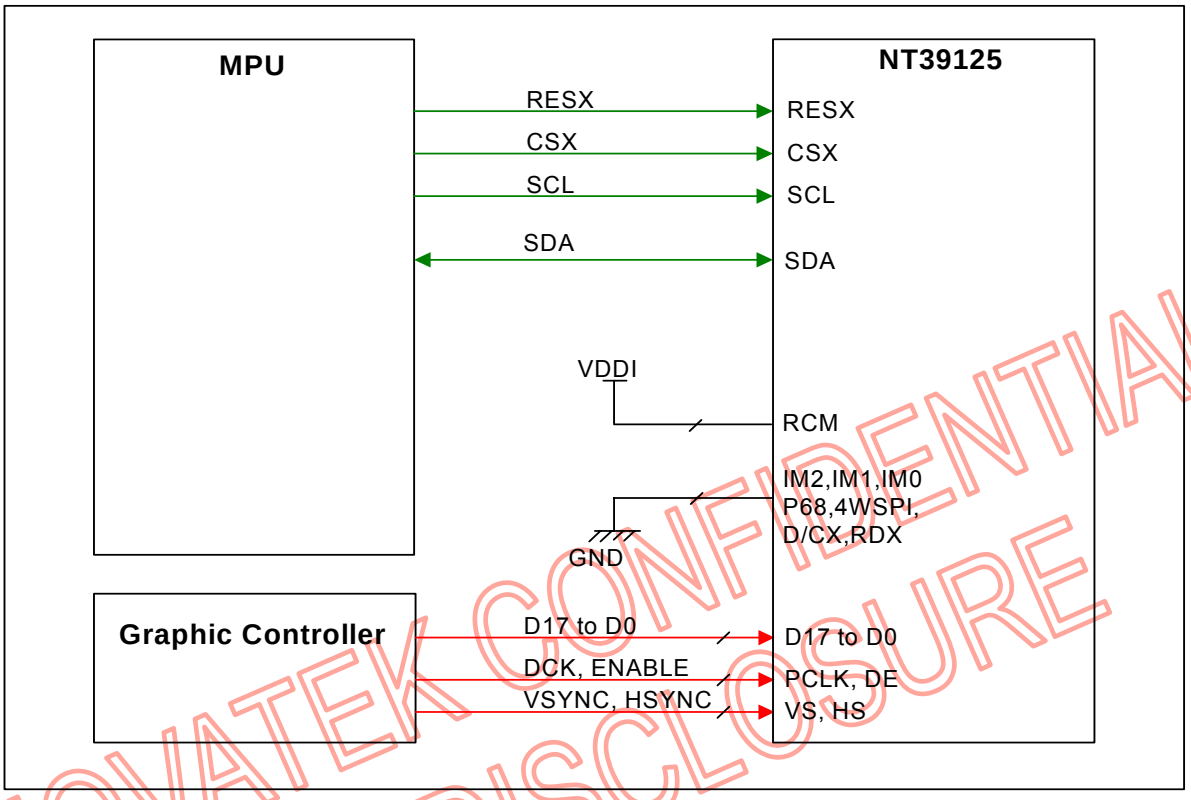
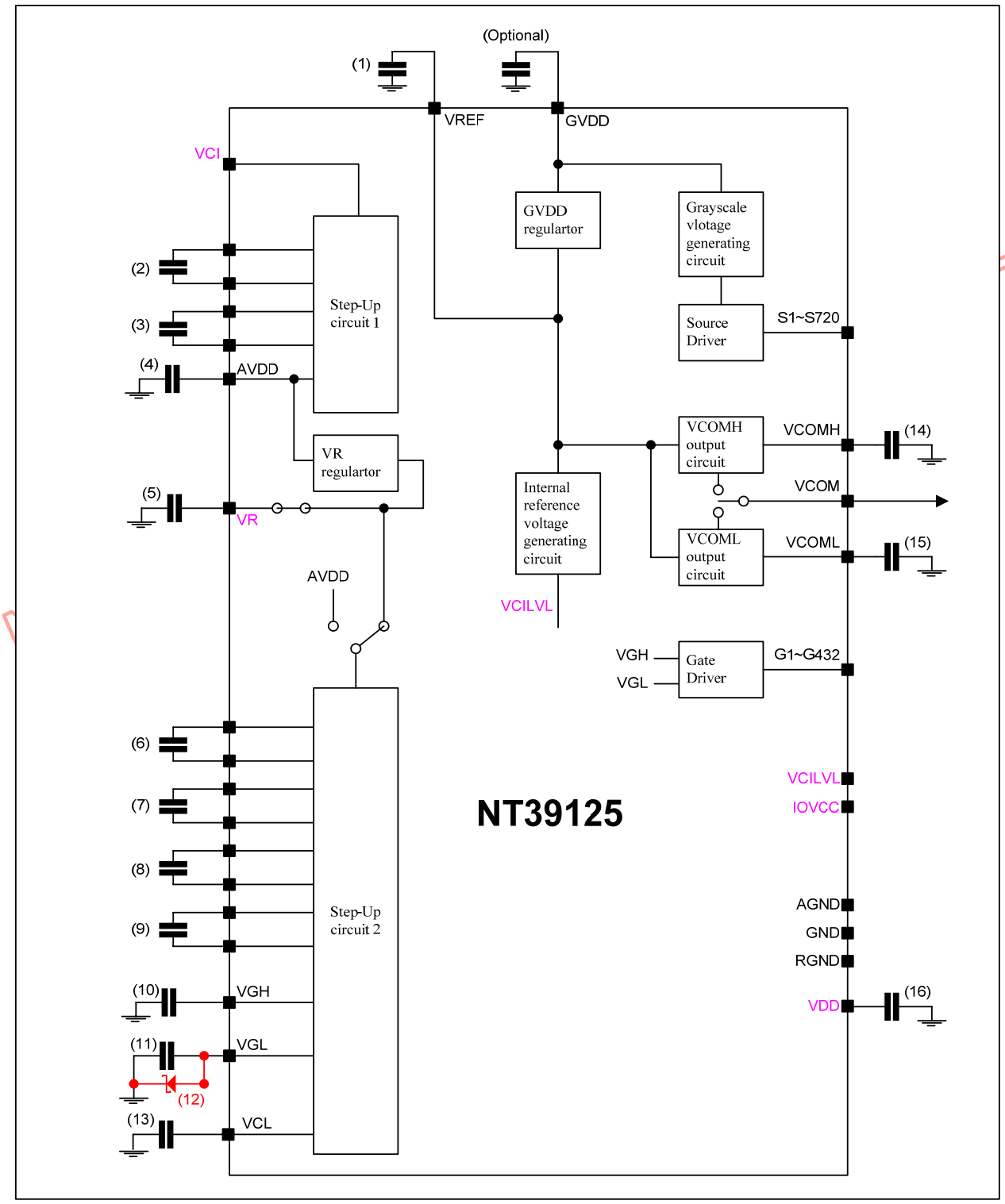


Fig. 8.1.11 Interfacing with RGB mode

8.2 EXTERNAL COMPONENTS CONNECTION

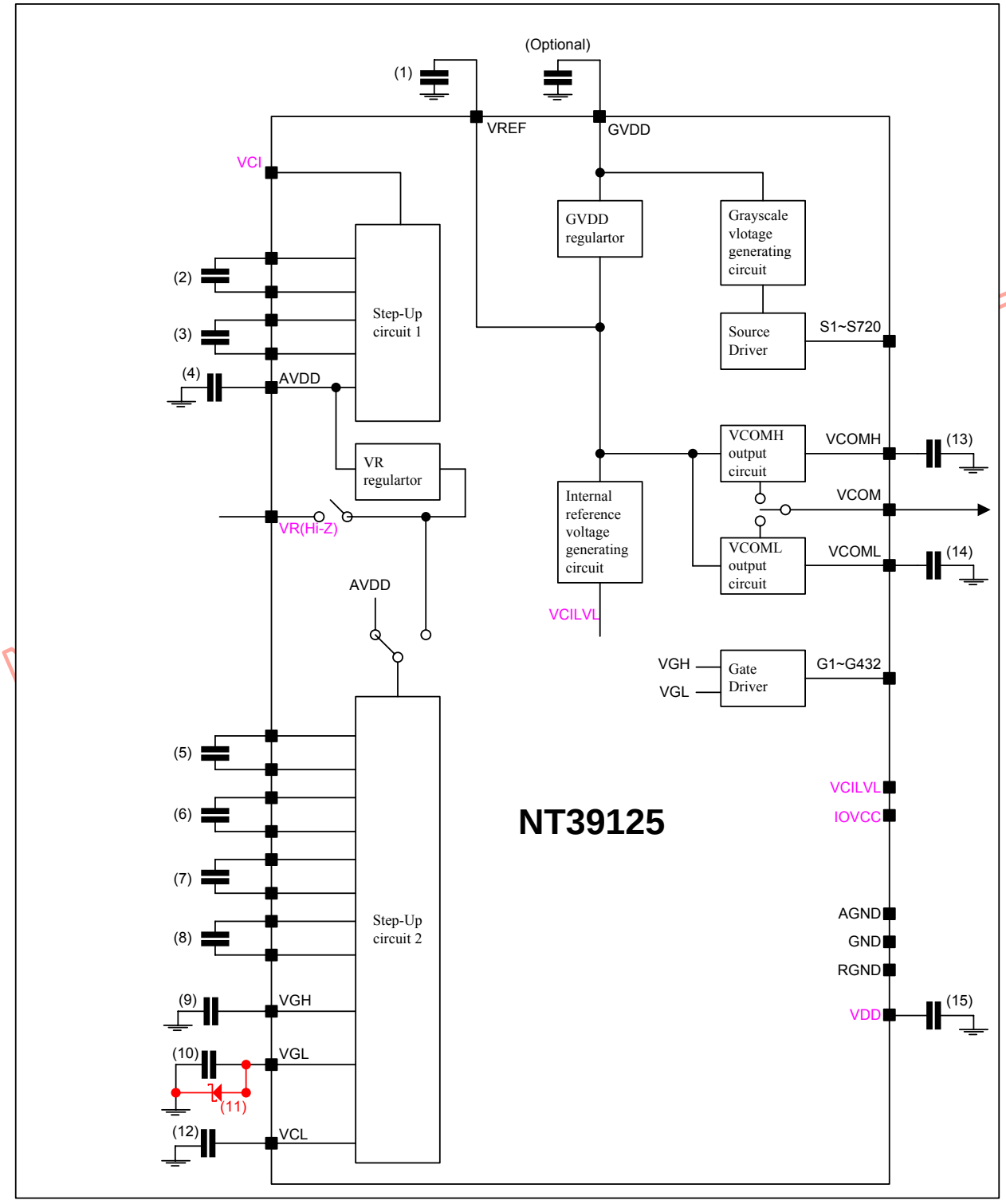
8.2.1 Configuration of Power Supply Circuit (VR=4.1V~5.5V)



The following table shows specifications of external elements:

No	Pad Name	Spec
1	Connect to Capacitor : VREF -------||-------- GND	1.0 uF (Max 6V)
2	Connect to Capacitor : C11+ -------||-------- C11-	1.0 uF (Max 6V)
3	Connect to Capacitor : C12+ -------||-------- C12-	1.0 uF (Max 6V)
4	Connect to Capacitor : AVDD -------||-------- GND	1.0 uF (Max 6V)
5	Connect to Capacitor : VR -------||-------- GND	1.0 uF (Max 6V)
6	Connect to Capacitor : C13+ -------||-------- C13-	1.0 uF (Max 6V)
7	Connect to Capacitor : C21+ -------||-------- C21-	1.0 uF (Max 10V)
8	Connect to Capacitor : C22+ -------||-------- C22-	1.0 uF (Max 10V)
9	Connect to Capacitor : C23+ -------||-------- C23-	1.0 uF (Max 10V)
10	Connect to Capacitor : VGH -------||-------- GND	1.0 uF (Max 25V)
11	Connect to Capacitor : VGL -------||-------- GND	1.0 uF (Max 25V)
12	Connect to Schottky diode: VGL -------►|-------- GND	Vf<0.4V at 20mA, -30~+85 degree C;VR > 30V
13	Connect to Capacitor : VCL -------||-------- GND	1.0 uF (Max 6V)
14	Connect to Capacitor : VCOMH -------||-------- GND	1.0 uF (Max 6V)
15	Connect to Capacitor : VCOML -------||-------- GND	1.0 uF (Max 6V)
16	Connect to Capacitor : VDD -------||-------- GND	1.0 uF (Max 6V)

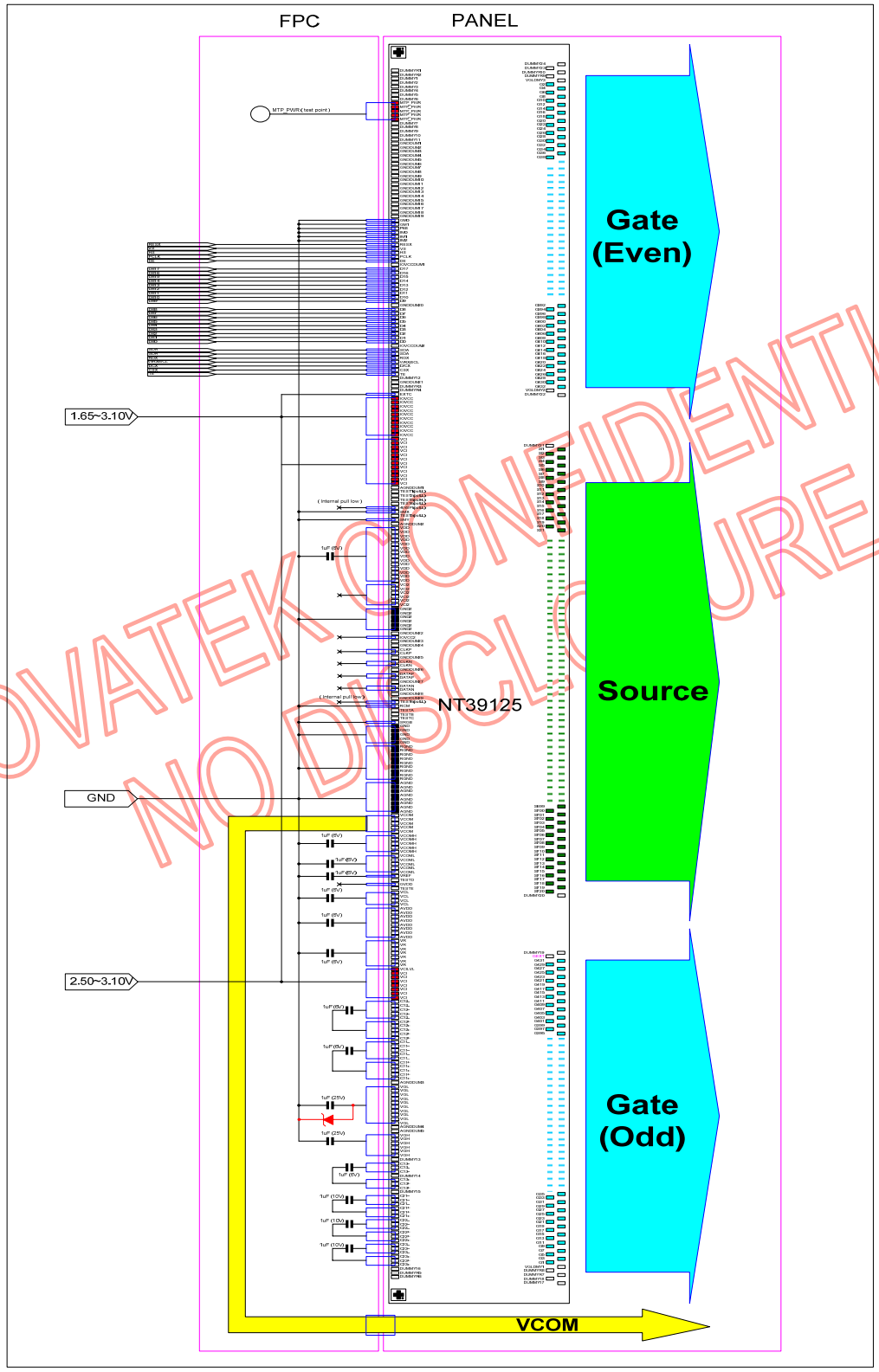
8.2.2 Configuration of Power Supply Circuit (VR=Hi-Z)



The following table shows specifications of external elements:

No	Pad Name	Spec
1	Connect to Capacitor : VREF -------||-------- GND	1.0 uF (Max 6V)
2	Connect to Capacitor : C11+ -------||-------- C11-	1.0 uF (Max 6V)
3	Connect to Capacitor : C12+ -------||-------- C12-	1.0 uF (Max 6V)
4	Connect to Capacitor : AVDD -------||-------- GND	1.0 uF (Max 6V)
5	Connect to Capacitor : C13+ -------||-------- C13-	1.0 uF (Max 6V)
6	Connect to Capacitor : C21+ -------||-------- C21-	1.0 uF (Max 10V)
7	Connect to Capacitor : C22+ -------||-------- C22-	1.0 uF (Max 10V)
8	Connect to Capacitor : C23+ -------||-------- C23-	1.0 uF (Max 10V)
9	Connect to Capacitor : VGH -------||-------- GND	1.0 uF (Max 25V)
10	Connect to Capacitor : VGL -------||-------- GND	1.0 uF (Max 25V)
11	Connect to Schottky diode: VGL -------►|-------- GND	Vf<0.4V at 20mA, -30~+85 degree C;VR > 30V
12	Connect to Capacitor : VCL -------||-------- GND	1.0 uF (Max 6V)
13	Connect to Capacitor : VCOMH -------||-------- GND	1.0 uF (Max 6V)
14	Connect to Capacitor : VCOML -------||-------- GND	1.0 uF (Max 6V)
15	Connect to Capacitor : VCC -------||-------- GND	1.0 uF (Max 6V)

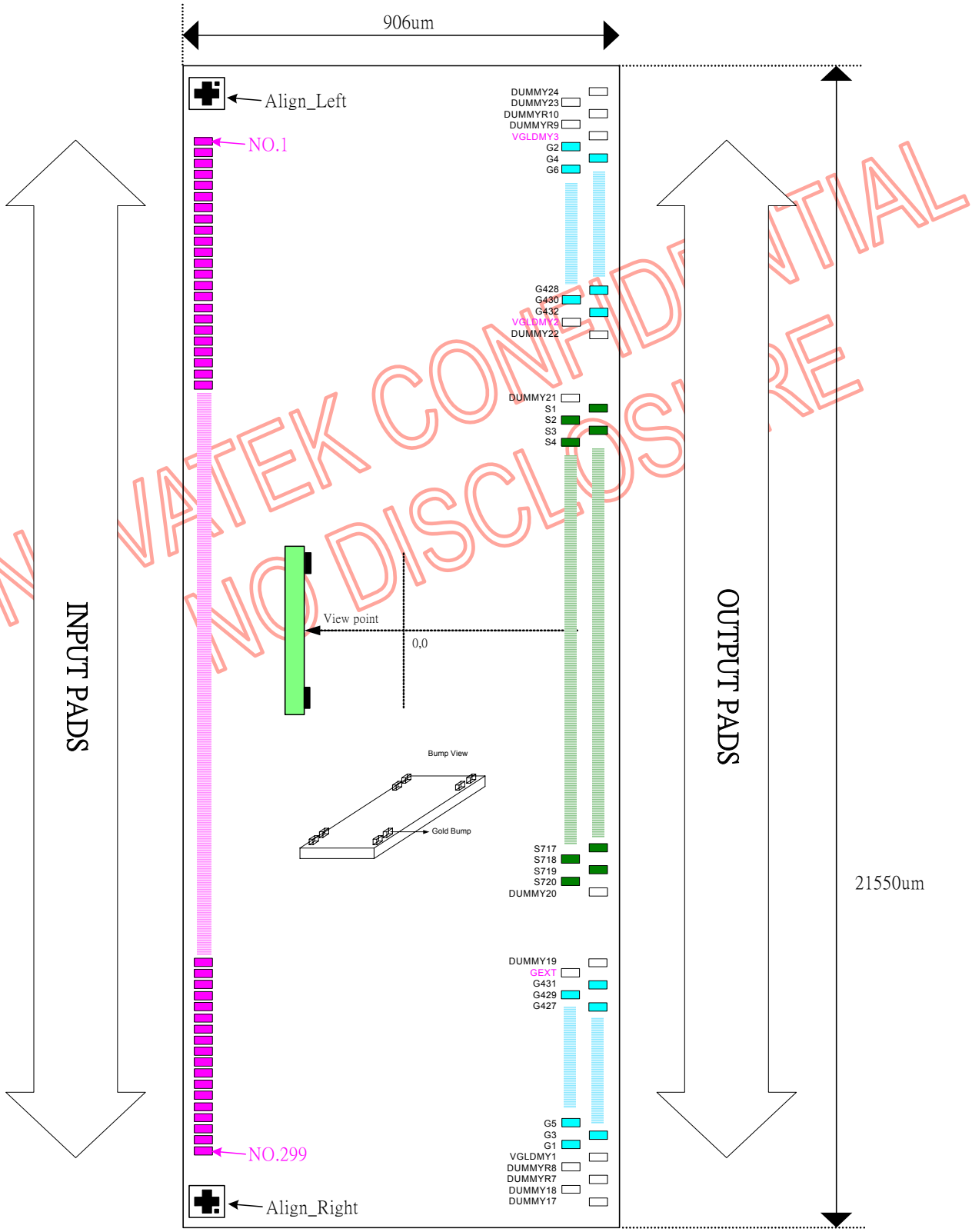
8.3 CONNECTION EXAMPLE WITH EXTERNAL COMPONENTS



9 CHIP INFORMATION

9.1 Chip Overview

-**Chip Size=** 21.550mm x 0.906mm
-**Chip Thickness=** 300 ± 20um

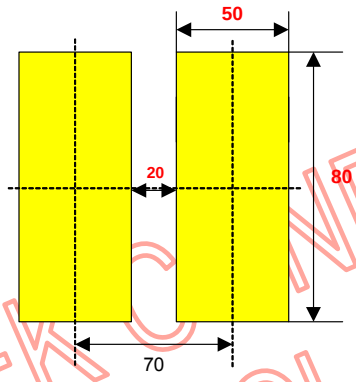


9.2 Bump Information

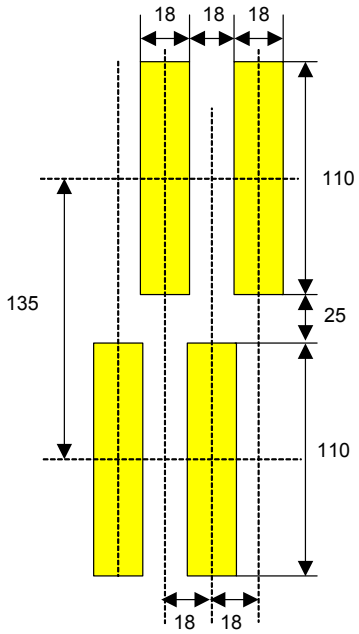
-PAD coordination: PAD center
-Coordinate origin: Chip center
-Au bumps size:
- Input side: 50um x 80um
- Output side: 18um x 110um

-**Au bump height=** 15um
-**Au bump hardness=** 65 ± 15 HV

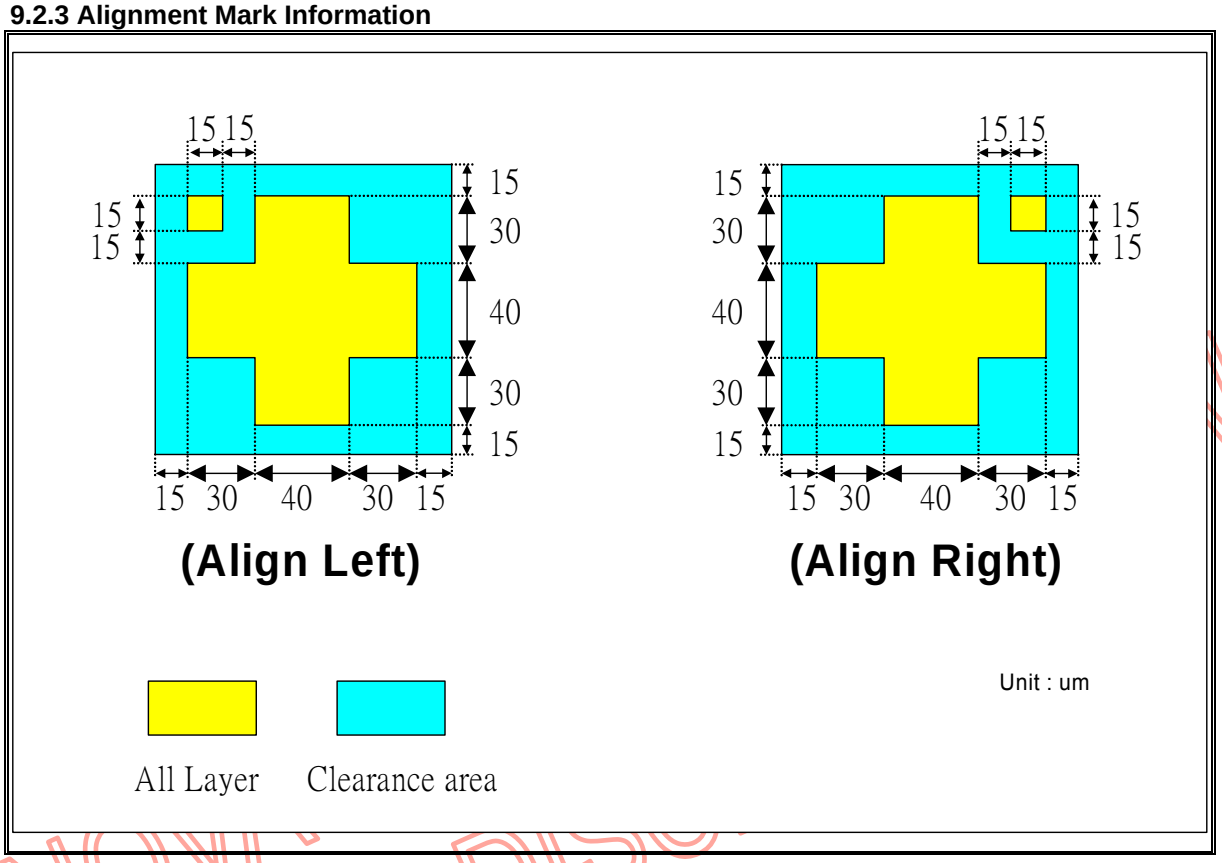
9.2.1 Input Pads Information

Input PAD	
NO.1~NO.299	 Unit : um

9.2.2 Output Pads Information

Output PAD	
NO.300~ NO.1467	 Unit : um

9.2.3 Alignment Mark Information



9.3 ALIGNMENT COORDINATES

	X-pos	Y-pos
Align_Left	-10655	-334
Aligh_Right	10655	-334

9.4 PAD COORDINATES

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
1	-10430.0	-354	DUMMYR1	61	-6230.0	-354	D7	121	-2030.0	-354	VDD
2	-10360.0	-354	DUMMYR2	62	-6160.0	-354	D6	122	-1960.0	-354	VDD
3	-10290.0	-354	DUMMY1	63	-6090.0	-354	D5	123	-1890.0	-354	VDD
4	-10220.0	-354	DUMMY2	64	-6020.0	-354	D4	124	-1820.0	-354	VDD
5	-10150.0	-354	DUMMY3	65	-5950.0	-354	D3	125	-1750.0	-354	VDD
6	-10080.0	-354	DUMMY4	66	-5880.0	-354	D2	126	-1680.0	-354	VDD
7	-10010.0	-354	DUMMY5	67	-5810.0	-354	D1	127	-1610.0	-354	VDD
8	-9940.0	-354	DUMMY6	68	-5740.0	-354	D0	128	-1540.0	-354	VCI2
9	-9870.0	-354	MTP_PWR	69	-5670.0	-354	IOVCCDUM2	129	-1470.0	-354	VCI2
10	-9800.0	-354	MTP_PWR	70	-5600.0	-354	SDA	130	-1400.0	-354	VCI2
11	-9730.0	-354	MTP_PWR	71	-5530.0	-354	SDA	131	-1330.0	-354	VCI2
12	-9660.0	-354	MTP_PWR	72	-5460.0	-354	RDX	132	-1260.0	-354	VCI2
13	-9590.0	-354	MTP_PWR	73	-5390.0	-354	WRX/SCL	133	-1190.0	-354	VCI2
14	-9520.0	-354	DUMMY7	74	-5320.0	-354	D/CX	134	-1120.0	-354	GND2
15	-9450.0	-354	DUMMY8	75	-5250.0	-354	CSX	135	-1050.0	-354	GND2
16	-9380.0	-354	DUMMY9	76	-5180.0	-354	TE	136	-980.0	-354	GND2
17	-9310.0	-354	DUMMY10	77	-5110.0	-354	DUMMY12	137	-910.0	-354	GND2
18	-9240.0	-354	DUMMY11	78	-5040.0	-354	GNDDUM21	138	-840.0	-354	GND2
19	-9170.0	-354	GNDDUM1	79	-4970.0	-354	DUMMYR3	139	-770.0	-354	GND2
20	-9100.0	-354	GNDDUM2	80	-4900.0	-354	DUMMYR4	140	-700.0	-354	GNDDUM22
21	-9030.0	-354	GNDDUM3	81	-4830.0	-354	EXTC	141	-630.0	-354	IOVCC2
22	-8960.0	-354	GNDDUM4	82	-4760.0	-354	IOVCC	142	-560.0	-354	GNDDUM23
23	-8890.0	-354	GNDDUM5	83	-4690.0	-354	IOVCC	143	-490.0	-354	GNDDUM24
24	-8820.0	-354	GNDDUM6	84	-4620.0	-354	IOVCC	144	-420.0	-354	CLKP
25	-8750.0	-354	GNDDUM7	85	-4550.0	-354	IOVCC	145	-350.0	-354	CLKP
26	-8680.0	-354	GNDDUM8	86	-4480.0	-354	IOVCC	146	-280.0	-354	GNDDUM25
27	-8610.0	-354	GNDDUM9	87	-4410.0	-354	IOVCC	147	-210.0	-354	CLKN
28	-8540.0	-354	GNDDUM10	88	-4340.0	-354	IOVCC	148	-140.0	-354	CLKN
29	-8470.0	-354	GNDDUM11	89	-4270.0	-354	IOVCC	149	-70.0	-354	GNDDUM26
30	-8400.0	-354	GNDDUM12	90	-4200.0	-354	IOVCC	150	0.0	-354	DATAP
31	-8330.0	-354	GNDDUM13	91	-4130.0	-354	IOVCC	151	70.0	-354	DATAP
32	-8260.0	-354	GNDDUM14	92	-4060.0	-354	VCI	152	140.0	-354	GNDDUM27
33	-8190.0	-354	GNDDUM15	93	-3990.0	-354	VCI	153	210.0	-354	DATAN
34	-8120.0	-354	GNDDUM16	94	-3920.0	-354	VCI	154	280.0	-354	DATAN
35	-8050.0	-354	GNDDUM17	95	-3850.0	-354	VCI	155	350.0	-354	GNDDUM28
36	-7980.0	-354	GNDDUM18	96	-3780.0	-354	VCI	156	420.0	-354	GNDDUM29
37	-7910.0	-354	GNDDUM19	97	-3710.0	-354	VCI	157	490.0	-354	TEST6(pull-L)
38	-7840.0	-354	GM0	98	-3640.0	-354	VCI	158	560.0	-354	RCM
39	-7770.0	-354	GM1	99	-3570.0	-354	VCI	159	630.0	-354	TESTA
40	-7700.0	-354	P68	100	-3500.0	-354	VCI	160	700.0	-354	TESTB
41	-7630.0	-354	IM0	101	-3430.0	-354	VCI	161	770.0	-354	TESTC
42	-7560.0	-354	IM1	102	-3360.0	-354	VCI	162	840.0	-354	SRGB
43	-7490.0	-354	IM2	103	-3290.0	-354	VCI	163	910.0	-354	GND
44	-7420.0	-354	RESX	104	-3220.0	-354	AGNDDUM1	164	980.0	-354	GND
45	-7350.0	-354	VS	105	-3150.0	-354	TEST1(pull-L)	165	1050.0	-354	GND
46	-7280.0	-354	HS	106	-3080.0	-354	TEST2(pull-L)	166	1120.0	-354	GND
47	-7210.0	-354	PCLK	107	-3010.0	-354	TEST3(pull-L)	167	1190.0	-354	GND
48	-7140.0	-354	DE	108	-2940.0	-354	TEST4(pull-L)	168	1260.0	-354	RGND
49	-7070.0	-354	IOVCCDUM1	109	-2870.0	-354	4WSPI(pull-L)	169	1330.0	-354	RGND
50	-7000.0	-354	D17	110	-2800.0	-354	SMX	170	1400.0	-354	RGND
51	-6930.0	-354	D16	111	-2730.0	-354	TEST5(pull-L)	171	1470.0	-354	RGND
52	-6860.0	-354	D15	112	-2660.0	-354	SMY	172	1540.0	-354	RGND
53	-6790.0	-354	D14	113	-2590.0	-354	AGNDDUM2	173	1610.0	-354	RGND
54	-6720.0	-354	D13	114	-2520.0	-354	VDD	174	1680.0	-354	RGND
55	-6650.0	-354	D12	115	-2450.0	-354	VDD	175	1750.0	-354	RGND
56	-6580.0	-354	D11	116	-2380.0	-354	VDD	176	1820.0	-354	RGND
57	-6510.0	-354	D10	117	-2310.0	-354	VDD	177	1890.0	-354	AGND
58	-6440.0	-354	D9	118	-2240.0	-354	VDD	178	1960.0	-354	AGND
59	-6370.0	-354	GNDDUM20	119	-2170.0	-354	VDD	179	2030.0	-354	AGND
60	-6300.0	-354	DB8	120	-2100.0	-354	VDD	180	2100.0	-354	AGND

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
181	2170.0	-354	AGND	241	6370.0	-354	C11-	301	10629.0	204	DUMMY18
182	2240.0	-354	AGND	242	6440.0	-354	C11-	302	10611.0	339	DUMMYR7
183	2310.0	-354	AGND	243	6510.0	-354	C11-	303	10593.0	204	DUMMYR8
184	2380.0	-354	AGND	244	6580.0	-354	C11-	304	10575.0	339	VGLDMY1
185	2450.0	-354	VCOM	245	6650.0	-354	C11-	305	10557.0	204	G1
186	2520.0	-354	VCOM	246	6720.0	-354	C11+	306	10539.0	339	G3
187	2590.0	-354	VCOM	247	6790.0	-354	C11+	307	10521.0	204	G5
188	2660.0	-354	VCOM	248	6860.0	-354	C11+	308	10503.0	339	G7
189	2730.0	-354	VCOM	249	6930.0	-354	C11+	309	10485.0	204	G9
190	2800.0	-354	VCOMH	250	7000.0	-354	C11+	310	10467.0	339	G11
191	2870.0	-354	VCOMH	251	7070.0	-354	AGNDDUM3	311	10449.0	204	G13
192	2940.0	-354	VCOMH	252	7140.0	-354	VGL	312	10431.0	339	G15
193	3010.0	-354	VCOMH	253	7210.0	-354	VGL	313	10413.0	204	G17
194	3080.0	-354	VCOMH	254	7280.0	-354	VGL	314	10395.0	339	G19
195	3150.0	-354	VCOML	255	7350.0	-354	VGL	315	10377.0	204	G21
196	3220.0	-354	VCOML	256	7420.0	-354	VGL	316	10359.0	339	G23
197	3290.0	-354	VCOML	257	7490.0	-354	VGL	317	10341.0	204	G25
198	3360.0	-354	VCOML	258	7560.0	-354	VGL	318	10323.0	339	G27
199	3430.0	-354	VCOML	259	7630.0	-354	VGL	319	10305.0	204	G29
200	3500.0	-354	VREF	260	7700.0	-354	VGL	320	10287.0	339	G31
201	3570.0	-354	TESTD	261	7770.0	-354	VGL	321	10269.0	204	G33
202	3640.0	-354	GVDD	262	7840.0	-354	AGNDDUM4	322	10251.0	339	G35
203	3710.0	-354	TESTE	263	7910.0	-354	AGNDDUM5	323	10233.0	204	G37
204	3780.0	-354	VCL	264	7980.0	-354	VGH	324	10215.0	339	G39
205	3850.0	-354	VCL	265	8050.0	-354	VGH	325	10197.0	204	G41
206	3920.0	-354	VCL	266	8120.0	-354	VGH	326	10179.0	339	G43
207	3990.0	-354	VCL	267	8190.0	-354	VGH	327	10161.0	204	G45
208	4060.0	-354	AVDD	268	8260.0	-354	VGH	328	10143.0	339	G47
209	4130.0	-354	AVDD	269	8330.0	-354	VGH	329	10125.0	204	G49
210	4200.0	-354	AVDD	270	8400.0	-354	DUMMY13	330	10107.0	339	G51
211	4270.0	-354	AVDD	271	8470.0	-354	C13-	331	10089.0	204	G53
212	4340.0	-354	AVDD	272	8540.0	-354	C13-	332	10071.0	339	G55
213	4410.0	-354	AVDD	273	8610.0	-354	C13-	333	10053.0	204	G57
214	4480.0	-354	AVDD	274	8680.0	-354	DUMMY14	334	10035.0	339	G59
215	4550.0	-354	AVDD	275	8750.0	-354	C13+	335	10017.0	204	G61
216	4620.0	-354	VR	276	8820.0	-354	C13+	336	9999.0	339	G63
217	4690.0	-354	VR	277	8890.0	-354	C13+	337	9981.0	204	G65
218	4760.0	-354	VR	278	8960.0	-354	DUMMY15	338	9963.0	339	G67
219	4830.0	-354	VR	279	9030.0	-354	C21-	339	9945.0	204	G69
220	4900.0	-354	VR	280	9100.0	-354	C21-	340	9927.0	339	G71
221	4970.0	-354	VR	281	9170.0	-354	C21-	341	9909.0	204	G73
222	5040.0	-354	VR	282	9240.0	-354	C21+	342	9891.0	339	G75
223	5110.0	-354	VCILVL	283	9310.0	-354	C21+	343	9873.0	204	G77
224	5180.0	-354	VCI	284	9380.0	-354	C21+	344	9855.0	339	G79
225	5250.0	-354	VCI	285	9450.0	-354	C22-	345	9837.0	204	G81
226	5320.0	-354	VCI	286	9520.0	-354	C22-	346	9819.0	339	G83
227	5390.0	-354	VCI	287	9590.0	-354	C22-	347	9801.0	204	G85
228	5460.0	-354	VCI	288	9660.0	-354	C22+	348	9783.0	339	G87
229	5530.0	-354	VCI	289	9730.0	-354	C22+	349	9765.0	204	G89
230	5600.0	-354	VCI	290	9800.0	-354	C22+	350	9747.0	339	G91
231	5670.0	-354	C12-	291	9870.0	-354	C23-	351	9729.0	204	G93
232	5740.0	-354	C12-	292	9940.0	-354	C23-	352	9711.0	339	G95
233	5810.0	-354	C12-	293	10010.0	-354	C23-	353	9693.0	204	G97
234	5880.0	-354	C12-	294	10080.0	-354	C23+	354	9675.0	339	G99
235	5950.0	-354	C12-	295	10150.0	-354	C23+	355	9657.0	204	G101
236	6020.0	-354	C12+	296	10220.0	-354	C23+	356	9639.0	339	G103
237	6090.0	-354	C12+	297	10290.0	-354	DUMMY16	357	9621.0	204	G105
238	6160.0	-354	C12+	298	10360.0	-354	DUMMYR5	358	9603.0	339	G107
239	6230.0	-354	C12+	299	10430.0	-354	DUMMYR6	359	9585.0	204	G109
240	6300.0	-354	C12+	300	10647.0	339	DUMMY17	360	9567.0	339	G111

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
361	9549.0	204	G113	421	8469.0	204	G233	481	7389.0	204	G353
362	9531.0	339	G115	422	8451.0	339	G235	482	7371.0	339	G355
363	9513.0	204	G117	423	8433.0	204	G237	483	7353.0	204	G357
364	9495.0	339	G119	424	8415.0	339	G239	484	7335.0	339	G359
365	9477.0	204	G121	425	8397.0	204	G241	485	7317.0	204	G361
366	9459.0	339	G123	426	8379.0	339	G243	486	7299.0	339	G363
367	9441.0	204	G125	427	8361.0	204	G245	487	7281.0	204	G365
368	9423.0	339	G127	428	8343.0	339	G247	488	7263.0	339	G367
369	9405.0	204	G129	429	8325.0	204	G249	489	7245.0	204	G369
370	9387.0	339	G131	430	8307.0	339	G251	490	7227.0	339	G371
371	9369.0	204	G133	431	8289.0	204	G253	491	7209.0	204	G373
372	9351.0	339	G135	432	8271.0	339	G255	492	7191.0	339	G375
373	9333.0	204	G137	433	8253.0	204	G257	493	7173.0	204	G377
374	9315.0	339	G139	434	8235.0	339	G259	494	7155.0	339	G379
375	9297.0	204	G141	435	8217.0	204	G261	495	7137.0	204	G381
376	9279.0	339	G143	436	8199.0	339	G263	496	7119.0	339	G383
377	9261.0	204	G145	437	8181.0	204	G265	497	7101.0	204	G385
378	9243.0	339	G147	438	8163.0	339	G267	498	7083.0	339	G387
379	9225.0	204	G149	439	8145.0	204	G269	499	7065.0	204	G389
380	9207.0	339	G151	440	8127.0	339	G271	500	7047.0	339	G391
381	9189.0	204	G153	441	8109.0	204	G273	501	7029.0	204	G393
382	9171.0	339	G155	442	8091.0	339	G275	502	7011.0	339	G395
383	9153.0	204	G157	443	8073.0	204	G277	503	6993.0	204	G397
384	9135.0	339	G159	444	8055.0	339	G279	504	6975.0	339	G399
385	9117.0	204	G161	445	8037.0	204	G281	505	6957.0	204	G401
386	9099.0	339	G163	446	8019.0	339	G283	506	6939.0	339	G403
387	9081.0	204	G165	447	8001.0	204	G285	507	6921.0	204	G405
388	9063.0	339	G167	448	7983.0	339	G287	508	6903.0	339	G407
389	9045.0	204	G169	449	7965.0	204	G289	509	6885.0	204	G409
390	9027.0	339	G171	450	7947.0	339	G291	510	6867.0	339	G411
391	9009.0	204	G173	451	7929.0	204	G293	511	6849.0	204	G413
392	8991.0	339	G175	452	7911.0	339	G295	512	6831.0	339	G415
393	8973.0	204	G177	453	7893.0	204	G297	513	6813.0	204	G417
394	8955.0	339	G179	454	7875.0	339	G299	514	6795.0	339	G419
395	8937.0	204	G181	455	7857.0	204	G301	515	6777.0	204	G421
396	8919.0	339	G183	456	7839.0	339	G303	516	6759.0	339	G423
397	8901.0	204	G185	457	7821.0	204	G305	517	6741.0	204	G425
398	8883.0	339	G187	458	7803.0	339	G307	518	6723.0	339	G427
399	8865.0	204	G189	459	7785.0	204	G309	519	6705.0	204	G429
400	8847.0	339	G191	460	7767.0	339	G311	520	6687.0	339	G431
401	8829.0	204	G193	461	7749.0	204	G313	521	6669.0	204	GEXT
402	8811.0	339	G195	462	7731.0	339	G315	522	6651.0	339	DUMMY19
403	8793.0	204	G197	463	7713.0	204	G317	523	6417.0	339	DUMMY20
404	8775.0	339	G199	464	7695.0	339	G319	524	6399.0	204	S720
405	8757.0	204	G201	465	7677.0	204	G321	525	6381.0	339	S719
406	8739.0	339	G203	466	7659.0	339	G323	526	6363.0	204	S718
407	8721.0	204	G205	467	7641.0	204	G325	527	6345.0	339	S717
408	8703.0	339	G207	468	7623.0	339	G327	528	6327.0	204	S716
409	8685.0	204	G209	469	7605.0	204	G329	529	6309.0	339	S715
410	8667.0	339	G211	470	7587.0	339	G331	530	6291.0	204	S714
411	8649.0	204	G213	471	7569.0	204	G333	531	6273.0	339	S713
412	8631.0	339	G215	472	7551.0	339	G335	532	6255.0	204	S712
413	8613.0	204	G217	473	7533.0	204	G337	533	6237.0	339	S711
414	8595.0	339	G219	474	7515.0	339	G339	534	6219.0	204	S710
415	8577.0	204	G221	475	7497.0	204	G341	535	6201.0	339	S709
416	8559.0	339	G223	476	7479.0	339	G343	536	6183.0	204	S708
417	8541.0	204	G225	477	7461.0	204	G345	537	6165.0	339	S707
418	8523.0	339	G227	478	7443.0	339	G347	538	6147.0	204	S706
419	8505.0	204	G229	479	7425.0	204	G349	539	6129.0	339	S705
420	8487.0	339	G231	480	7407.0	339	G351	540	6111.0	204	S704

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
541	6093.0	339	S703	601	5013.0	339	S643	661	3933.0	339	S583
542	6075.0	204	S702	602	4995.0	204	S642	662	3915.0	204	S582
543	6057.0	339	S701	603	4977.0	339	S641	663	3897.0	339	S581
544	6039.0	204	S700	604	4959.0	204	S640	664	3879.0	204	S580
545	6021.0	339	S699	605	4941.0	339	S639	665	3861.0	339	S579
546	6003.0	204	S698	606	4923.0	204	S638	666	3843.0	204	S578
547	5985.0	339	S697	607	4905.0	339	S637	667	3825.0	339	S577
548	5967.0	204	S696	608	4887.0	204	S636	668	3807.0	204	S576
549	5949.0	339	S695	609	4869.0	339	S635	669	3789.0	339	S575
550	5931.0	204	S694	610	4851.0	204	S634	670	3771.0	204	S574
551	5913.0	339	S693	611	4833.0	339	S633	671	3753.0	339	S573
552	5895.0	204	S692	612	4815.0	204	S632	672	3735.0	204	S572
553	5877.0	339	S691	613	4797.0	339	S631	673	3717.0	339	S571
554	5859.0	204	S690	614	4779.0	204	S630	674	3699.0	204	S570
555	5841.0	339	S689	615	4761.0	339	S629	675	3681.0	339	S569
556	5823.0	204	S688	616	4743.0	204	S628	676	3663.0	204	S568
557	5805.0	339	S687	617	4725.0	339	S627	677	3645.0	339	S567
558	5787.0	204	S686	618	4707.0	204	S626	678	3627.0	204	S566
559	5769.0	339	S685	619	4689.0	339	S625	679	3609.0	339	S565
560	5751.0	204	S684	620	4671.0	204	S624	680	3591.0	204	S564
561	5733.0	339	S683	621	4653.0	339	S623	681	3573.0	339	S563
562	5715.0	204	S682	622	4635.0	204	S622	682	3555.0	204	S562
563	5697.0	339	S681	623	4617.0	339	S621	683	3537.0	339	S561
564	5679.0	204	S680	624	4599.0	204	S620	684	3519.0	204	S560
565	5661.0	339	S679	625	4581.0	339	S619	685	3501.0	339	S559
566	5643.0	204	S678	626	4563.0	204	S618	686	3483.0	204	S558
567	5625.0	339	S677	627	4545.0	339	S617	687	3465.0	339	S557
568	5607.0	204	S676	628	4527.0	204	S616	688	3447.0	204	S556
569	5589.0	339	S675	629	4509.0	339	S615	689	3429.0	339	S555
570	5571.0	204	S674	630	4491.0	204	S614	690	3411.0	204	S554
571	5553.0	339	S673	631	4473.0	339	S613	691	3393.0	339	S553
572	5535.0	204	S672	632	4455.0	204	S612	692	3375.0	204	S552
573	5517.0	339	S671	633	4437.0	339	S611	693	3357.0	339	S551
574	5499.0	204	S670	634	4419.0	204	S610	694	3339.0	204	S550
575	5481.0	339	S669	635	4401.0	339	S609	695	3321.0	339	S549
576	5463.0	204	S668	636	4383.0	204	S608	696	3303.0	204	S548
577	5445.0	339	S667	637	4365.0	339	S607	697	3285.0	339	S547
578	5427.0	204	S666	638	4347.0	204	S606	698	3267.0	204	S546
579	5409.0	339	S665	639	4329.0	339	S605	699	3249.0	339	S545
580	5391.0	204	S664	640	4311.0	204	S604	700	3231.0	204	S544
581	5373.0	339	S663	641	4293.0	339	S603	701	3213.0	339	S543
582	5355.0	204	S662	642	4275.0	204	S602	702	3195.0	204	S542
583	5337.0	339	S661	643	4257.0	339	S601	703	3177.0	339	S541
584	5319.0	204	S660	644	4239.0	204	S600	704	3159.0	204	S540
585	5301.0	339	S659	645	4221.0	339	S599	705	3141.0	339	S539
586	5283.0	204	S658	646	4203.0	204	S598	706	3123.0	204	S538
587	5265.0	339	S657	647	4185.0	339	S597	707	3105.0	339	S537
588	5247.0	204	S656	648	4167.0	204	S596	708	3087.0	204	S536
589	5229.0	339	S655	649	4149.0	339	S595	709	3069.0	339	S535
590	5211.0	204	S654	650	4131.0	204	S594	710	3051.0	204	S534
591	5193.0	339	S653	651	4113.0	339	S593	711	3033.0	339	S533
592	5175.0	204	S652	652	4095.0	204	S592	712	3015.0	204	S532
593	5157.0	339	S651	653	4077.0	339	S591	713	2997.0	339	S531
594	5139.0	204	S650	654	4059.0	204	S590	714	2979.0	204	S530
595	5121.0	339	S649	655	4041.0	339	S589	715	2961.0	339	S529
596	5103.0	204	S648	656	4023.0	204	S588	716	2943.0	204	S528
597	5085.0	339	S647	657	4005.0	339	S587	717	2925.0	339	S527
598	5067.0	204	S646	658	3987.0	204	S586	718	2907.0	204	S526
599	5049.0	339	S645	659	3969.0	339	S585	719	2889.0	339	S525
600	5031.0	204	S644	660	3951.0	204	S584	720	2871.0	204	S524

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
721	2853.0	339	S523	781	1773.0	339	S463	841	693.0	339	S403
722	2835.0	204	S522	782	1755.0	204	S462	842	675.0	204	S402
723	2817.0	339	S521	783	1737.0	339	S461	843	657.0	339	S401
724	2799.0	204	S520	784	1719.0	204	S460	844	639.0	204	S400
725	2781.0	339	S519	785	1701.0	339	S459	845	621.0	339	S399
726	2763.0	204	S518	786	1683.0	204	S458	846	603.0	204	S398
727	2745.0	339	S517	787	1665.0	339	S457	847	585.0	339	S397
728	2727.0	204	S516	788	1647.0	204	S456	848	567.0	204	S396
729	2709.0	339	S515	789	1629.0	339	S455	849	549.0	339	S395
730	2691.0	204	S514	790	1611.0	204	S454	850	531.0	204	S394
731	2673.0	339	S513	791	1593.0	339	S453	851	513.0	339	S393
732	2655.0	204	S512	792	1575.0	204	S452	852	495.0	204	S392
733	2637.0	339	S511	793	1557.0	339	S451	853	477.0	339	S391
734	2619.0	204	S510	794	1539.0	204	S450	854	459.0	204	S390
735	2601.0	339	S509	795	1521.0	339	S449	855	441.0	339	S389
736	2583.0	204	S508	796	1503.0	204	S448	856	423.0	204	S388
737	2565.0	339	S507	797	1485.0	339	S447	857	405.0	339	S387
738	2547.0	204	S506	798	1467.0	204	S446	858	387.0	204	S386
739	2529.0	339	S505	799	1449.0	339	S445	859	369.0	339	S385
740	2511.0	204	S504	800	1431.0	204	S444	860	351.0	204	S384
741	2493.0	339	S503	801	1413.0	339	S443	861	333.0	339	S383
742	2475.0	204	S502	802	1395.0	204	S442	862	315.0	204	S382
743	2457.0	339	S501	803	1377.0	339	S441	863	297.0	339	S381
744	2439.0	204	S500	804	1359.0	204	S440	864	279.0	204	S380
745	2421.0	339	S499	805	1341.0	339	S439	865	261.0	339	S379
746	2403.0	204	S498	806	1323.0	204	S438	866	243.0	204	S378
747	2385.0	339	S497	807	1305.0	339	S437	867	225.0	339	S377
748	2367.0	204	S496	808	1287.0	204	S436	868	207.0	204	S376
749	2349.0	339	S495	809	1269.0	339	S435	869	189.0	339	S375
750	2331.0	204	S494	810	1251.0	204	S434	870	171.0	204	S374
751	2313.0	339	S493	811	1233.0	339	S433	871	153.0	339	S373
752	2295.0	204	S492	812	1215.0	204	S432	872	135.0	204	S372
753	2277.0	339	S491	813	1197.0	339	S431	873	117.0	339	S371
754	2259.0	204	S490	814	1179.0	204	S430	874	99.0	204	S370
755	2241.0	339	S489	815	1161.0	339	S429	875	81.0	339	S369
756	2223.0	204	S488	816	1143.0	204	S428	876	63.0	204	S368
757	2205.0	339	S487	817	1125.0	339	S427	877	45.0	339	S367
758	2187.0	204	S486	818	1107.0	204	S426	878	27.0	204	S366
759	2169.0	339	S485	819	1089.0	339	S425	879	9.0	339	S365
760	2151.0	204	S484	820	1071.0	204	S424	880	-9.0	204	S364
761	2133.0	339	S483	821	1053.0	339	S423	881	-27.0	339	S363
762	2115.0	204	S482	822	1035.0	204	S422	882	-45.0	204	S362
763	2097.0	339	S481	823	1017.0	339	S421	883	-63.0	339	S361
764	2079.0	204	S480	824	999.0	204	S420	884	-81.0	204	S360
765	2061.0	339	S479	825	981.0	339	S419	885	-99.0	339	S359
766	2043.0	204	S478	826	963.0	204	S418	886	-117.0	204	S358
767	2025.0	339	S477	827	945.0	339	S417	887	-135.0	339	S357
768	2007.0	204	S476	828	927.0	204	S416	888	-153.0	204	S356
769	1989.0	339	S475	829	909.0	339	S415	889	-171.0	339	S355
770	1971.0	204	S474	830	891.0	204	S414	890	-189.0	204	S354
771	1953.0	339	S473	831	873.0	339	S413	891	-207.0	339	S353
772	1935.0	204	S472	832	855.0	204	S412	892	-225.0	204	S352
773	1917.0	339	S471	833	837.0	339	S411	893	-243.0	339	S351
774	1899.0	204	S470	834	819.0	204	S410	894	-261.0	204	S350
775	1881.0	339	S469	835	801.0	339	S409	895	-279.0	339	S349
776	1863.0	204	S468	836	783.0	204	S408	896	-297.0	204	S348
777	1845.0	339	S467	837	765.0	339	S407	897	-315.0	339	S347
778	1827.0	204	S466	838	747.0	204	S406	898	-333.0	204	S346
779	1809.0	339	S465	839	729.0	339	S405	899	-351.0	339	S345
780	1791.0	204	S464	840	711.0	204	S404	900	-369.0	204	S344

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
901	-387.0	339	S343	961	-1467.0	339	S283	1021	-2547.0	339	S223
902	-405.0	204	S342	962	-1485.0	204	S282	1022	-2565.0	204	S222
903	-423.0	339	S341	963	-1503.0	339	S281	1023	-2583.0	339	S221
904	-441.0	204	S340	964	-1521.0	204	S280	1024	-2601.0	204	S220
905	-459.0	339	S339	965	-1539.0	339	S279	1025	-2619.0	339	S219
906	-477.0	204	S338	966	-1557.0	204	S278	1026	-2637.0	204	S218
907	-495.0	339	S337	967	-1575.0	339	S277	1027	-2655.0	339	S217
908	-513.0	204	S336	968	-1593.0	204	S276	1028	-2673.0	204	S216
909	-531.0	339	S335	969	-1611.0	339	S275	1029	-2691.0	339	S215
910	-549.0	204	S334	970	-1629.0	204	S274	1030	-2709.0	204	S214
911	-567.0	339	S333	971	-1647.0	339	S273	1031	-2727.0	339	S213
912	-585.0	204	S332	972	-1665.0	204	S272	1032	-2745.0	204	S212
913	-603.0	339	S331	973	-1683.0	339	S271	1033	-2763.0	339	S211
914	-621.0	204	S330	974	-1701.0	204	S270	1034	-2781.0	204	S210
915	-639.0	339	S329	975	-1719.0	339	S269	1035	-2799.0	339	S209
916	-657.0	204	S328	976	-1737.0	204	S268	1036	-2817.0	204	S208
917	-675.0	339	S327	977	-1755.0	339	S267	1037	-2835.0	339	S207
918	-693.0	204	S326	978	-1773.0	204	S266	1038	-2853.0	204	S206
919	-711.0	339	S325	979	-1791.0	339	S265	1039	-2871.0	339	S205
920	-729.0	204	S324	980	-1809.0	204	S264	1040	-2889.0	204	S204
921	-747.0	339	S323	981	-1827.0	339	S263	1041	-2907.0	339	S203
922	-765.0	204	S322	982	-1845.0	204	S262	1042	-2925.0	204	S202
923	-783.0	339	S321	983	-1863.0	339	S261	1043	-2943.0	339	S201
924	-801.0	204	S320	984	-1881.0	204	S260	1044	-2961.0	204	S200
925	-819.0	339	S319	985	-1899.0	339	S259	1045	-2979.0	339	S199
926	-837.0	204	S318	986	-1917.0	204	S258	1046	-2997.0	204	S198
927	-855.0	339	S317	987	-1935.0	339	S257	1047	-3015.0	339	S197
928	-873.0	204	S316	988	-1953.0	204	S256	1048	-3033.0	204	S196
929	-891.0	339	S315	989	-1971.0	339	S255	1049	-3051.0	339	S195
930	-909.0	204	S314	990	-1989.0	204	S254	1050	-3069.0	204	S194
931	-927.0	339	S313	991	-2007.0	339	S253	1051	-3087.0	339	S193
932	-945.0	204	S312	992	-2025.0	204	S252	1052	-3105.0	204	S192
933	-963.0	339	S311	993	-2043.0	339	S251	1053	-3123.0	339	S191
934	-981.0	204	S310	994	-2061.0	204	S250	1054	-3141.0	204	S190
935	-999.0	339	S309	995	-2079.0	339	S249	1055	-3159.0	339	S189
936	-1017.0	204	S308	996	-2097.0	204	S248	1056	-3177.0	204	S188
937	-1035.0	339	S307	997	-2115.0	339	S247	1057	-3195.0	339	S187
938	-1053.0	204	S306	998	-2133.0	204	S246	1058	-3213.0	204	S186
939	-1071.0	339	S305	999	-2151.0	339	S245	1059	-3231.0	339	S185
940	-1089.0	204	S304	1000	-2169.0	204	S244	1060	-3249.0	204	S184
941	-1107.0	339	S303	1001	-2187.0	339	S243	1061	-3267.0	339	S183
942	-1125.0	204	S302	1002	-2205.0	204	S242	1062	-3285.0	204	S182
943	-1143.0	339	S301	1003	-2223.0	339	S241	1063	-3303.0	339	S181
944	-1161.0	204	S300	1004	-2241.0	204	S240	1064	-3321.0	204	S180
945	-1179.0	339	S299	1005	-2259.0	339	S239	1065	-3339.0	339	S179
946	-1197.0	204	S298	1006	-2277.0	204	S238	1066	-3357.0	204	S178
947	-1215.0	339	S297	1007	-2295.0	339	S237	1067	-3375.0	339	S177
948	-1233.0	204	S296	1008	-2313.0	204	S236	1068	-3393.0	204	S176
949	-1251.0	339	S295	1009	-2331.0	339	S235	1069	-3411.0	339	S175
950	-1269.0	204	S294	1010	-2349.0	204	S234	1070	-3429.0	204	S174
951	-1287.0	339	S293	1011	-2367.0	339	S233	1071	-3447.0	339	S173
952	-1305.0	204	S292	1012	-2385.0	204	S232	1072	-3465.0	204	S172
953	-1323.0	339	S291	1013	-2403.0	339	S231	1073	-3483.0	339	S171
954	-1341.0	204	S290	1014	-2421.0	204	S230	1074	-3501.0	204	S170
955	-1359.0	339	S289	1015	-2439.0	339	S229	1075	-3519.0	339	S169
956	-1377.0	204	S288	1016	-2457.0	204	S228	1076	-3537.0	204	S168
957	-1395.0	339	S287	1017	-2475.0	339	S227	1077	-3555.0	339	S167
958	-1413.0	204	S286	1018	-2493.0	204	S226	1078	-3573.0	204	S166
959	-1431.0	339	S285	1019	-2511.0	339	S225	1079	-3591.0	339	S165
960	-1449.0	204	S284	1020	-2529.0	204	S224	1080	-3609.0	204	S164

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
1081	-3627.0	339	S163	1141	-4707.0	339	S103	1201	-5787.0	339	S43
1082	-3645.0	204	S162	1142	-4725.0	204	S102	1202	-5805.0	204	S42
1083	-3663.0	339	S161	1143	-4743.0	339	S101	1203	-5823.0	339	S41
1084	-3681.0	204	S160	1144	-4761.0	204	S100	1204	-5841.0	204	S40
1085	-3699.0	339	S159	1145	-4779.0	339	S99	1205	-5859.0	339	S39
1086	-3717.0	204	S158	1146	-4797.0	204	S98	1206	-5877.0	204	S38
1087	-3735.0	339	S157	1147	-4815.0	339	S97	1207	-5895.0	339	S37
1088	-3753.0	204	S156	1148	-4833.0	204	S96	1208	-5913.0	204	S36
1089	-3771.0	339	S155	1149	-4851.0	339	S95	1209	-5931.0	339	S35
1090	-3789.0	204	S154	1150	-4869.0	204	S94	1210	-5949.0	204	S34
1091	-3807.0	339	S153	1151	-4887.0	339	S93	1211	-5967.0	339	S33
1092	-3825.0	204	S152	1152	-4905.0	204	S92	1212	-5985.0	204	S32
1093	-3843.0	339	S151	1153	-4923.0	339	S91	1213	-6003.0	339	S31
1094	-3861.0	204	S150	1154	-4941.0	204	S90	1214	-6021.0	204	S30
1095	-3879.0	339	S149	1155	-4959.0	339	S89	1215	-6039.0	339	S29
1096	-3897.0	204	S148	1156	-4977.0	204	S88	1216	-6057.0	204	S28
1097	-3915.0	339	S147	1157	-4995.0	339	S87	1217	-6075.0	339	S27
1098	-3933.0	204	S146	1158	-5013.0	204	S86	1218	-6093.0	204	S26
1099	-3951.0	339	S145	1159	-5031.0	339	S85	1219	-6111.0	339	S25
1100	-3969.0	204	S144	1160	-5049.0	204	S84	1220	-6129.0	204	S24
1101	-3987.0	339	S143	1161	-5067.0	339	S83	1221	-6147.0	339	S23
1102	-4005.0	204	S142	1162	-5085.0	204	S82	1222	-6165.0	204	S22
1103	-4023.0	339	S141	1163	-5103.0	339	S81	1223	-6183.0	339	S21
1104	-4041.0	204	S140	1164	-5121.0	204	S80	1224	-6201.0	204	S20
1105	-4059.0	339	S139	1165	-5139.0	339	S79	1225	-6219.0	339	S19
1106	-4077.0	204	S138	1166	-5157.0	204	S78	1226	-6237.0	204	S18
1107	-4095.0	339	S137	1167	-5175.0	339	S77	1227	-6255.0	339	S17
1108	-4113.0	204	S136	1168	-5193.0	204	S76	1228	-6273.0	204	S16
1109	-4131.0	339	S135	1169	-5211.0	339	S75	1229	-6291.0	339	S15
1110	-4149.0	204	S134	1170	-5229.0	204	S74	1230	-6309.0	204	S14
1111	-4167.0	339	S133	1171	-5247.0	339	S73	1231	-6327.0	339	S13
1112	-4185.0	204	S132	1172	-5265.0	204	S72	1232	-6345.0	204	S12
1113	-4203.0	339	S131	1173	-5283.0	339	S71	1233	-6363.0	339	S11
1114	-4221.0	204	S130	1174	-5301.0	204	S70	1234	-6381.0	204	S10
1115	-4239.0	339	S129	1175	-5319.0	339	S69	1235	-6399.0	339	S9
1116	-4257.0	204	S128	1176	-5337.0	204	S68	1236	-6417.0	204	S8
1117	-4275.0	339	S127	1177	-5355.0	339	S67	1237	-6435.0	339	S7
1118	-4293.0	204	S126	1178	-5373.0	204	S66	1238	-6453.0	204	S6
1119	-4311.0	339	S125	1179	-5391.0	339	S65	1239	-6471.0	339	S5
1120	-4329.0	204	S124	1180	-5409.0	204	S64	1240	-6489.0	204	S4
1121	-4347.0	339	S123	1181	-5427.0	339	S63	1241	-6507.0	339	S3
1122	-4365.0	204	S122	1182	-5445.0	204	S62	1242	-6525.0	204	S2
1123	-4383.0	339	S121	1183	-5463.0	339	S61	1243	-6543.0	339	S1
1124	-4401.0	204	S120	1184	-5481.0	204	S60	1244	-6561.0	204	DUMMY21
1125	-4419.0	339	S119	1185	-5499.0	339	S59	1245	-6651.0	339	DUMMY22
1126	-4437.0	204	S118	1186	-5517.0	204	S58	1246	-6669.0	204	VGLDMY2
1127	-4455.0	339	S117	1187	-5535.0	339	S57	1247	-6687.0	339	G432
1128	-4473.0	204	S116	1188	-5553.0	204	S56	1248	-6705.0	204	G430
1129	-4491.0	339	S115	1189	-5571.0	339	S55	1249	-6723.0	339	G428
1130	-4509.0	204	S114	1190	-5589.0	204	S54	1250	-6741.0	204	G426
1131	-4527.0	339	S113	1191	-5607.0	339	S53	1251	-6759.0	339	G424
1132	-4545.0	204	S112	1192	-5625.0	204	S52	1252	-6777.0	204	G422
1133	-4563.0	339	S111	1193	-5643.0	339	S51	1253	-6795.0	339	G420
1134	-4581.0	204	S110	1194	-5661.0	204	S50	1254	-6813.0	204	G418
1135	-4599.0	339	S109	1195	-5679.0	339	S49	1255	-6831.0	339	G416
1136	-4617.0	204	S108	1196	-5697.0	204	S48	1256	-6849.0	204	G414
1137	-4635.0	339	S107	1197	-5715.0	339	S47	1257	-6867.0	339	G412
1138	-4653.0	204	S106	1198	-5733.0	204	S46	1258	-6885.0	204	G410
1139	-4671.0	339	S105	1199	-5751.0	339	S45	1259	-6903.0	339	G408
1140	-4689.0	204	S104	1200	-5769.0	204	S44	1260	-6921.0	204	G406

Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME	Pad No	X-pos	Y-pos	NAME
1261	-6939.0	339	G404	1321	-8019.0	339	G284	1381	-9099.0	339	G164
1262	-6957.0	204	G402	1322	-8037.0	204	G282	1382	-9117.0	204	G162
1263	-6975.0	339	G400	1323	-8055.0	339	G280	1383	-9135.0	339	G160
1264	-6993.0	204	G398	1324	-8073.0	204	G278	1384	-9153.0	204	G158
1265	-7011.0	339	G396	1325	-8091.0	339	G276	1385	-9171.0	339	G156
1266	-7029.0	204	G394	1326	-8109.0	204	G274	1386	-9189.0	204	G154
1267	-7047.0	339	G392	1327	-8127.0	339	G272	1387	-9207.0	339	G152
1268	-7065.0	204	G390	1328	-8145.0	204	G270	1388	-9225.0	204	G150
1269	-7083.0	339	G388	1329	-8163.0	339	G268	1389	-9243.0	339	G148
1270	-7101.0	204	G386	1330	-8181.0	204	G266	1390	-9261.0	204	G146
1271	-7119.0	339	G384	1331	-8199.0	339	G264	1391	-9279.0	339	G144
1272	-7137.0	204	G382	1332	-8217.0	204	G262	1392	-9297.0	204	G142
1273	-7155.0	339	G380	1333	-8235.0	339	G260	1393	-9315.0	339	G140
1274	-7173.0	204	G378	1334	-8253.0	204	G258	1394	-9333.0	204	G138
1275	-7191.0	339	G376	1335	-8271.0	339	G256	1395	-9351.0	339	G136
1276	-7209.0	204	G374	1336	-8289.0	204	G254	1396	-9369.0	204	G134
1277	-7227.0	339	G372	1337	-8307.0	339	G252	1397	-9387.0	339	G132
1278	-7245.0	204	G370	1338	-8325.0	204	G250	1398	-9405.0	204	G130
1279	-7263.0	339	G368	1339	-8343.0	339	G248	1399	-9423.0	339	G128
1280	-7281.0	204	G366	1340	-8361.0	204	G246	1400	-9441.0	204	G126
1281	-7299.0	339	G364	1341	-8379.0	339	G244	1401	-9459.0	339	G124
1282	-7317.0	204	G362	1342	-8397.0	204	G242	1402	-9477.0	204	G122
1283	-7335.0	339	G360	1343	-8415.0	339	G240	1403	-9495.0	339	G120
1284	-7353.0	204	G358	1344	-8433.0	204	G238	1404	-9513.0	204	G118
1285	-7371.0	339	G356	1345	-8451.0	339	G236	1405	-9531.0	339	G116
1286	-7389.0	204	G354	1346	-8469.0	204	G234	1406	-9549.0	204	G114
1287	-7407.0	339	G352	1347	-8487.0	339	G232	1407	-9567.0	339	G112
1288	-7425.0	204	G350	1348	-8505.0	204	G230	1408	-9585.0	204	G110
1289	-7443.0	339	G348	1349	-8523.0	339	G228	1409	-9603.0	339	G108
1290	-7461.0	204	G346	1350	-8541.0	204	G226	1410	-9621.0	204	G106
1291	-7479.0	339	G344	1351	-8559.0	339	G224	1411	-9639.0	339	G104
1292	-7497.0	204	G342	1352	-8577.0	204	G222	1412	-9657.0	204	G102
1293	-7515.0	339	G340	1353	-8595.0	339	G220	1413	-9675.0	339	G100
1294	-7533.0	204	G338	1354	-8613.0	204	G218	1414	-9693.0	204	G98
1295	-7551.0	339	G336	1355	-8631.0	339	G216	1415	-9711.0	339	G96
1296	-7569.0	204	G334	1356	-8649.0	204	G214	1416	-9729.0	204	G94
1297	-7587.0	339	G332	1357	-8667.0	339	G212	1417	-9747.0	339	G92
1298	-7605.0	204	G330	1358	-8685.0	204	G210	1418	-9765.0	204	G90
1299	-7623.0	339	G328	1359	-8703.0	339	G208	1419	-9783.0	339	G88
1300	-7641.0	204	G326	1360	-8721.0	204	G206	1420	-9801.0	204	G86
1301	-7659.0	339	G324	1361	-8739.0	339	G204	1421	-9819.0	339	G84
1302	-7677.0	204	G322	1362	-8757.0	204	G202	1422	-9837.0	204	G82
1303	-7695.0	339	G320	1363	-8775.0	339	G200	1423	-9855.0	339	G80
1304	-7713.0	204	G318	1364	-8793.0	204	G198	1424	-9873.0	204	G78
1305	-7731.0	339	G316	1365	-8811.0	339	G196	1425	-9891.0	339	G76
1306	-7749.0	204	G314	1366	-8829.0	204	G194	1426	-9909.0	204	G74
1307	-7767.0	339	G312	1367	-8847.0	339	G192	1427	-9927.0	339	G72
1308	-7785.0	204	G310	1368	-8865.0	204	G190	1428	-9945.0	204	G70
1309	-7803.0	339	G308	1369	-8883.0	339	G188	1429	-9963.0	339	G68
1310	-7821.0	204	G306	1370	-8901.0	204	G186	1430	-9981.0	204	G66
1311	-7839.0	339	G304	1371	-8919.0	339	G184	1431	-9999.0	339	G64
1312	-7857.0	204	G302	1372	-8937.0	204	G182	1432	-10017.0	204	G62
1313	-7875.0	339	G300	1373	-8955.0	339	G180	1433	-10035.0	339	G60
1314	-7893.0	204	G298	1374	-8973.0	204	G178	1434	-10053.0	204	G58
1315	-7911.0	339	G296	1375	-8991.0	339	G176	1435	-10071.0	339	G56
1316	-7929.0	204	G294	1376	-9009.0	204	G174	1436	-10089.0	204	G54
1317	-7947.0	339	G292	1377	-9027.0	339	G172	1437	-10107.0	339	G52
1318	-7965.0	204	G290	1378	-9045.0	204	G170	1438	-10125.0	204	G50
1319	-7983.0	339	G288	1379	-9063.0	339	G168	1439	-10143.0	339	G48
1320	-8001.0	204	G286	1380	-9081.0	204	G166	1440	-10161.0	204	G46

Pad No	X-pos	Y-pos	NAME
1441	-10179.0	339	G44
1442	-10197.0	204	G42
1443	-10215.0	339	G40
1444	-10233.0	204	G38
1445	-10251.0	339	G36
1446	-10269.0	204	G34
1447	-10287.0	339	G32
1448	-10305.0	204	G30
1449	-10323.0	339	G28
1450	-10341.0	204	G26
1451	-10359.0	339	G24
1452	-10377.0	204	G22
1453	-10395.0	339	G20
1454	-10413.0	204	G18
1455	-10431.0	339	G16
1456	-10449.0	204	G14
1457	-10467.0	339	G12
1458	-10485.0	204	G10
1459	-10503.0	339	G8
1460	-10521.0	204	G6
1461	-10539.0	339	G4
1462	-10557.0	204	G2
1463	-10575.0	339	VGLDMY3
1464	-10593.0	204	DUMMYR9
1465	-10611.0	339	DUMMYR10
1466	-10629.0	204	DUMMY23
1467	-10647.0	339	DUMMY24