DATA SHEET

(DOC No. HX8347-I(N)-DS)

HX8347-I(N)

240RGB x 320 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 Oct., 2011

Himax Technologies, Inc.
http://www.himax.com.tw

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Revision History

Oct., 2011

Version	Date	Description of Changes
01	2011/10/24	New setup

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1. General Description

This document describes Himax's HX8347-I 240RGBx320 dots resolution driving controller. The HX8347-I is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-I can be operated in low-voltage (1.4V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-I also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-I supports three interface groups: Command-Parameter interface group, Register-Content interface group and RGB interface mode. Command-Parameter interface mode and Register-Content interface mode are selected by the external pin IFSEL setting, and RGB interface mode is selected by Software setting **RCM[1:0]**. This manual description focuses on Command-Parameter interface mode and RGB interface mode, about the Register-Content interface mode; please refer to the HX8347-I (T) datasheet for detail.

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2.Features

2.1 Display

- Resolution:
  - 240(H) x RGB(H) x 320(V)
- Display Color modes
  - Normal Display Mode On
    1. System Interface Circuit
       a. Full color mode:
          – 262k colours (18bit 6(R):6(G):6(B))
       b. Reduce color mode:
          – 65k colours (16bit 5(R):6(G):5(B))
          – 4096 colours(12bit 4(R):4(G):4(B))
    2. RGB Interface Circuit
       a. 65,536(R(5),G(6),B(5)) colors
       b. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    – 8 (R(1),G(1),B(1)) colors

2.2 Display module

- Frame Memory area 240 (H) x 320 (V) x 18 bit
- On module DC/DC converter
- DDVDH = 5.0 V for two time pump (Power supply for driver circuit range)
- VREG1 = 3.3V to 4.8V (Source output voltage range)
- VGH = +9.0 to +14.5V (Positive Gate output voltage range)
- VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- VCOMH = 2.5V to 4.8V, 15mv/step (Common electrode output high voltage)
- VCOML = -2.5V to 0.0V, 15mv/step (Common electrode output low voltage)

2.3 Display control interface

- Display Interface types supported
  - System interface:
    1. 8-/9-/16-/18-bit parallel bus system interface
    2. 3-wire & 4-wire serial bus system interface
  - RGB interface:
    1. 6-/16-/18-bit RGB interface
- Color modes
  - 12 bit/pixel: R(4), G(4), B(4)
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)

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2.4 Input power

- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.3V ~ 3.3V
- OTP programming voltage (VPP): 6.5V ± 0.2V

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support 1~7 Line inversion or Farme inversion
- Support Area scrolling
- Support Partial display mode
- Support Color enhancement function
- Support normal black/normal white LCD
- Support wide view angle display
- On-chip OTP (One-time-programming) and MTP(three-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function
- Operating temperature range : -40℃~ 85℃

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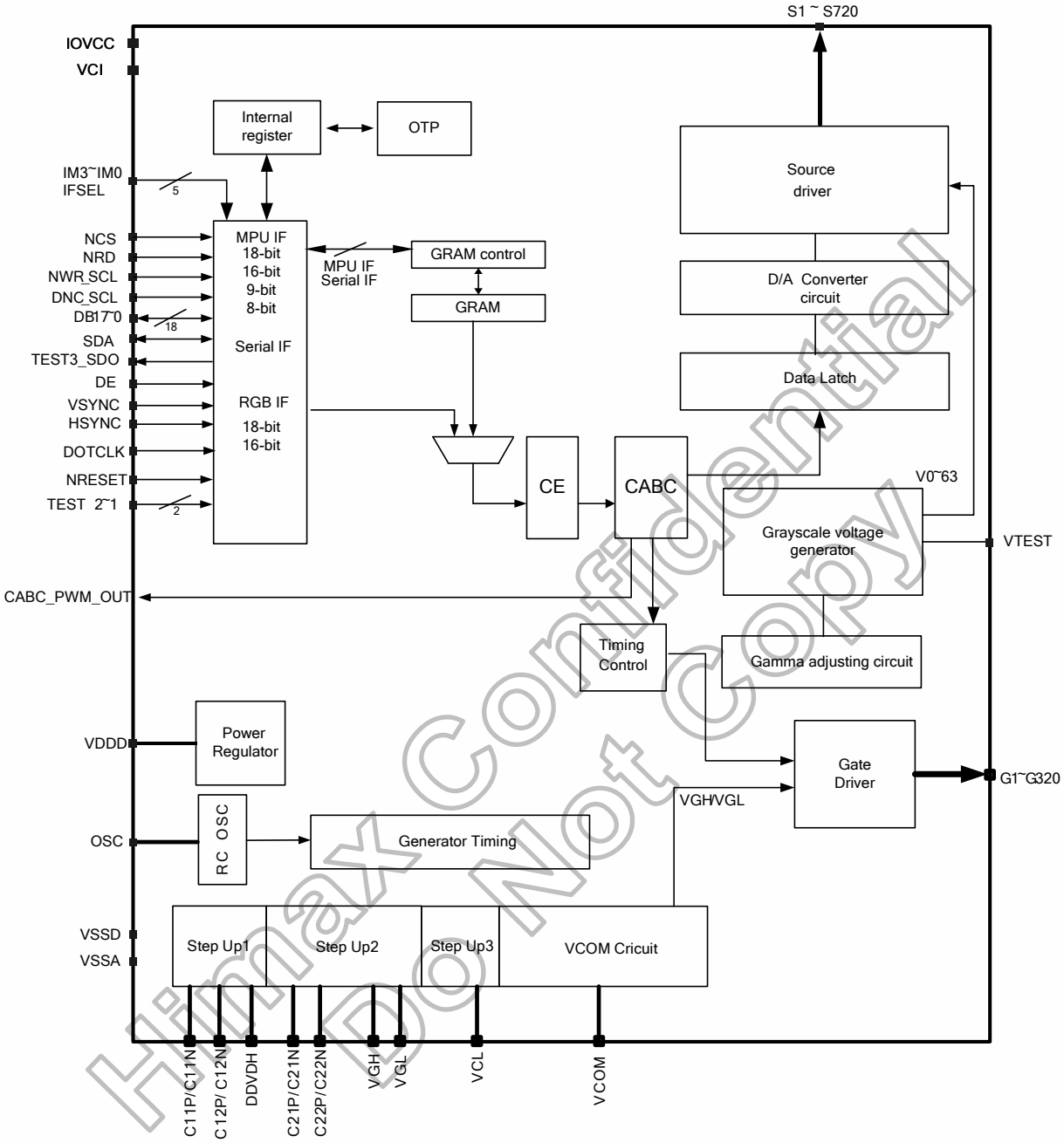
3.Block Diagram

3.1 Block diagram



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3.2 Pin description

<table>
<tr><th colspan="5">Interface Logic Pin</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IFSEL</td><td>I</td><td>1</td><td>MPU</td><td>Interface format select pin
<table><tr><th>IFSEL</th><th>Interface Format Selection</th></tr><tr><td>1</td><td>Command-Parameter interface mode</td></tr><tr><td>0</td><td>Register-content interface mode</td></tr></table>In this document, the IFSEL has to be connected to IOVCC and Command-Parameter interface mode is select.</td></tr>
<tr><td>IM3, IM2,IM1,IM0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bits Parallel type I</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 16-bits Parallel type I</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 9-bits Parallel type I</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bits Parallel type I</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire Serial interface type I</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire Serial interface type I</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bits Parallel type II</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bits Parallel type II</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel type II</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel type II</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire Serial interface type II</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire Serial interface type II</td></tr></table>If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>NWR_SCL</td><td>I</td><td>1</td><td>MPU</td><td>(NWR) Write enable pin I80 parallel bus system interface.
(SCL) server as serial data clock in serial bus system interface when IFSEL=0.
Fix it to IOVCC or VSSD level when not used.</td></tr>
<tr><td>NRD</td><td>I</td><td>1</td><td>MPU</td><td>(NRD) Read enable pin I80 parallel bus system interface.
If not used, please fix this pin at IOVCC or GND level</td></tr>
<tr><td>SDA</td><td>I/O</td><td>1</td><td>MCU</td><td>Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal.
If not used, please let it open</td></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td>(DNC) Command / parameter or display data selection pin.
(SCL) server as serial data clock in serial bus system interface when IFSEL=1.
If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Vertical synchronizing signal in RGB interface.
Has to be fixed to VSSD level or let to open if it is not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Horizontal synchronizing signal in RGB interface.
Has to be fixed to VSSD level or let to open if it is not used.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode.
Has to be fixed to VSSD level or let to open if it is not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Data enable signal in RGB interface.
Has to be fixed to VSSD level or let to open if it is not used.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>DB17~0</td><td>I/O</td><td>18</td><td>MPU</td><td>18-bit bi-directional data bus.
The unused pins let to open or connected to VSSD.</td></tr>
</table>

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Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	8	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
CABC_PWM_OUT	O	1	Backlight Circuit	CABC backlight control PWM signal output
BC_CTL	O	1	Backlight Circuit	LED Driver Enable Signal. If not used, please open this pin.
TEST3/SDO	O	1	MPU	Serial data output pin (SDO) in serial bus system interface II. If not used, please open this pin.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11P,C11N C12P, C12N	I/O	7,7,7,7	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C21P,C21N C22P,C22N	I/O	2,2,2,2	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	7	Power Supply	Digital IO Pad power supply
VCI	P	8	Power Supply	Analog power supply
VSSD	P	8	Ground	Digital ground
VSSC	P	9	Ground	Charge pump ground
VSSA	P	7	Ground	Analog ground
VDDD	O	14	Stabilizing capacitor	Output from internal logic voltage . Connect to a stabilizing capacitor
VREG1	P	4	OPEN	Internal generated stable power for source driver unit.
VCL	P	8	Stabilizing capacitor	An output from the step-up circuit3. A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	7	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	P	5	Stabilizing capacitor	A positive power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGH.
VGL	P	6	Stabilizing capacitor	A negative power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGL.

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Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST2-1	I	2	GND	Test pin input (Internal pull low). Disconnect it.
OSC	I	1	Open	A test pin. Disconnect it.
DUMMY	-	64	Open	Dummy pads
VPP_OTP	-	7	Power supply	Power supply pin used in OTP program mode and operates at 6.5V ± 0.2. If not in OTP program mode, please let it open.

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4. Interface

The HX8347-I supports two-type interface group: Command-Parameter interface group, Register-Content interface group.

This manual description focuses on Command-Parameter interface group. About the Register-Content interface mode, please refer to the HX8347-I(T) datasheet for detail.

In Command-Parameter interface group (IFSEL = 'H'), the HX8347-I has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8347-I shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

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4.1 System interface circuit

The system interface circuit in HX8347-I supports 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU. The input bus width format of system interface circuit is selected by external pins IM(3-0) setting. For selecting the input bus format, please refer to Table 4.1

In MPU interface, it includes command code and the following parameter and GRAM data. The command code can be written through data bus by setting DNC_SCL=0. Then the parameter or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

IM3	IM2	IM1	IM0	Interface	DNC_SCL	NWR_SCL	Data Bus use	
							Register/Content	GRAM
0	0	0	0	8080 MCU 8-bits Parallel type I	DNC	NWR	DB7-DB0	DB7-DB0: 8-bits Data
0	0	0	1	8080 MCU 16-bits Parallel type I	DNC	NWR	DB7-DB0	DB15-DB0: 16-bit Data
0	0	1	0	8080 MCU 9-bits Parallel type I	DNC	NWR	DB7-DB0	DB8-DB0: 9-bits Data
0	0	1	1	8080 MCU 18-bits Parallel type I	DNC	NWR	DB7-DB0	DB17-DB0: 18-bits Data
0	1	0	1	3-wire Serial interface type I	SCL	-	SDA	
0	1	1	0	4-wire Serial interface type I	SCL	DNC	SDA	
1	0	0	0	8080 MCU 16-bits Parallel type II	DNC	NWR	DB8-DB1	DB17-10, DB8-DB1: 16-bit Data
1	0	0	1	8080 MCU 8-bits Parallel type II	DNC	NWR	DB17-DB10	DB17-DB10: 8-bits Data
1	0	1	0	8080 MCU 18-bits Parallel type II	DNC	NWR	DB8-DB1	DB17-DB0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel type II	DNC	NWR	DB17-DB10	DB17-DB9: 9-bits Data
1	1	0	1	3-wire Serial interface type II	SCL	-	SDI/SDO	
1	1	1	0	4-wire Serial interface type II	SCL	DNC	SDI/SDO	
Other Setting				Setting Invalid				

Table 4-1: MPU seletiocn in interface circuit

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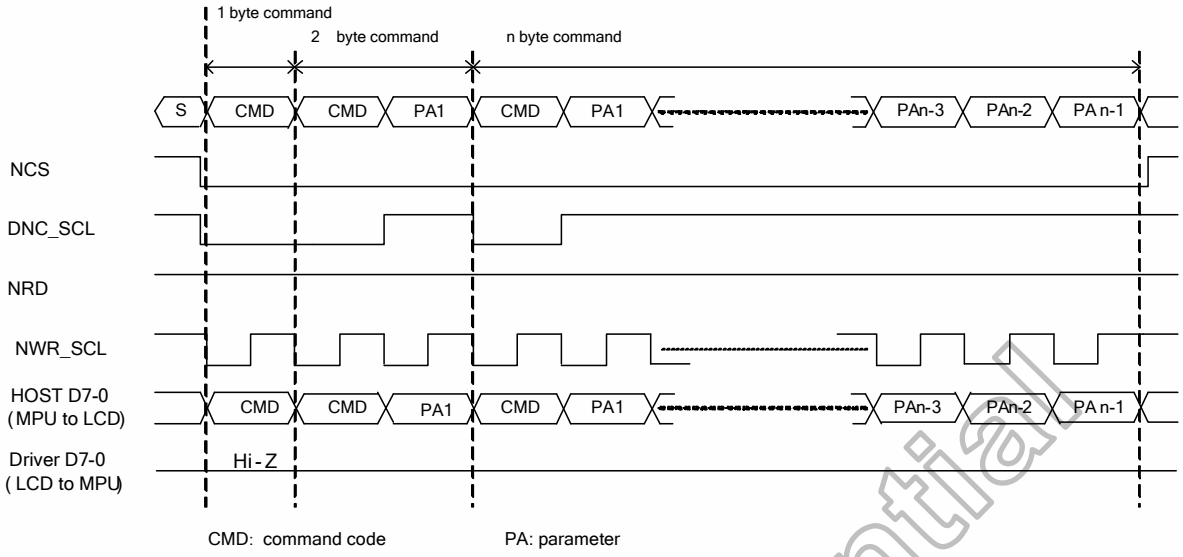
Write to register



Read from register

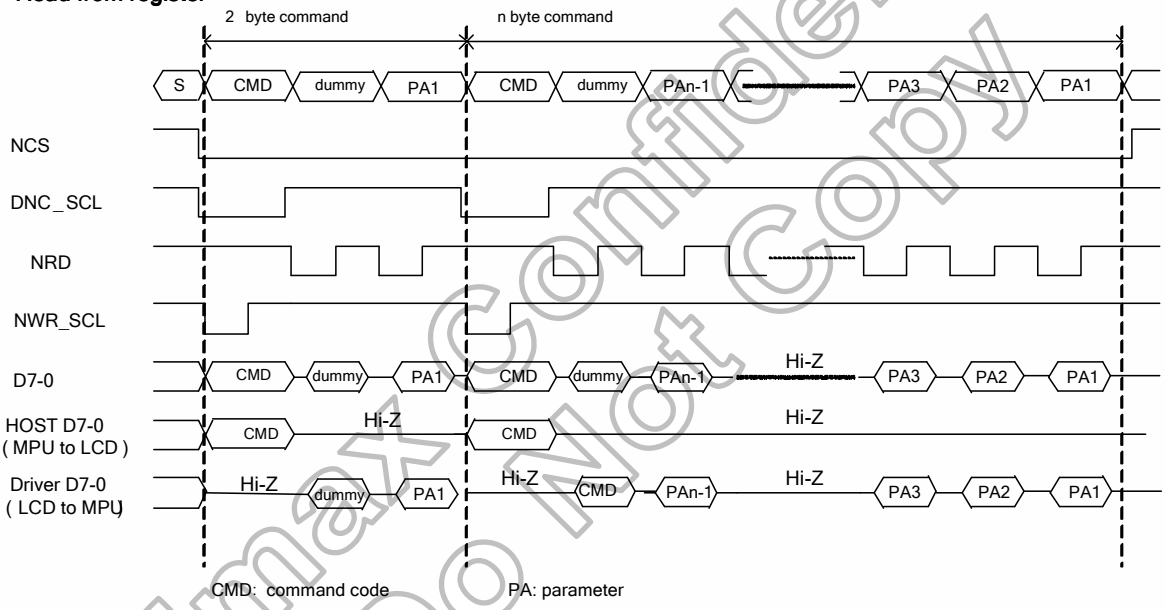


Figure 4-1: Register read/write timing in parallel bus system interface (for I80 series MPU)

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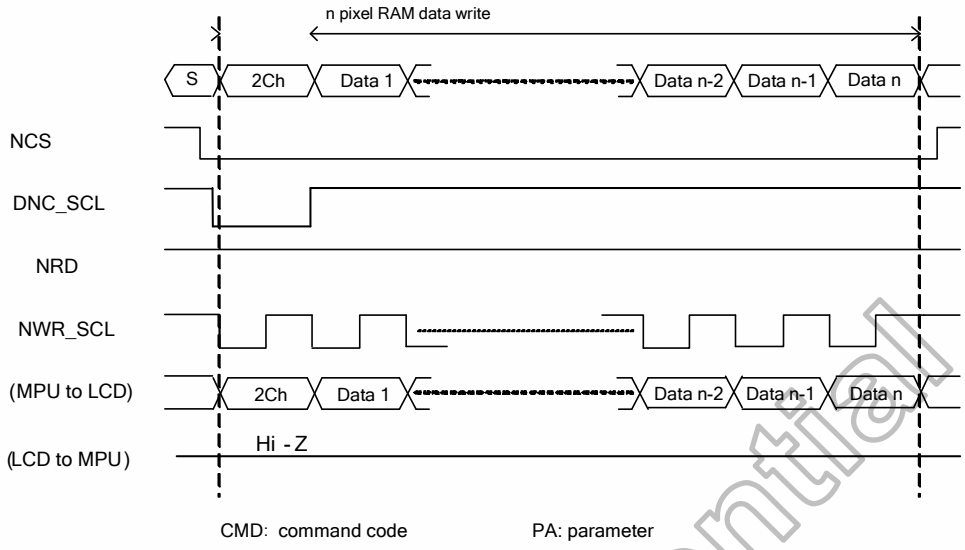
Write to GRAM



Read from GRAM

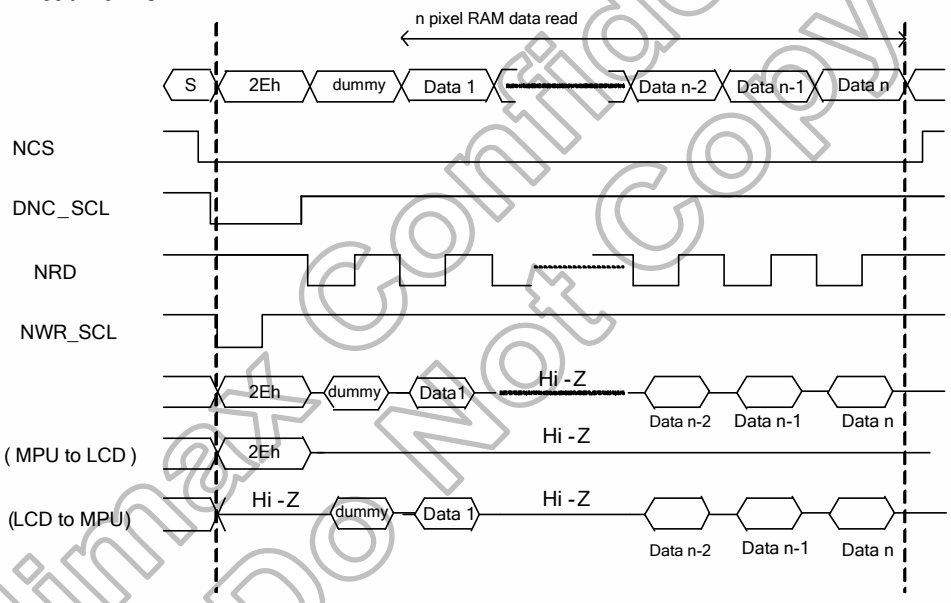


Figure 4-2: GRAM read/write timing in parallel bus system interface (for I80 series MPU)

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4.1.1 MCU data color coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	X	X	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixels/ 3-bytes)
	X	X	X	X	X	X	X	X	X	X	B3	B2	B1	B0	R3	R2	R1	R0	
	X	X	X	X	X	X	X	X	X	X	G3	G2	G1	G0	B3	B2	B1	B0	
05h	X	X	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
	X	X	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0	
06h	X	X	X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	X	X	X	X	X	X	X	X	X	X	G5	G4	G3	G2	G1	G0	x	x	
	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0	x	x	

Table 4-2: 8-bit parallel interface type I GRAM write table

- Parallel 16-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	X	X	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
05h	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
06h	X	X	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	X	X	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	X	X	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4-3: 16-bit parallel interface type I GRAM write table

- Parallel 9-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	X	X	X	X	X	X	X	X	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	X	X	X	X	X	X	X	X	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4-4: 9-bit parallel interface type I GRAM write table

- Parallel 18-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 4-5: 18-bit parallel interface type I GRAM write table

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- Parallel 8-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixels/ 3-bytes)
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixels/ 2-bytes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 4-6: 8-bit parallel interface type II GRAM write table

- Parallel 16-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
									x	0	0	1	0	1	1	0	0	x	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4K-Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 4-7: 16-bit parallel interface type II GRAM write set table

- Parallel 9-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	**2CH**
3AH	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 4-8: 9-bit parallel interface set type II GRAM write table

- Parallel 18-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	x	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 4-9: 18-bit parallel interface type II GRAM write set table

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8-bit parallel bus system interface

The I80-system 8-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0000”. And I80-system 8-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “1001”. Figure 4.3 is the example of type I interface with I80 microcomputer system interface. And Figure 4.4 is the example of type II interface with I80 microcomputer system interface.

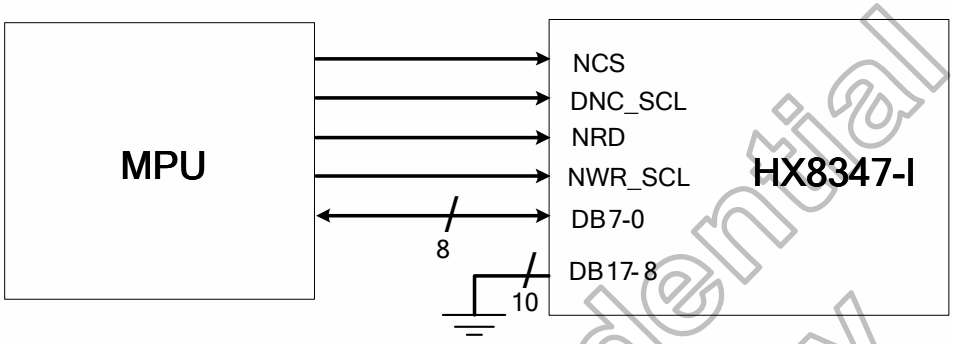

Figure 4-3: Example of I80- system 8-bit parallel bus interface type I

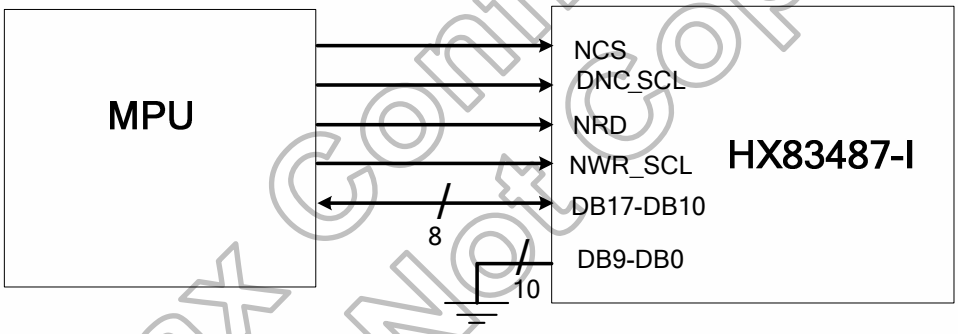

Figure 4-4: Example of I80-system 8-bit parallel bus interface type II

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8-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colors, 3AH="03h"
There are 2-pixels (6 sub-pixels) per 3-bytes.

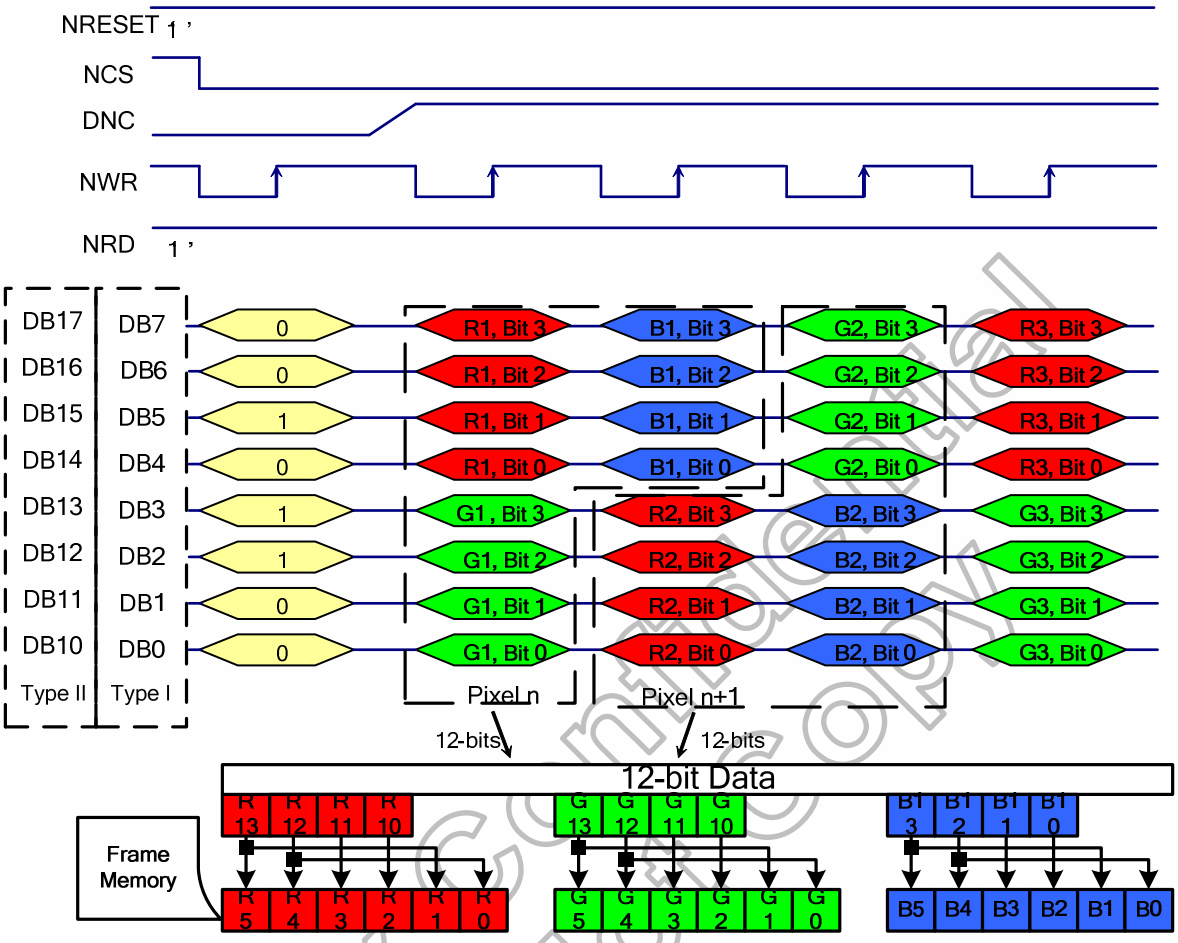

Figure 4-5: Write data for RGB 4-4-4 (4k colors) bits input in 8-bit parallel Interface

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8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH="05h"
There is 1-pixel (3 sub-pixels) per 2-bytes.

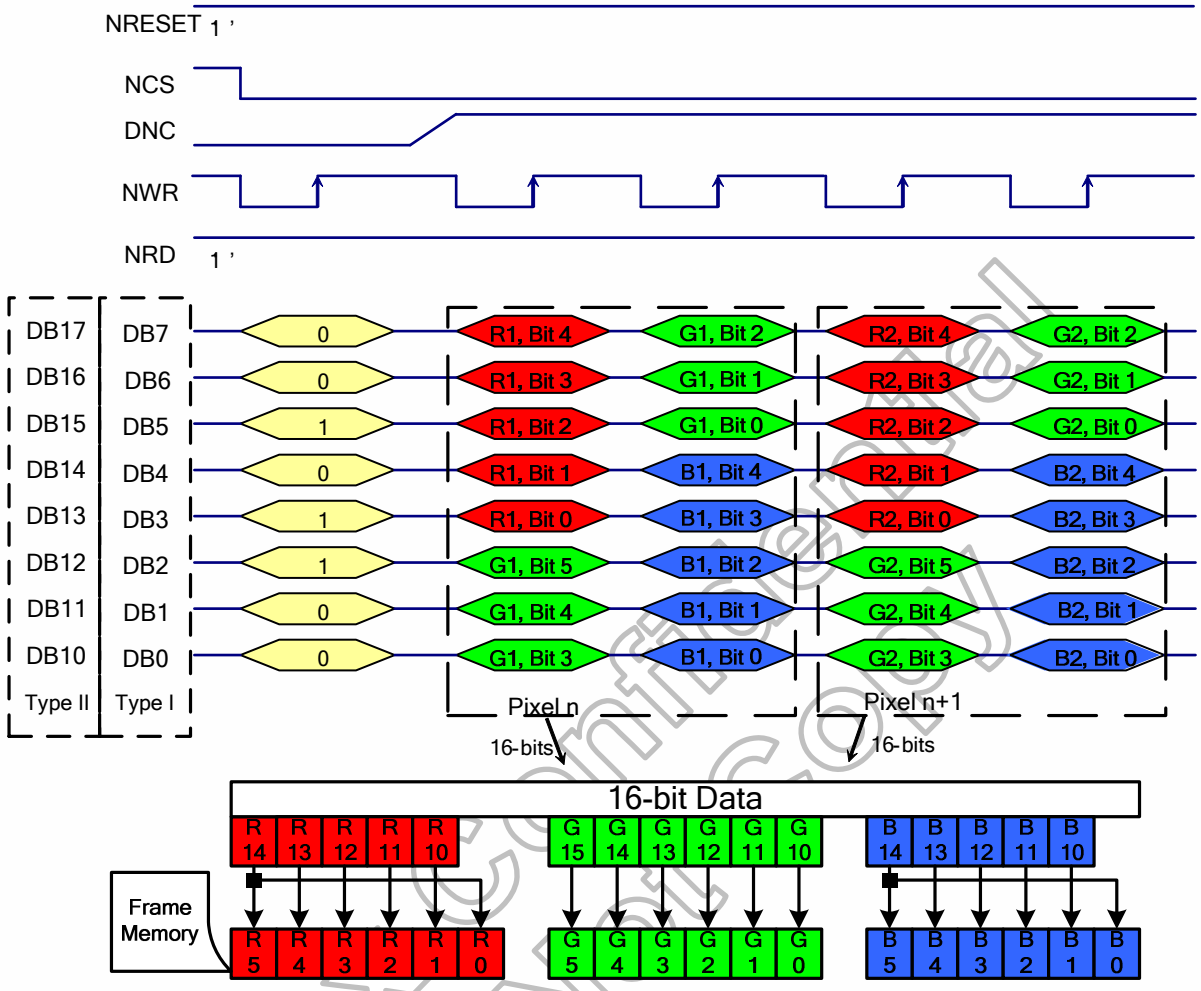

Figure 4-6: Write data for RGB 5-6-5 (65k colors) bits input in 8-bit parallel Interface(EPF[1:0] = 2'b00)

Note: If R[4:0] = B[4:0], R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]} when EPF[1:0] = 2'b11

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8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 3-bytes.

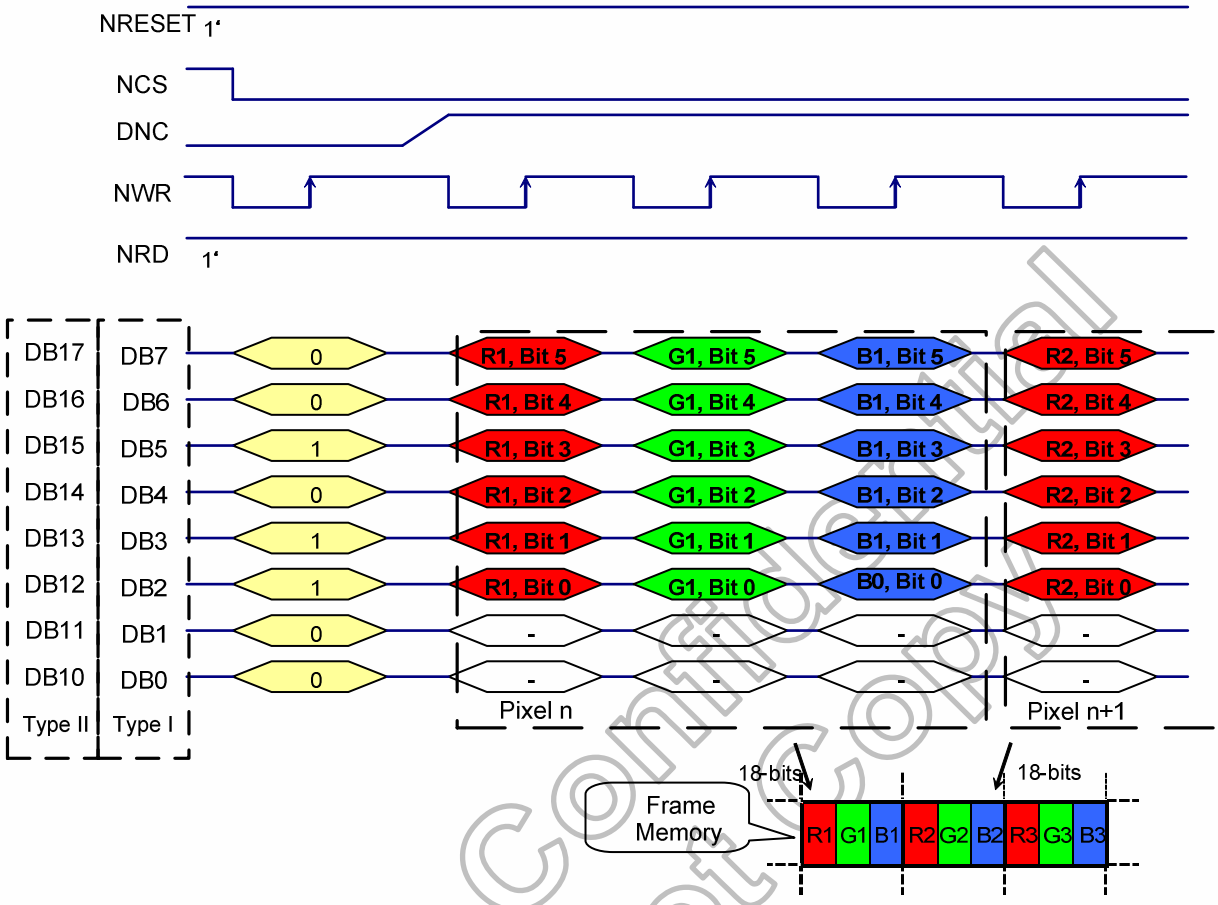

Figure 4-7: Write data for RGB 6-6-6-bits(262k colors) input in 8-bit parallel Interface

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16-bit parallel bus system interface

The I80-system 16-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, IM0” pins to “0001”. And I80-system 16-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, IM0” pins to “1000”. Figure 4.11 is the example of type I interface with I80 microcomputer system interface. And Figure 4.12 is the example of type II interface with I80 microcomputer system interface.

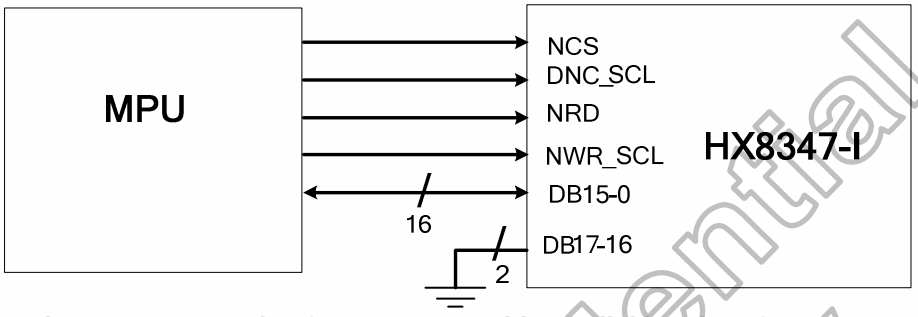

Figure 4-8: Example of I80 system 16-bit parallel bus interface type I

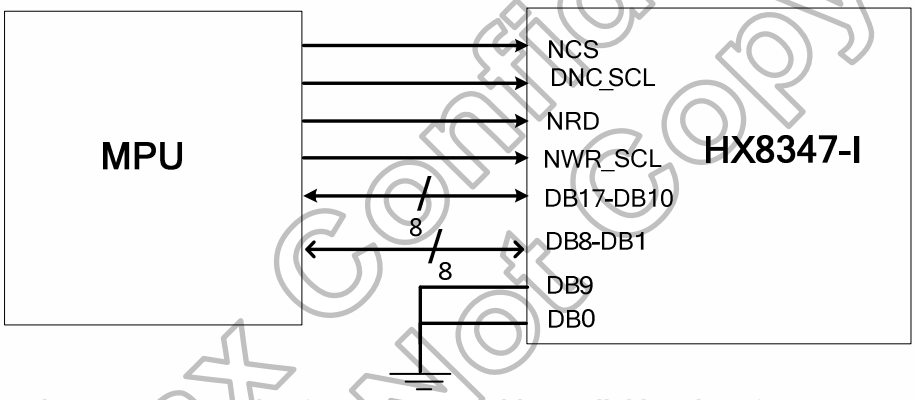

Figure 4-9: Example of I80 system 16-bit parallel bus interface type II

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16-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colors, 3AH="03h"

There is 1-pixel (3 sub-pixels) per 1-byte

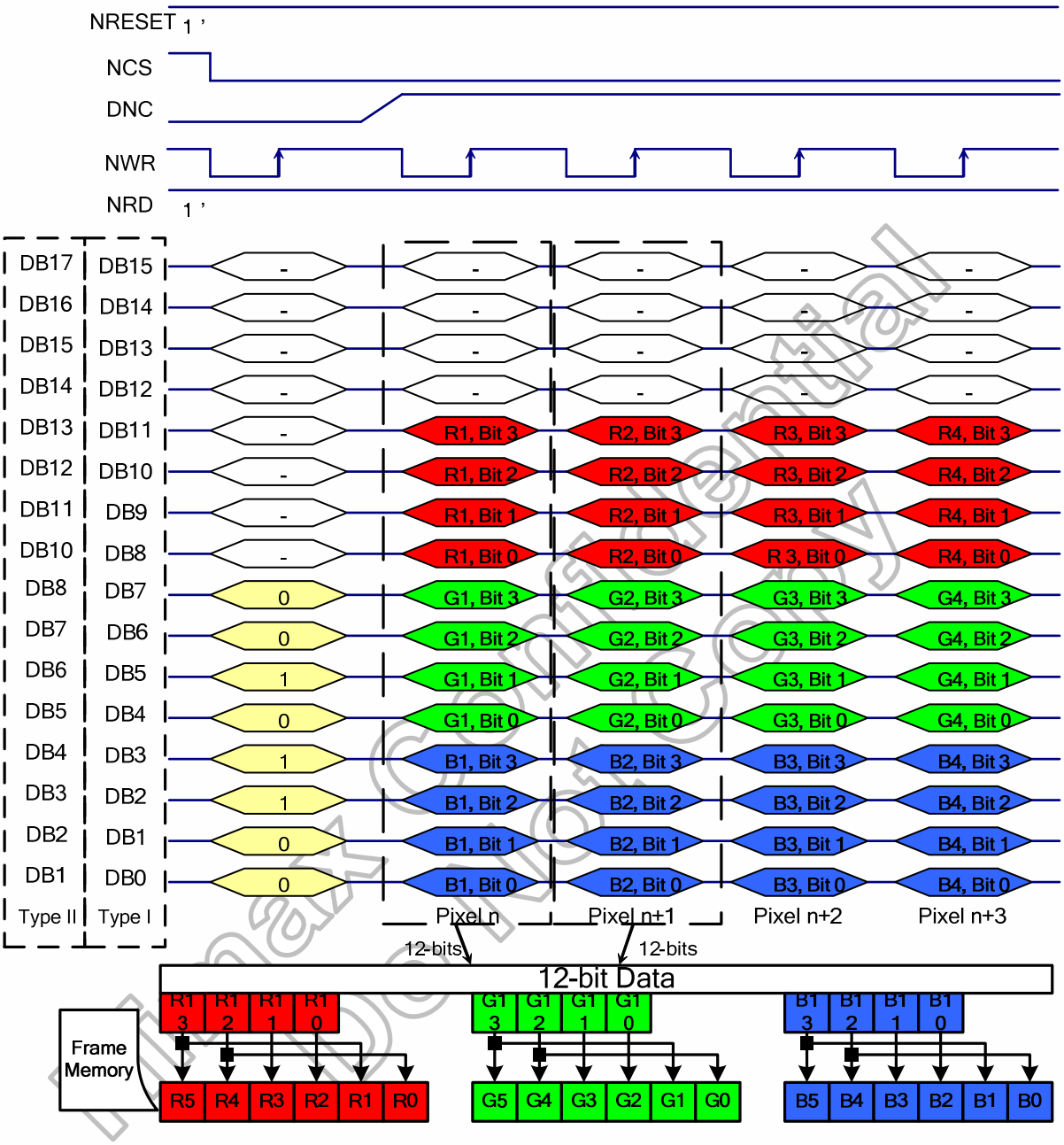

Figure 4-10: Write data for RGB 4-4-4 (4k colors) bits input in 16-bit parallel Interface

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16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH="05h"
There is 1-pixel (3 sub-pixels) per 1-byte

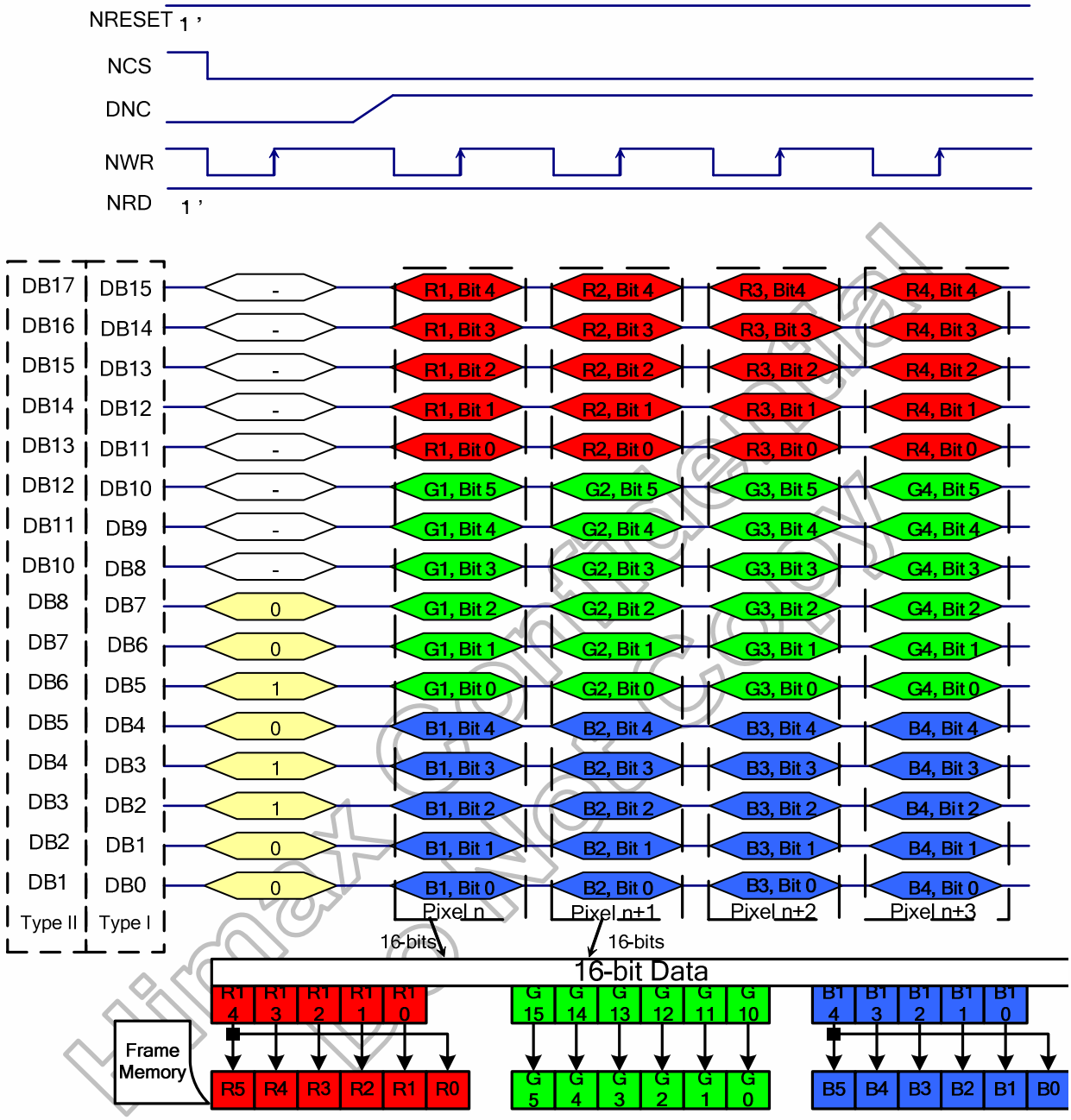

Figure 4-11: Write data for RGB 5-6-5 (65k colors) bits input in 16-bit parallel Interface(EPF[1:0] = 2'b00)

Note: If R[4:0] = B[4:0], R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]} when EPF[1:0] = 2'b11

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16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There are 2-pixels (6 sub-pixels) per 3-bytes

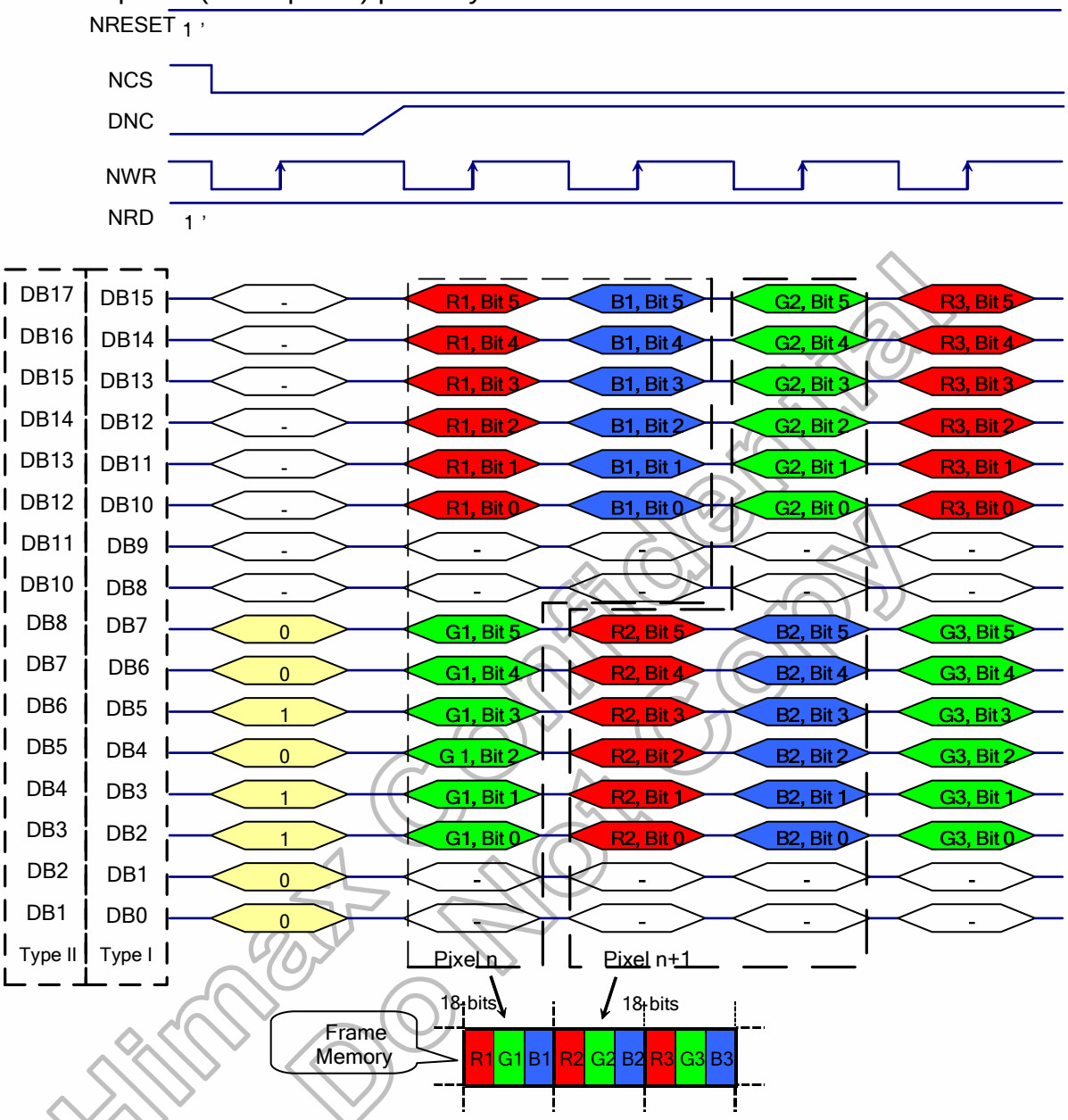

Figure 4-12: Write data for RGB 6-6-6 (262k colors) bits input in 16-bit parallel Interface

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9-bit parallel bus system interface

The I80-system 9-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0010”. And I80-system 9-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, IM0” pins to “1011”. Figure 4.19 is the example of type I interface with I80 microcomputer system interface. And Figure 4.20 is the example of type II interface with I80 microcomputer system interface.

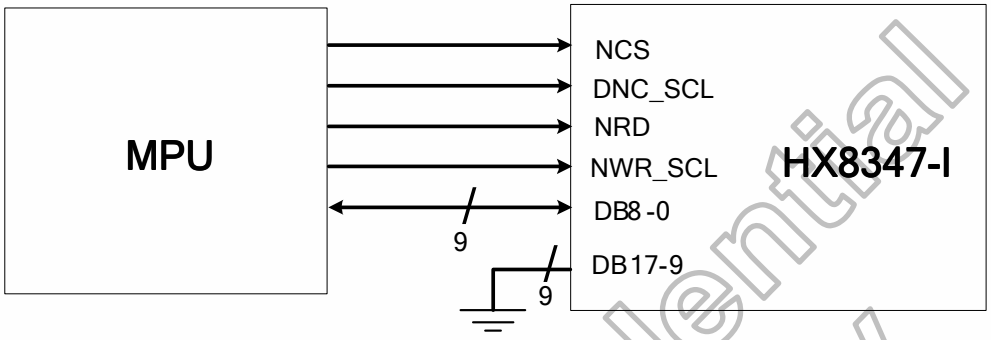

Figure 4-13: Example of I80 system 9-bit parallel bus interface type I

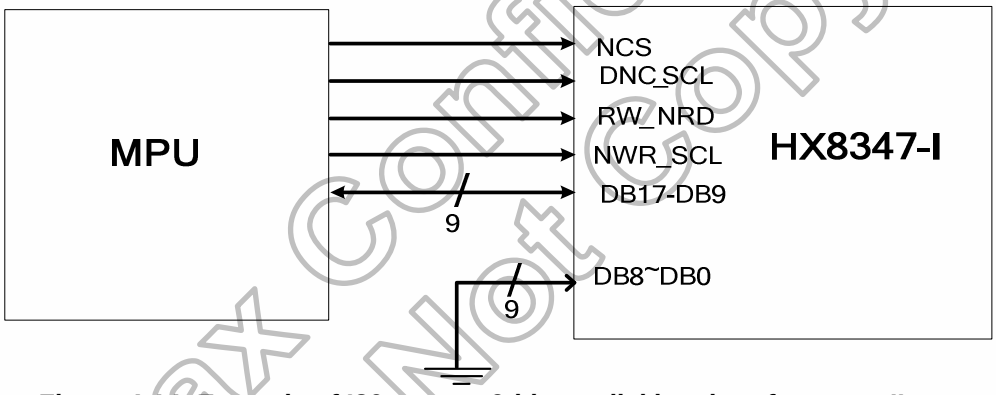

Figure 4-14: Example of I80 system 9-bit parallel bus interface type II

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9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 2-bytes

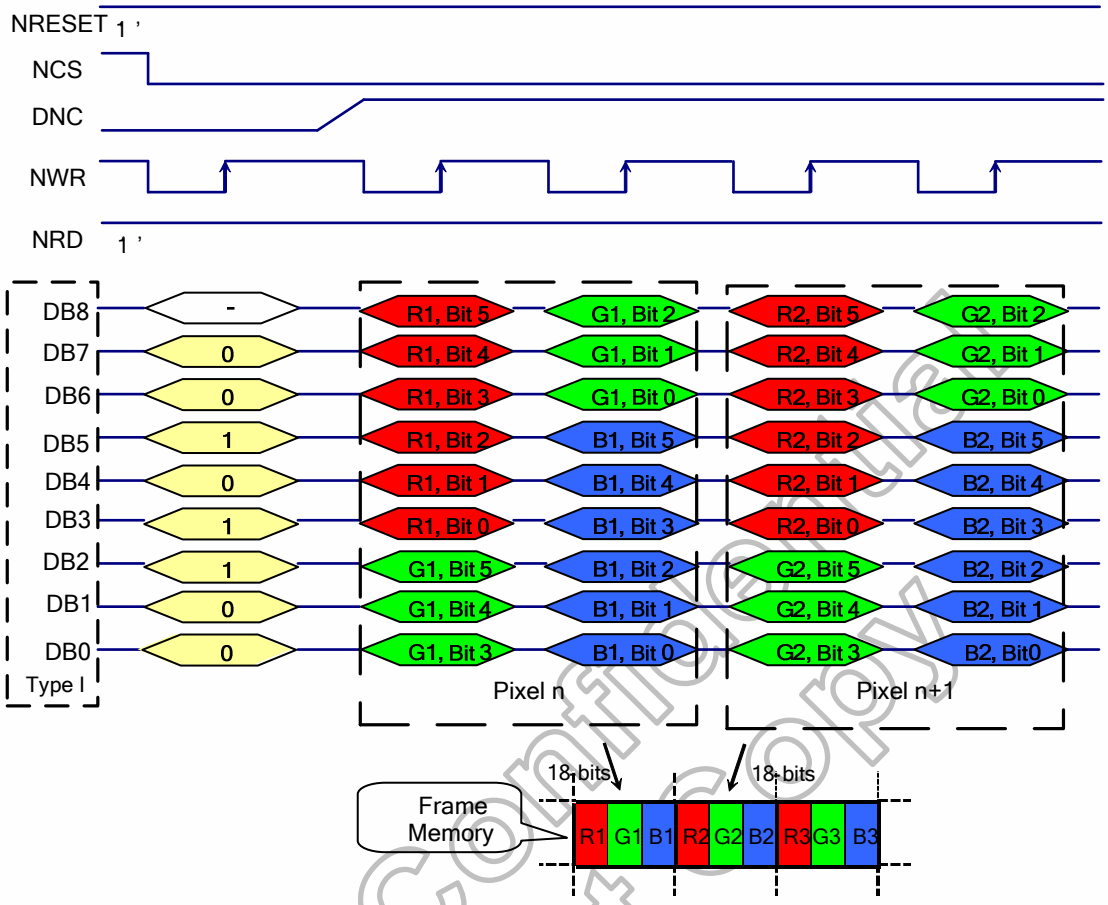

Figure 4-15: Write data for RGB 6-6-6 (262k colors) bits input in 8-bit parallel Interface type I

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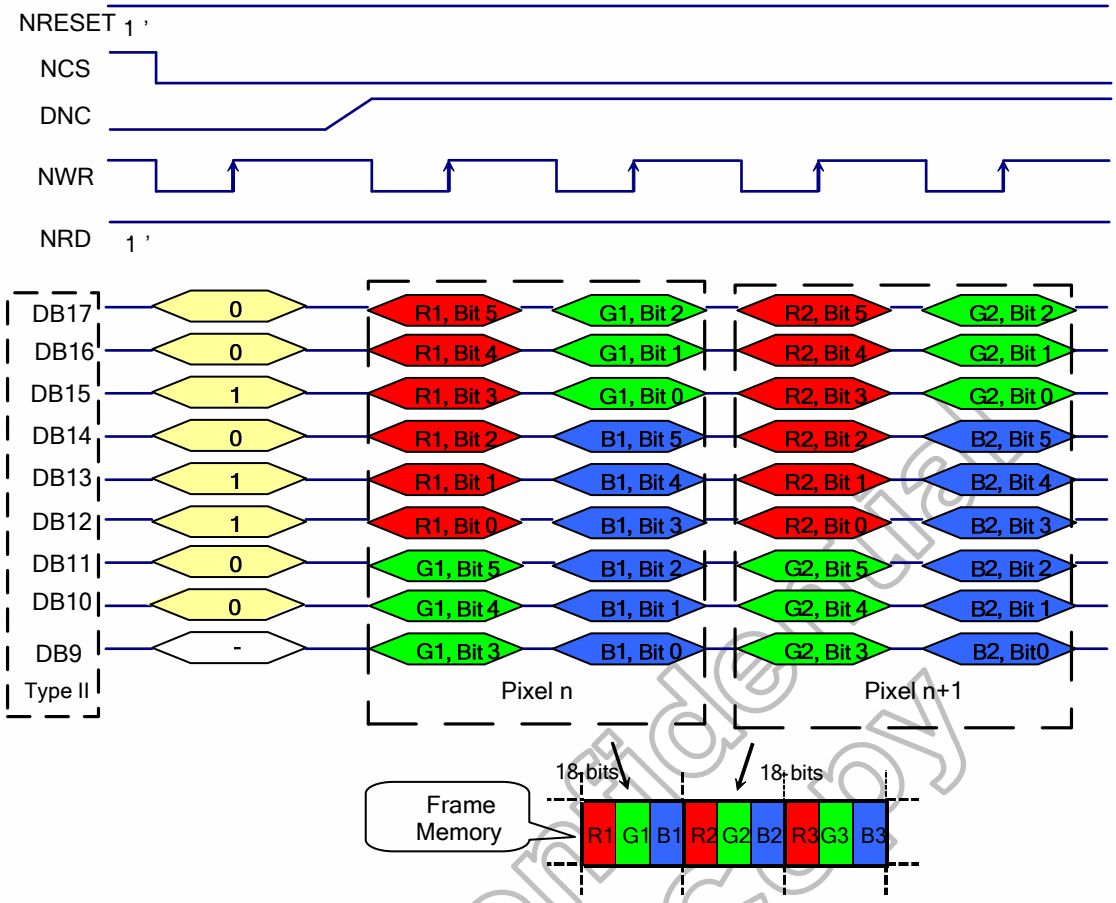

Figure 4-16: Write data for RGB 6-6-6 (262k colors) bits input in 9-bit parallel Interface type II

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18-bit parallel bus system interface

The I80-system 18-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0011”. And the I80-system 18-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, IM0” pins to “1010”. Figure 4.17 is the example of interface with I80 microcomputer system interface.

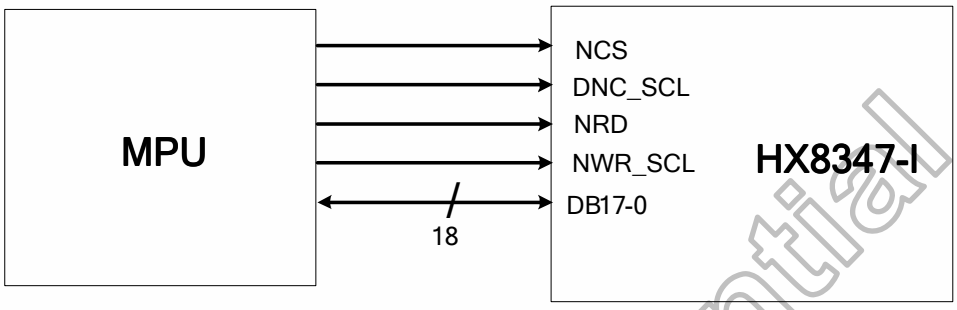

Figure 4-17: Example of I80- system 18-bit parallel bus interface

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18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (6 sub-pixels) per 1-byte

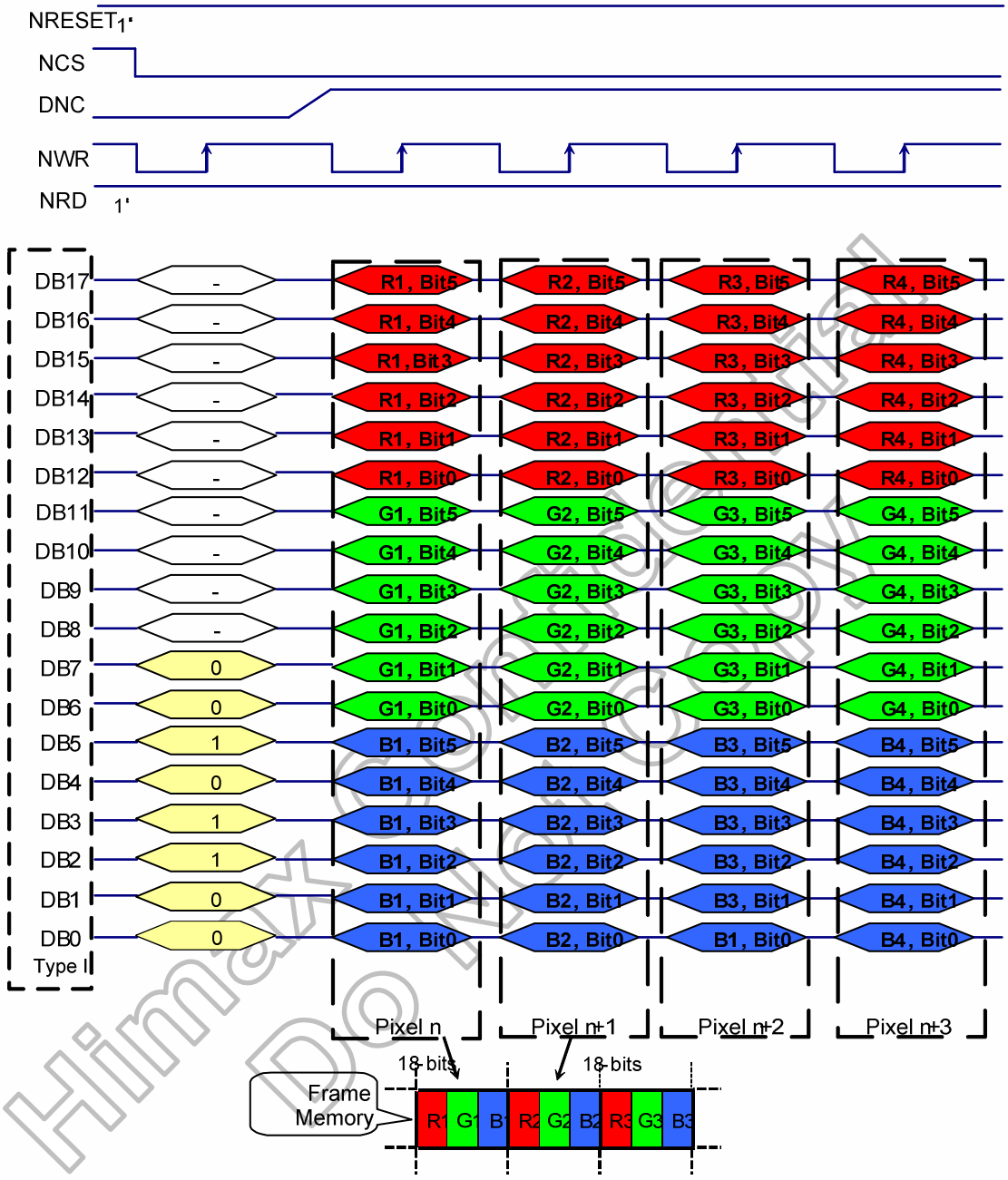

Figure 4-18: Input data bus and GRAM data mapping in 18-bit bus system interface I with 18-bit-data Input ("IM3, IM2, IM1, IM"="0011")

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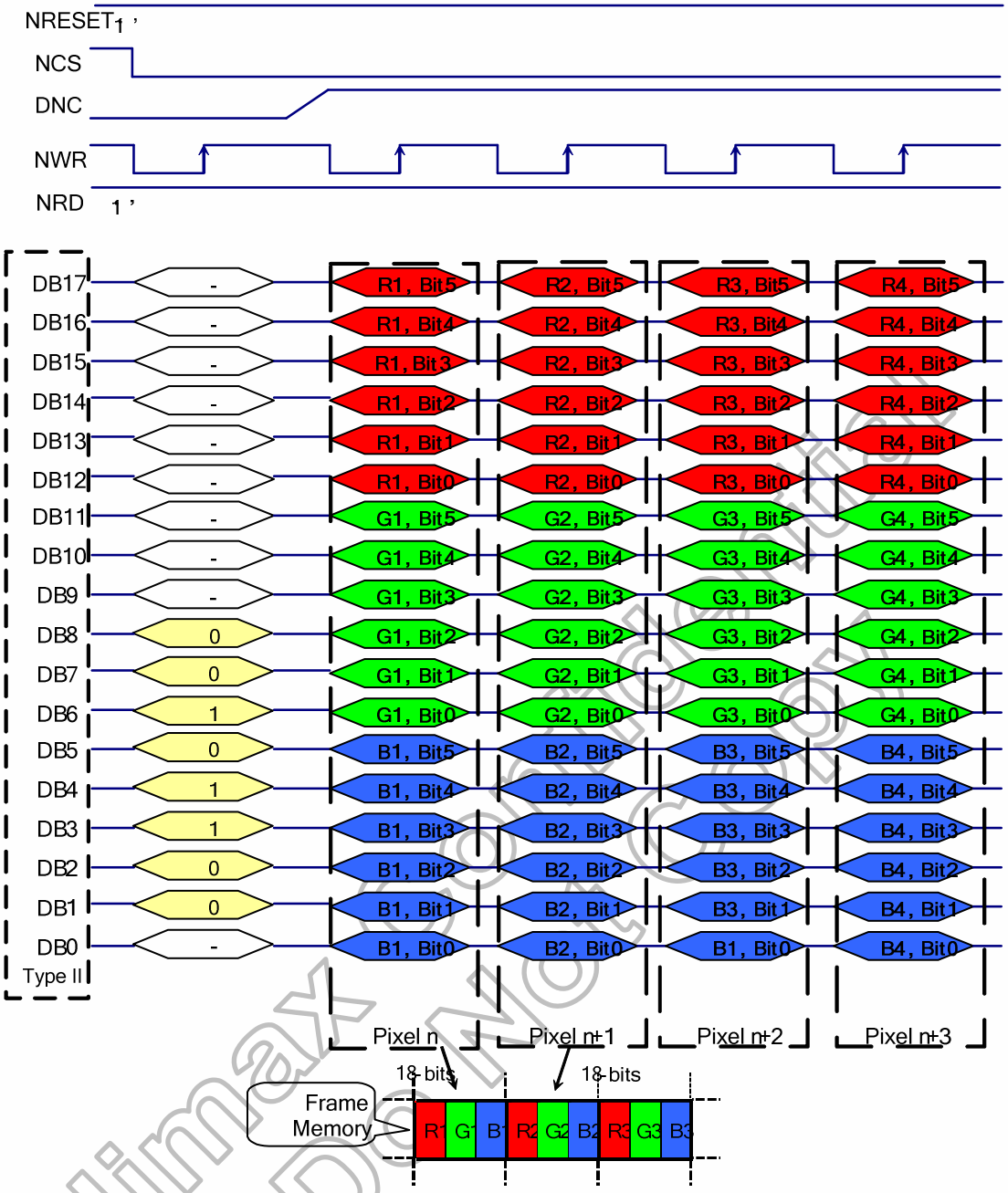

Figure 4-19: Input data bus and GRAM data mapping in 18-bit bus system interface II with 18-bit-data input (“IM3, IM2, IM1, IM”= “1010”)

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MCU Data Color Coding for RAM data *Read*

- Parallel 8-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0000")

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4-10: 8-bit parallel interface type I GRAM read table

- Parallel 16-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0001")

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4-11: 16-bit parallel interface type I GRAM read table

- Parallel 9-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0010")

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4-12: 9-bit parallel interface type I GRAM read table

- Parallel 18-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0011")

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Command	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4-13: 18-bit parallel interface type I GRAM read table

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- Parallel 8-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	**2EH**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 4-14: 8-bit parallel interface type II GRAM read table

- Parallel 16-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	x	**2EH**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 4-15: 16-bit parallel interface type II GRAM read table

- Parallel 9-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 4-16: 9-bit parallel interface type II GRAM read table

- Parallel 18-Bits Bus Interface type II (IM3,IM2,IM1,IM0="1010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	x	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4-17: 18-bit parallel interface type II GRAM read table

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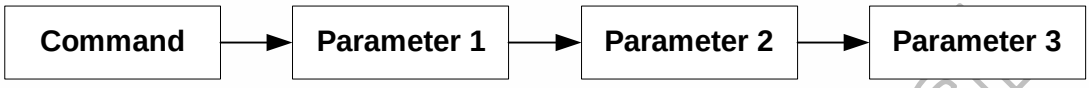
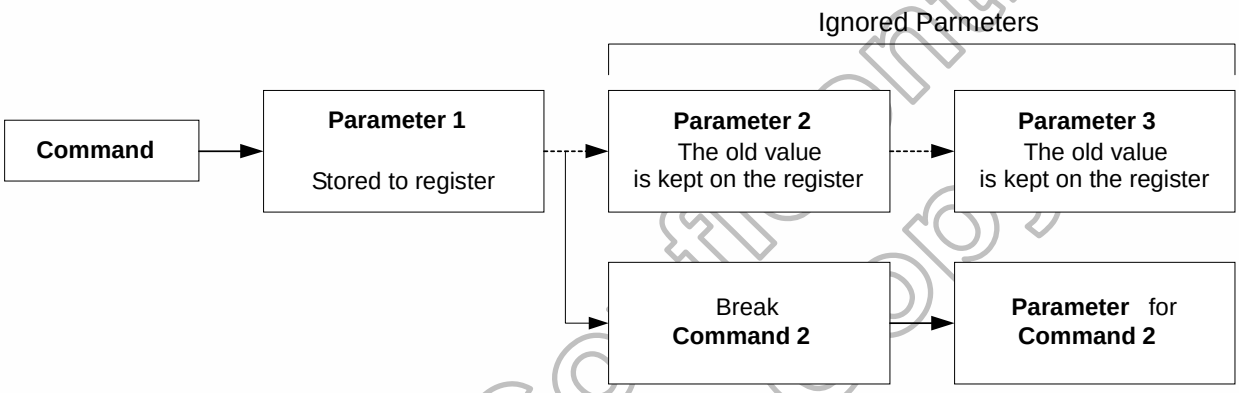
4.1.2 Display module data transfer break

If one or more parameter command is being sent and a break occurs sending before the last parameter and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. If there is a new command as shown in the following example:

Without break



With break



Note: Break can be another command or noise

Figure 4-20: Break during parameter sending

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4.1.3 Serial bus system interface

The HX8347-I supports two kinds of serial bus interface by setting external pins “IM3, IM2, IM1 IM0” pins to “0101” 3-wire serial interface I, and “IM3,IM2, IM1 IM0” pins to “0110” 4-wire serial interface I. The serial bus system interface I mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDA), and the serial transfer clock signal (DNC_SCL).

The external setting “IM3, IM2, IM1 IM0” pins to “1101” 3-wire serial interface II and and “IM3,IM2, IM1 IM0” pins to “1110” 4-wire serial interface II. The serial bus system interface II mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI) output data (SDO), and the serial transfer clock signal (DNC_SCL).

4.1.3.1 3-wire serial interface

The chip select **NCS** (active low) enables and disables the serial interface. **NRESET** (active low) is an external reset signal. **SCL** is serial data clock and **SDA** is serial input data or output signal**.**

Serial data must be input to **SDA** in the sequence D/NC, D7 to D0. The HX8347-I reads the SDA data at the rising edge of **SCL** signal. The first bit of serial data D/NC is data/command flag. When D/NC = "1", D7 to D0 bits are GRAM data or command parameters. When D/NC = "0" D7 to D0 bits are commands.

SCL is not a continuous clock and it can be stopped by the host MCU when **SCL** is low or high after a rising edge of **SCL** for D0 in the writing mode.

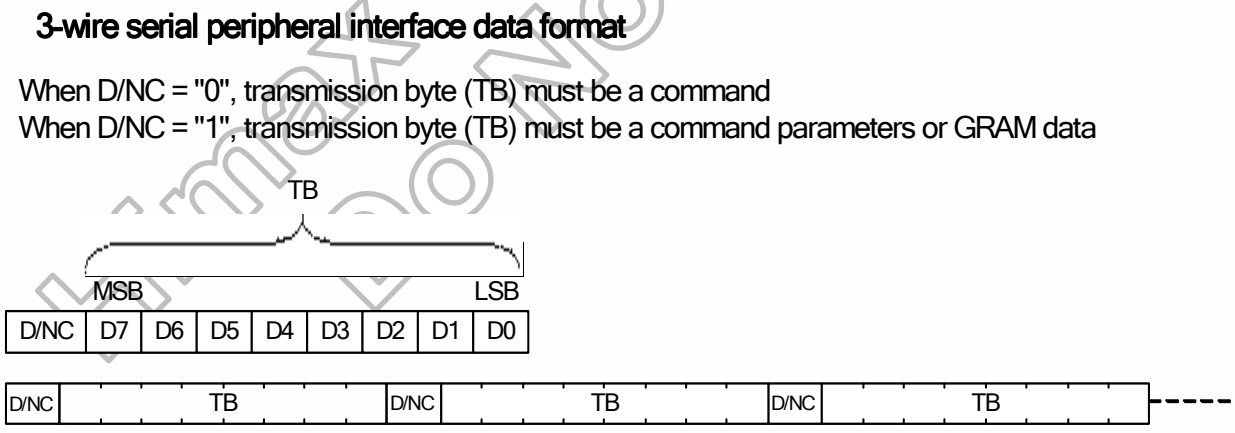

Figure 4-21: Serial peripheral interface data format

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4.1.3.1.1 Write operation in serial peripheral interface

The host MCU drives the **NCS**pin low and starts by setting the D/CX-bit on **SDA**. The bit is read by the display on the first rising edge of **SCL**. On the next falling edge of **SCL** the MSB data bit (D7) is set on **SDA** by the MCU. On the next falling edge of **SCL** the next bit (D6) is set on **SDA**. This continues until all 8 Data bits have been transmitted as shown in Figure 4.21 and Figure 4.22.

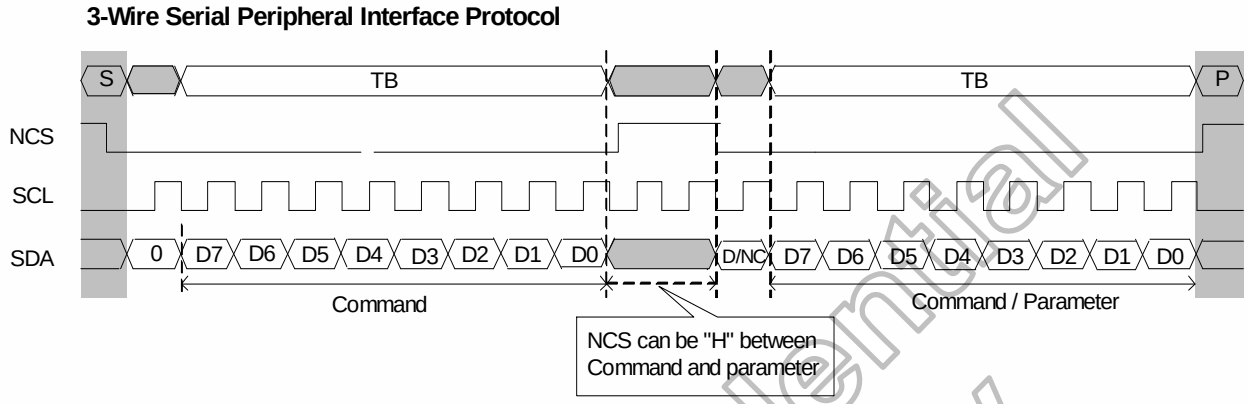

Figure 4-22: Serial peripheral interface protocol in command write operation

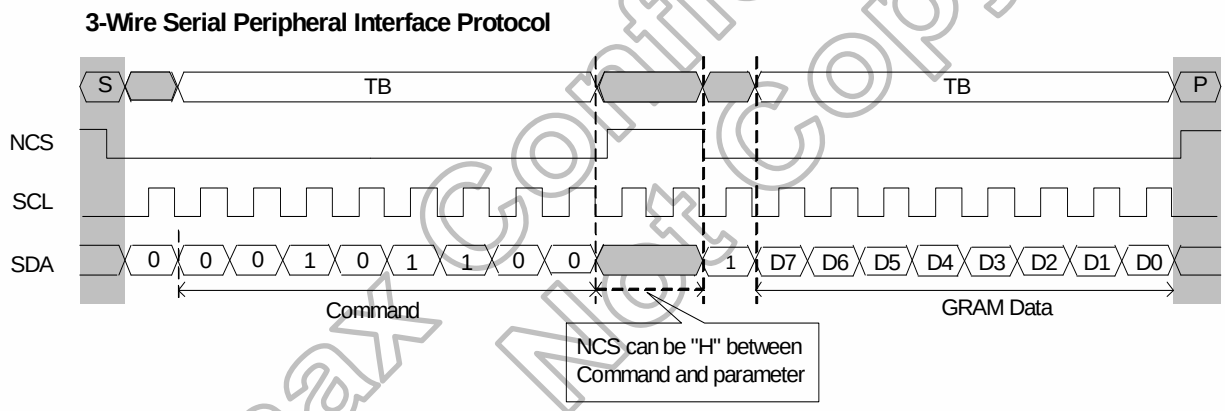

Figure 4-23: Serial peripheral interface protocol in GRAM write operation

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4.1.3.1.2 Read operation in serial peripheral interface

In serial peripheral interface read operation, the host controller first has to send a command and then the following byte is transmitted to host controller in the **SDA**. The read mode has three type command data read (8-/24-/32-bit) and one type GRAM data read.

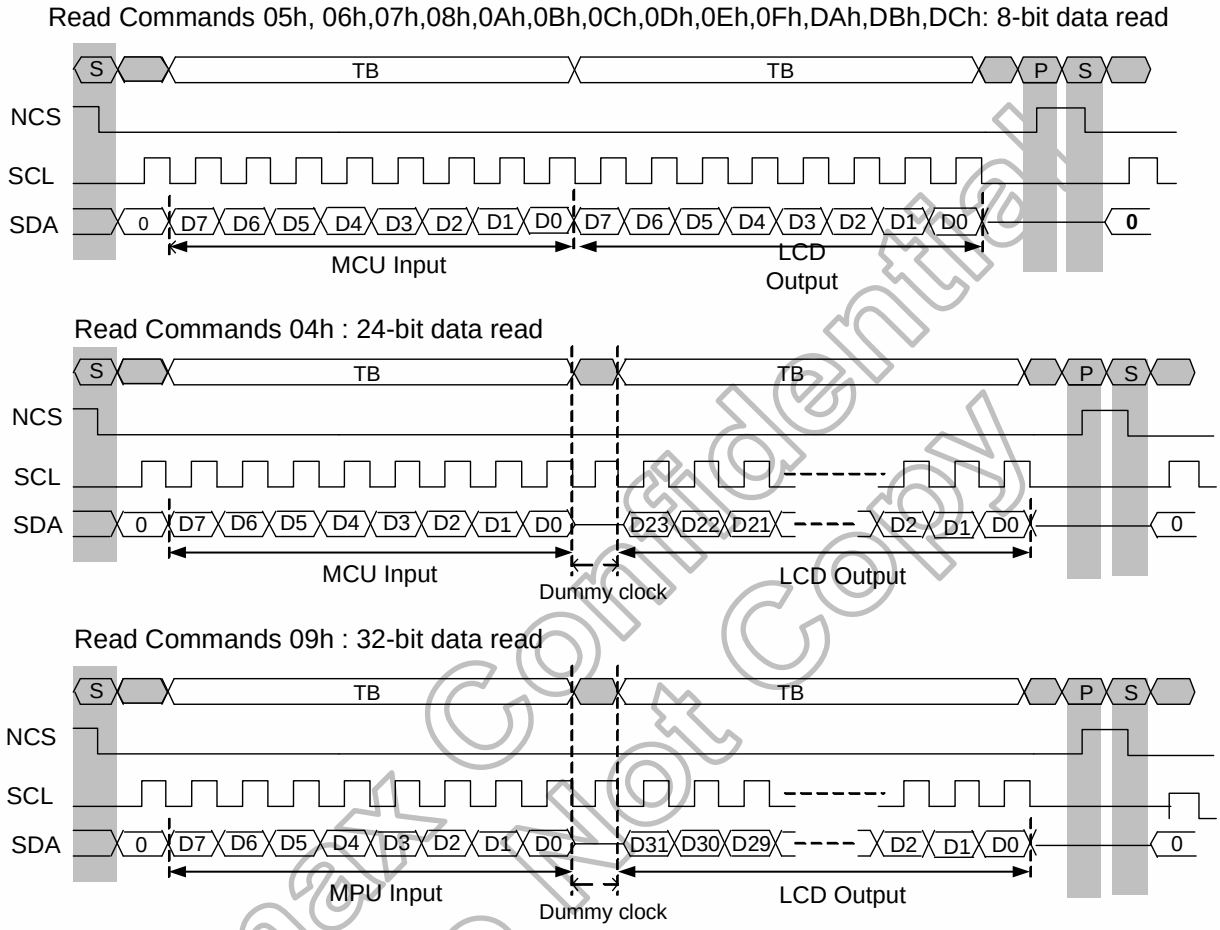

Figure 4-24: Command read operation in serial peripheral interface

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4.1.3.1.3 General data format in serial bus system interface

There are two types data format to write display data at Serial data bus Interface and it is as same as 8-bit bus Interface.

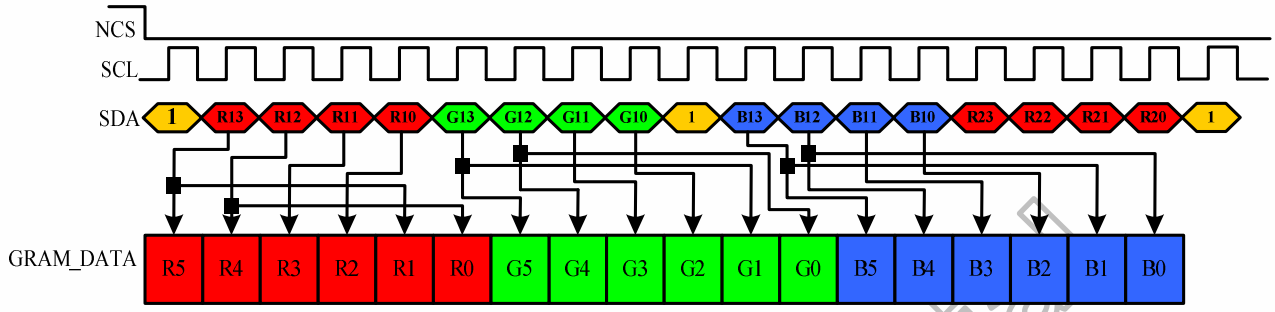

Figure 4-25: Write data for RGB 4-4-4-bits (4k colors) input (D[2:0] = '101' in R3Ah, EPF[1:0] = 2'b00)

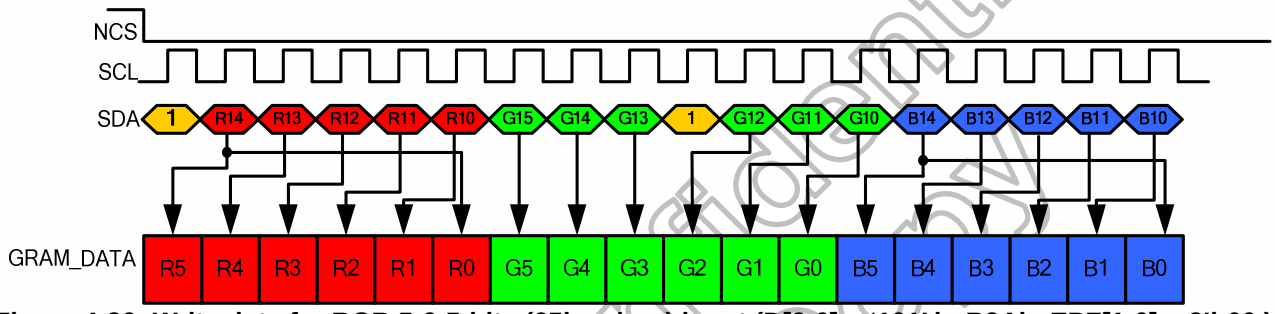

Figure 4-26: Write data for RGB 5-6-5-bits (65k colors) input (D[2:0] = '101' in R3Ah, EPF[1:0] = 2'b00)

Note: If R[4:0] = B[4:0], R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]} when EPF[1:0] = 2'b11

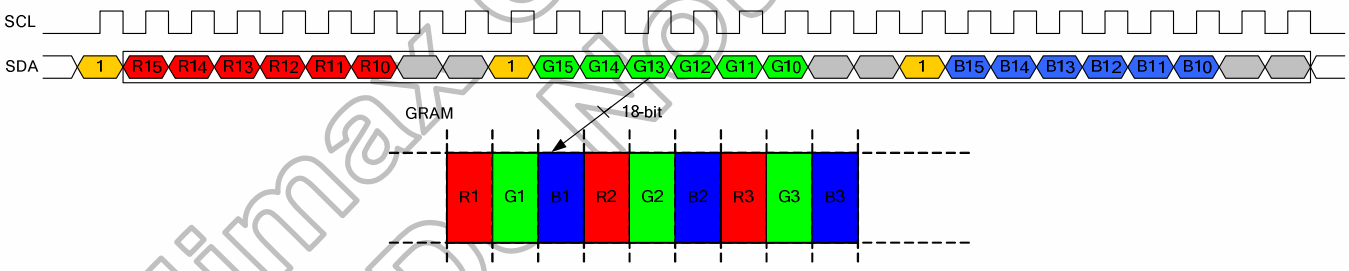

Figure 4-27: Write data for RGB 6-6-6-bits (262k colors) (D[2:0] = '110' in R3Ah)

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4.1.3.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC pin. If DNC is low, the transmission byte is command byte. If DNC is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

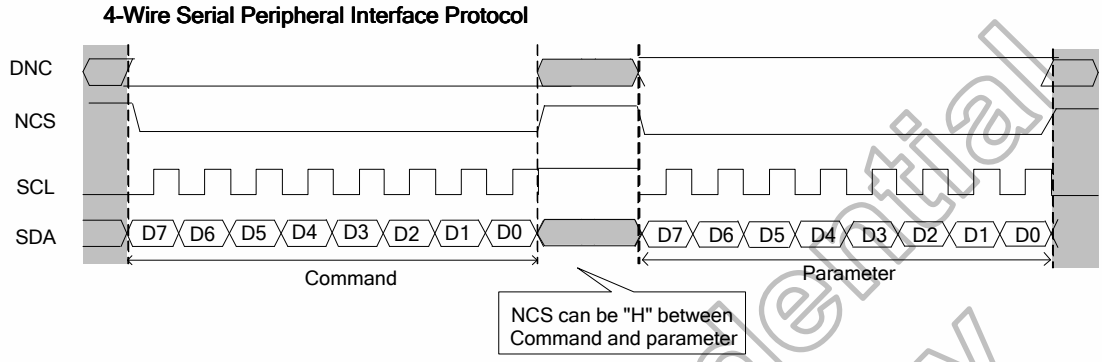

Figure 4-28: Index register write timing in 4-wire serial bus system interface

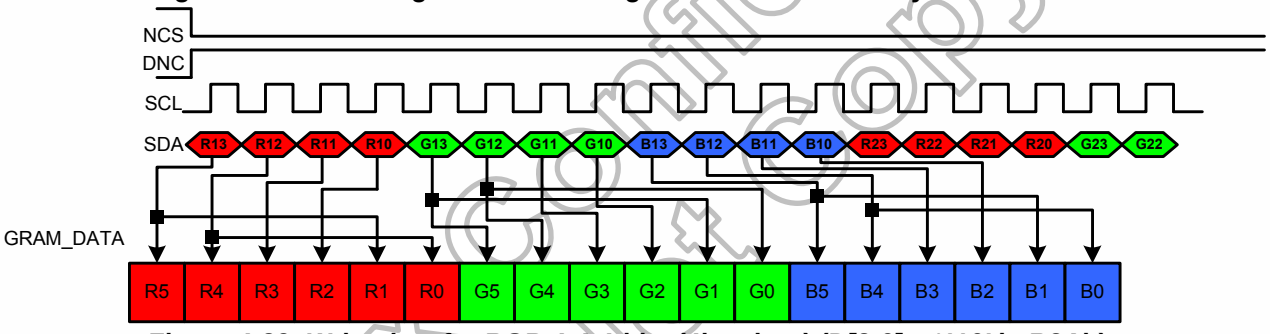

Figure 4-29: Write data for RGB 4-4-4-bits (4k colors) (D[2:0] = '110' in R3Ah)

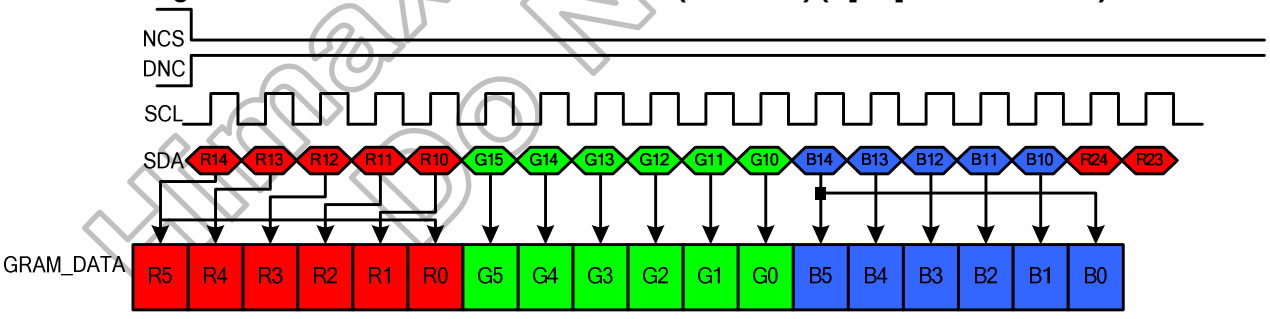

Figure 4-30: Write data for RGB 5-6-5-bits (65k colors) (D[2:0] = '101' in R3Ah, EPF[1:0] = 2'b00)

Note: If R[4:0] = B[4:0], R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]} when EPF[1:0] = 2'b11

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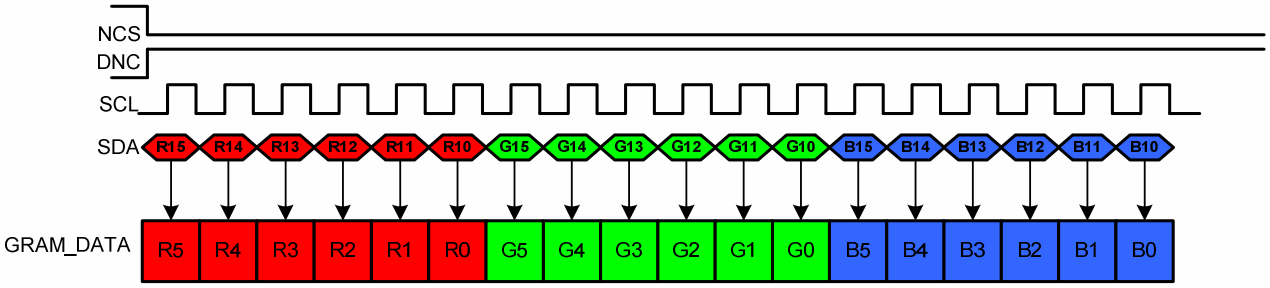

Figure 4-31: Write data for RGB 6-6-6-bits (262k colors) (D[2:0] = '110' in R3Ah)

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4.1.3.3 Display module data transfer recovery for SPI

If there is a break during data transmission when transmit a command before a whole byte has been completed, the HX8347-I will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (NCS) is next activated.

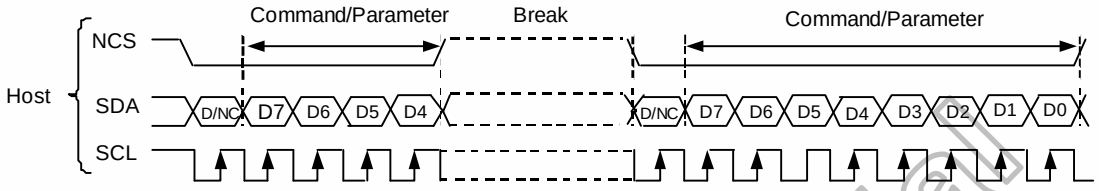
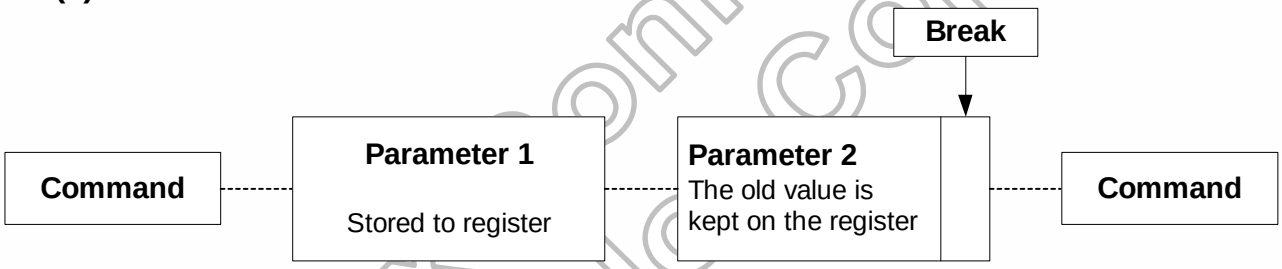


Figure 4-32: Break in SPI mode

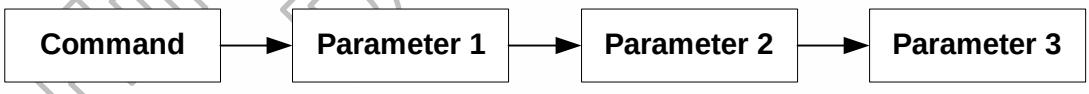
If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

(1) Middle of frame

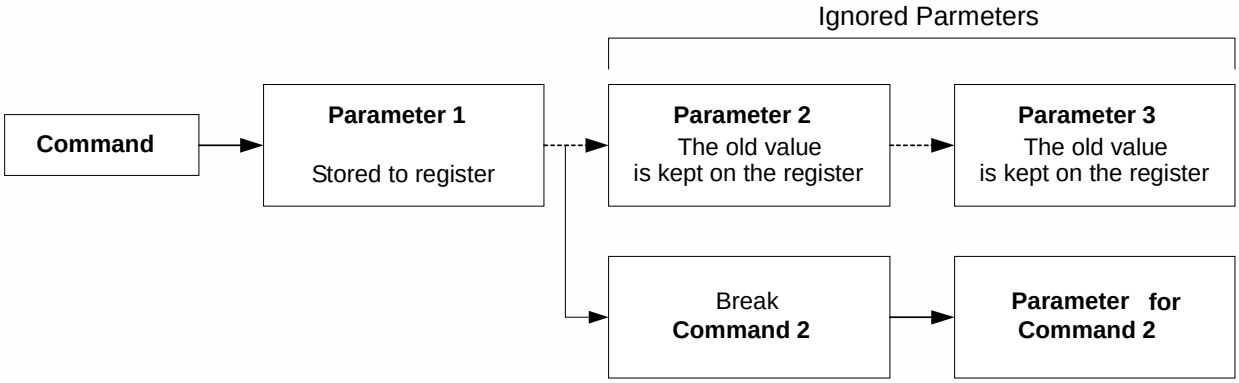


(2) Between frames

Without break



With break



Note: Break can be anoter command or noise

Figure 4-33: Break during parameter in SPI mode

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4.2 RGB interface

The HX8347-I uses **RCM[1:0]='10' or '11' Software setting to select RGB interface.** When after Power on Sequence, the RGB interface is activated. When RCM[1:0]='10' use VSYNC, HSYNC, DE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM[1:0]='11' use VSYNC, HSYNC, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and D[17-0]-lines states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues clock for other functions of the display module e.g. Sleep Mode etc.

In RGB interface mode, the valid display data is inputted in pixel unit via D[17-0] according to the high-level("H") of ENABLE signal, and display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and pixel clock (DOTCLK). Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VSYNC) signal is used to tell when there is received a new frame of the display, and this is negative ('-', '0', low) active. Horizontal synchronization signal (HSYNC) is used to tell when there is received a new line of the frame, and this is negative ('-', '0', low) active. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display, and this is positive ('+', '1', high) active. D[17-0] are used to tell what is the information of the image that is transferred on the display when DE="H".

The pixel clock cycle is described in the following figure.

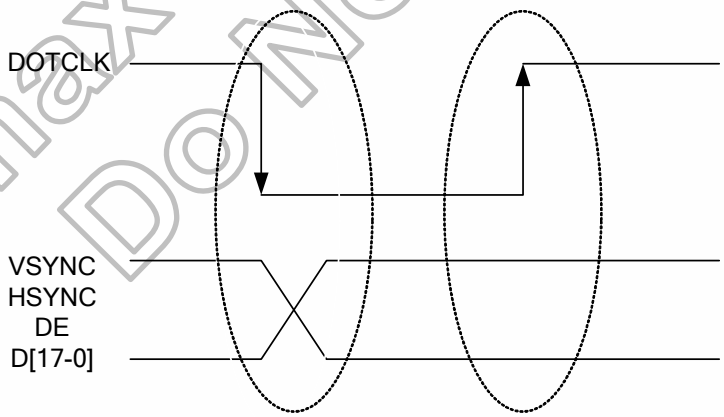

Figure 4-34: DOTCLK cycle

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General timing diagram in RGB interface is shown as below:

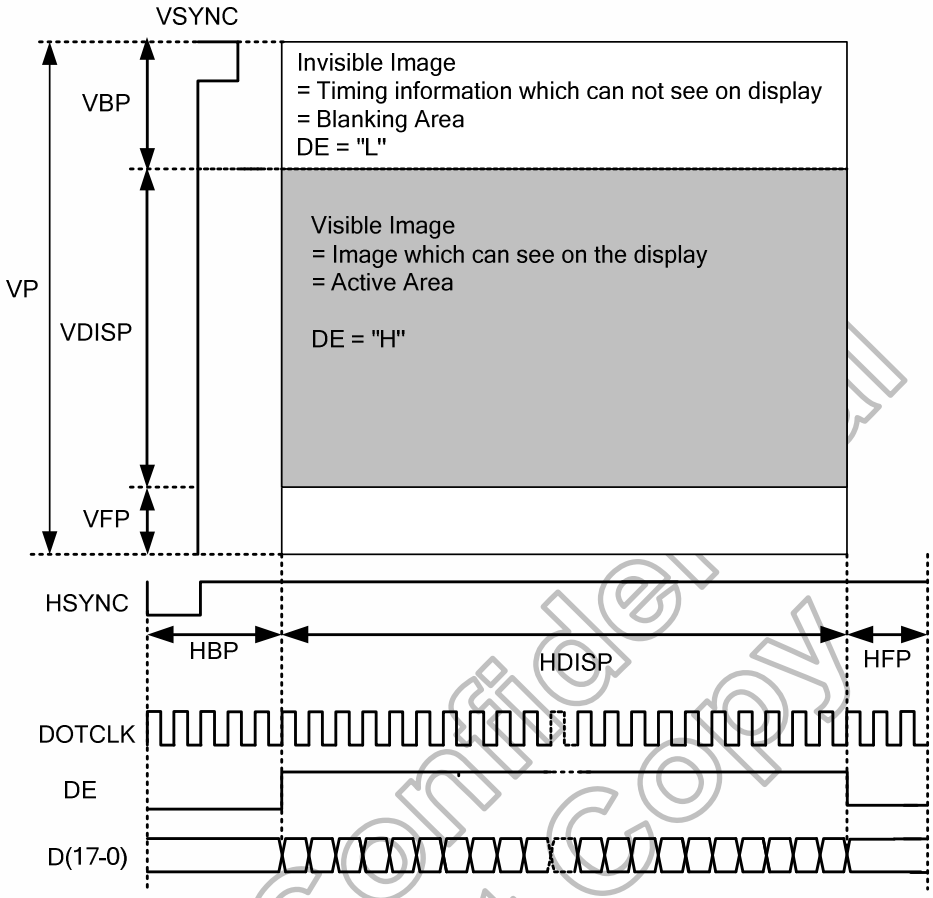

Figure 4-35: RGB interface circuit input timing diagram

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.

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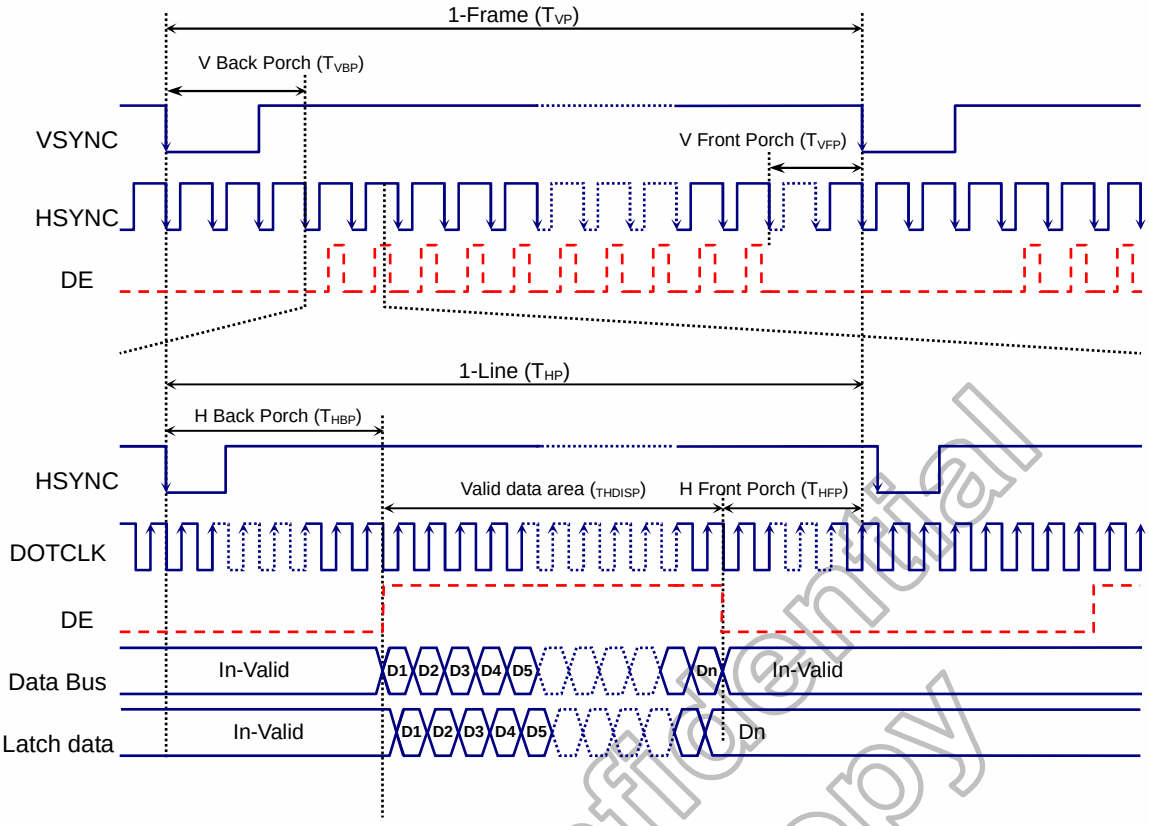

Note: (1) RGB mode 2 doesn't need DE signal
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (B3H) command.

Figure 4-36: RGB mode timing diagram

The input data format per pixel in RGB interface is selected by R3Ah (D4-D6 bits). For selecting the input bus format, please refer to Table 4.18.

Interface Type	Register D(6:4) in R3Ah	Number of data per pixel	Transferring method of one pixel data
16-bit RGB Interface	101	16 bits	16-bit collective
18-bit RGB Interface	110	18 bits	18-bit collective

Table 4-18: Input data format in RGB interface

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RGB interface mode

RGB I/F Mode	DOTCLK	DE	VSYNC	HSYNC	Video Data bus D[17:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = “10”), writing data to display is done by DOTCLK and Video Data Bus (D[17:0]), when DE is high state. The external synchronization signals (DOTCLK, VSYNC and HSYNC) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VSYNC, HSYNC and DE signals to driver.

In RGB Mode 2 (RCM1, RCM0 = “11”), blanking porch setting of VSYNC and HSYNC signals are defined by SETRGB command. DE pin is not used.

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4.2.1 Color order on RGB interface

4.2.1.1 Meaning of pixel information on RGB interface

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on RGB interface, is describing on the following table:

Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colors on this table - Not all gray levels of colors.

Table 4-19: Meaning of pixel information for main colors on RGB interface

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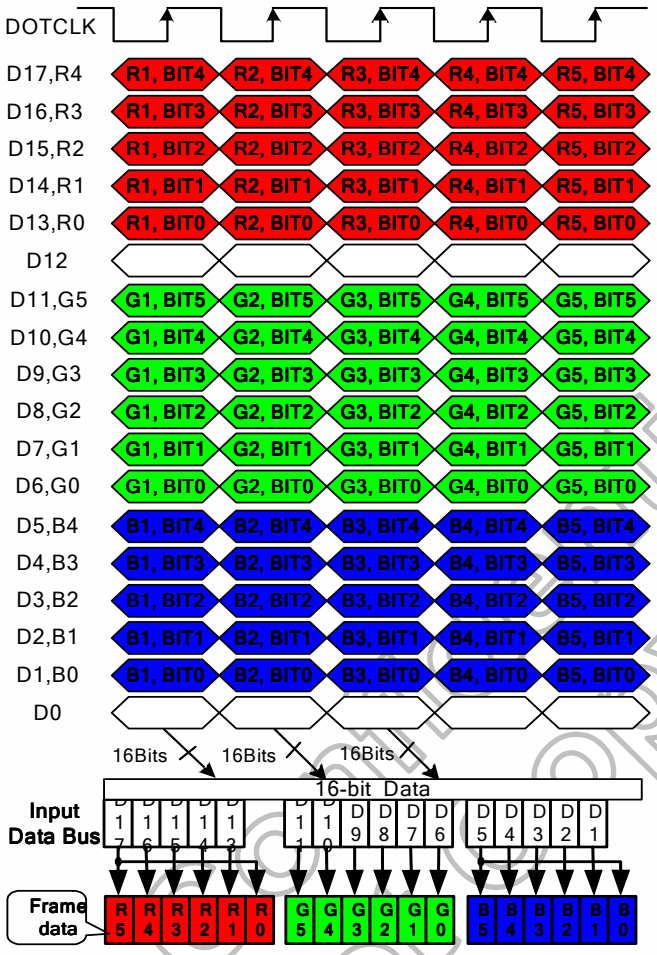
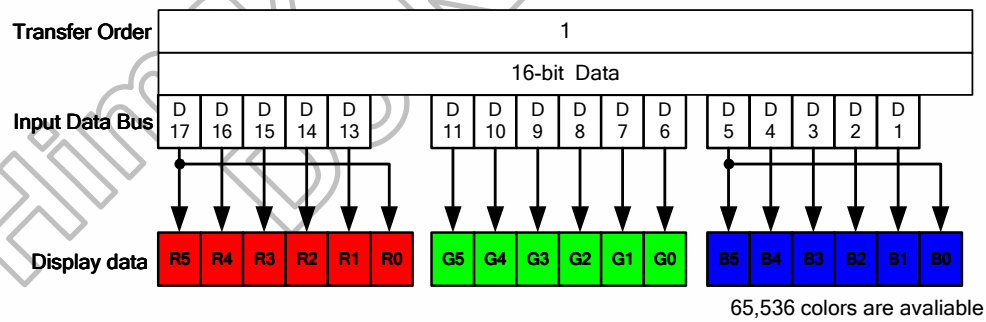
4.2.1.2 16 bit / pixel color order on RGB interface



16-bit to 18-bit data mapping operation in LSI



Note: DB12 and DB0 are fixed to high or low level in 16-bit RGB interface.

Figure 4-37: 16 bit/pixel color order on RGB interface

Note: If R[4:0] = B[4:0], R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]} when EPF[1:0] = 2'b11

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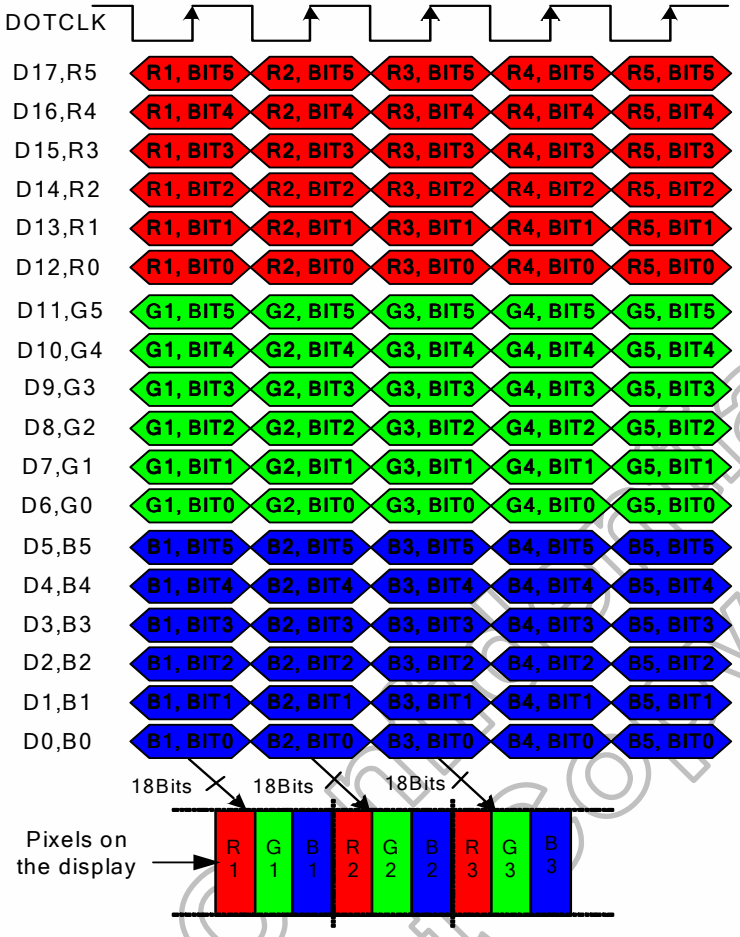
4.2.1.3 18 bit / pixel color order on RGB interface



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4.2.2 One pixel display data memory

The display module includes one pixel (18 bit: 6 bits for R, G and B). This memory includes information of the first active pixel on the frame (pixel: 0, 0=first active line and pixel on the display) from RGB interface.

The purpose of this memory is that there is possible the checks that DB[17-0] – lines are working correctly. The information of this memory is read via serial interface.

There will not be any abnormal visible effect on the display when there is written RGB information to this memory or read RGB information via the serial interface from this memory at the same time.

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5. Functional Description

5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

(00,00)H	(00,01)H	(00,02)H	---------	(00,EC)H	(00,ED)H	(00,EE)H	(00,EF)H
(01,00)H	(01,01)H	(01,02)H	---------	(01,EC)H	(01,ED)H	(01,EE)H	(01,EF)H
(02,00)H	(02,01)H	(02,02)H	---------	(02,EC)H	(02,ED)H	(02,EE)H	(02,EF)H
(03,00)H	(03,01)H	(03,02)H	---------	(03,EC)H	(03,ED)H	(03,EE)H	(03,EF)H
(04,00)H	(04,01)H	(04,02)H	---------	(04,EC)H	(04,ED)H	(04,EE)H	(04,EF)H
(05,00)H	(05,01)H	(05,02)H	---------	(05,EC)H	(05,ED)H	(05,EE)H	(05,EF)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(13A,00)H	(13A,01)H	(13A,02)H	---------	(13A,EC)H	(13A,ED)H	(13A,EE)H	(13A,EF)H
(13B,00)H	(13B,01)H	(13B,02)H	---------	(13B,EC)H	(13B,ED)H	(13B,EE)H	(13B,EF)H
(13C,00)H	(13C,01)H	(13C,02)H	---------	(13C,EC)H	(13C,ED)H	(13C,EE)H	(13C,EF)H
(13D,00)H	(13D,01)H	(13D,02)H	---------	(13D,EC)H	(13DED)H	(13D17E)H	(13D,EF)H
(13E,00)H	(13E,01)H	(13E,02)H	---------	(13E,EC)H	(13E,ED)H	(13E,EE)H	(13E,EF)H
(13F,00)H	(13F,01)H	(13F,02)H	---------	(13F,EC)H	(13F,ED)H	(13F,EE)H	(13F,EF)H

Table 5-1: GRAM address for display panel position

5.2 Address counter (AC) of GRAM

The HX8347-I contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the **CASET** (start: **SC**, end: **EC**) and the PASET (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

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5.2.1 System interface to GRAM write direction

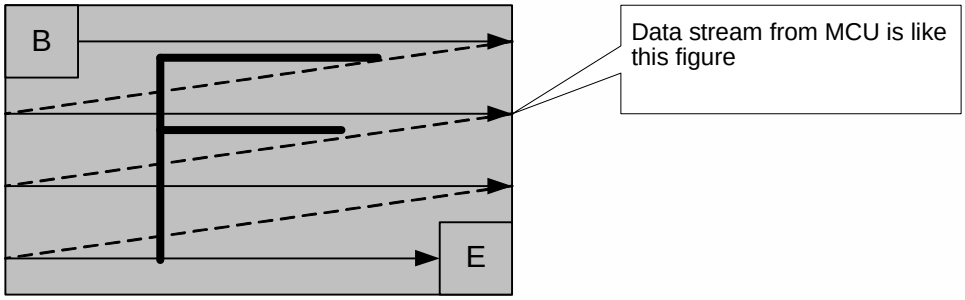

Figure 5-1: Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits setting

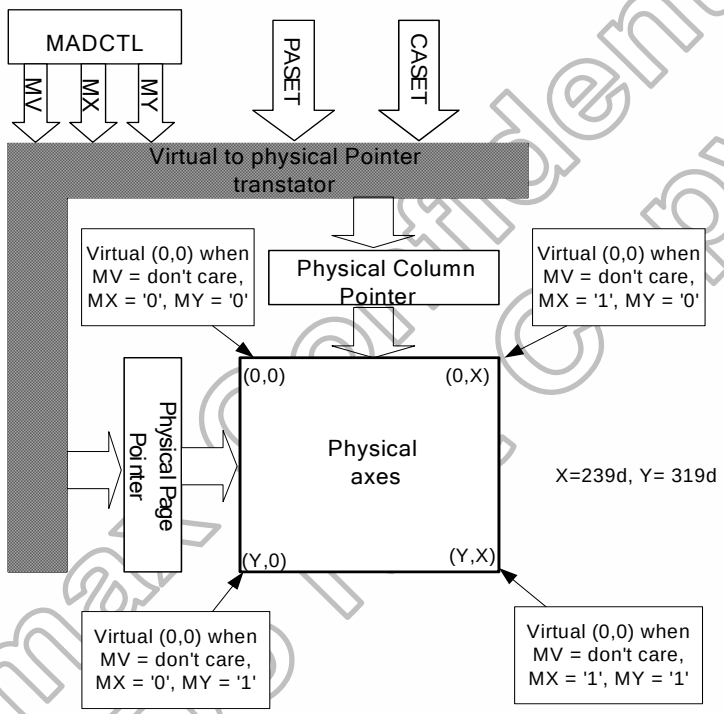

Figure 5-2: Image data writing control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 5-2: CASET and PASET control for physical column/page pointers

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For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

Table 5-3: Rules for updating GRAM order

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The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

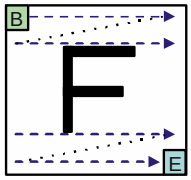
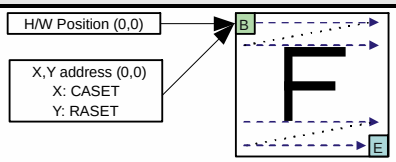
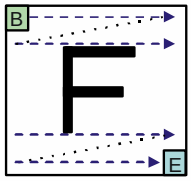
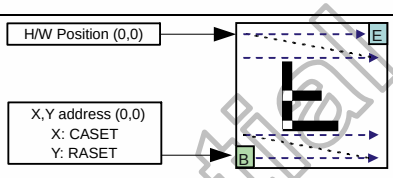
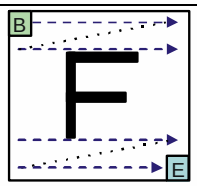
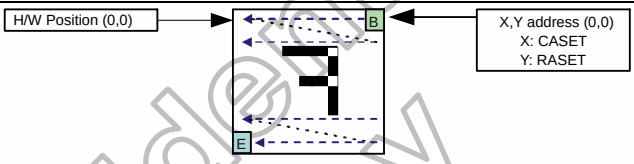
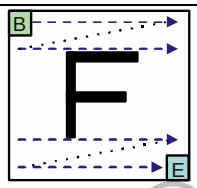
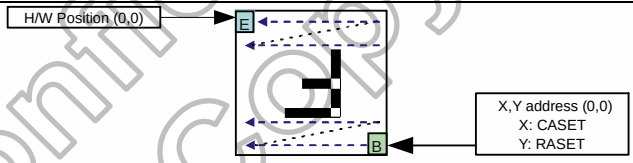
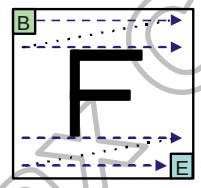
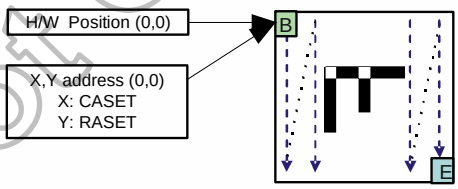
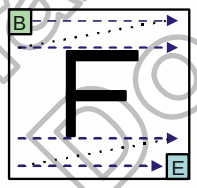
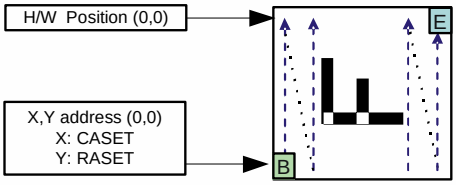
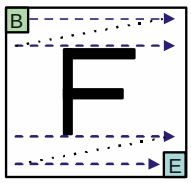
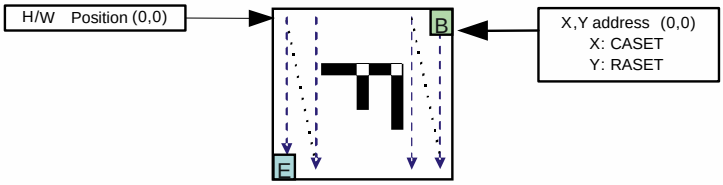
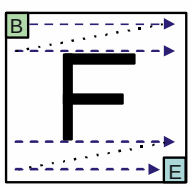
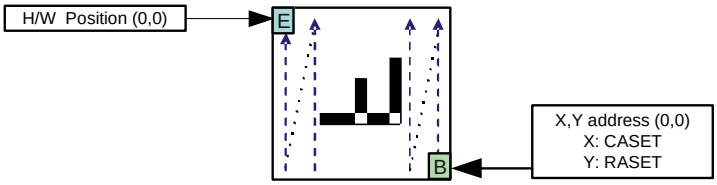
Display Data Direction	MADCTR parameter MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 5-4: Address direction settings

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Example for rotation with MY, MX and MV

This example is using following values: start page=0, end page=40, start column=0 and end column=20=> commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.

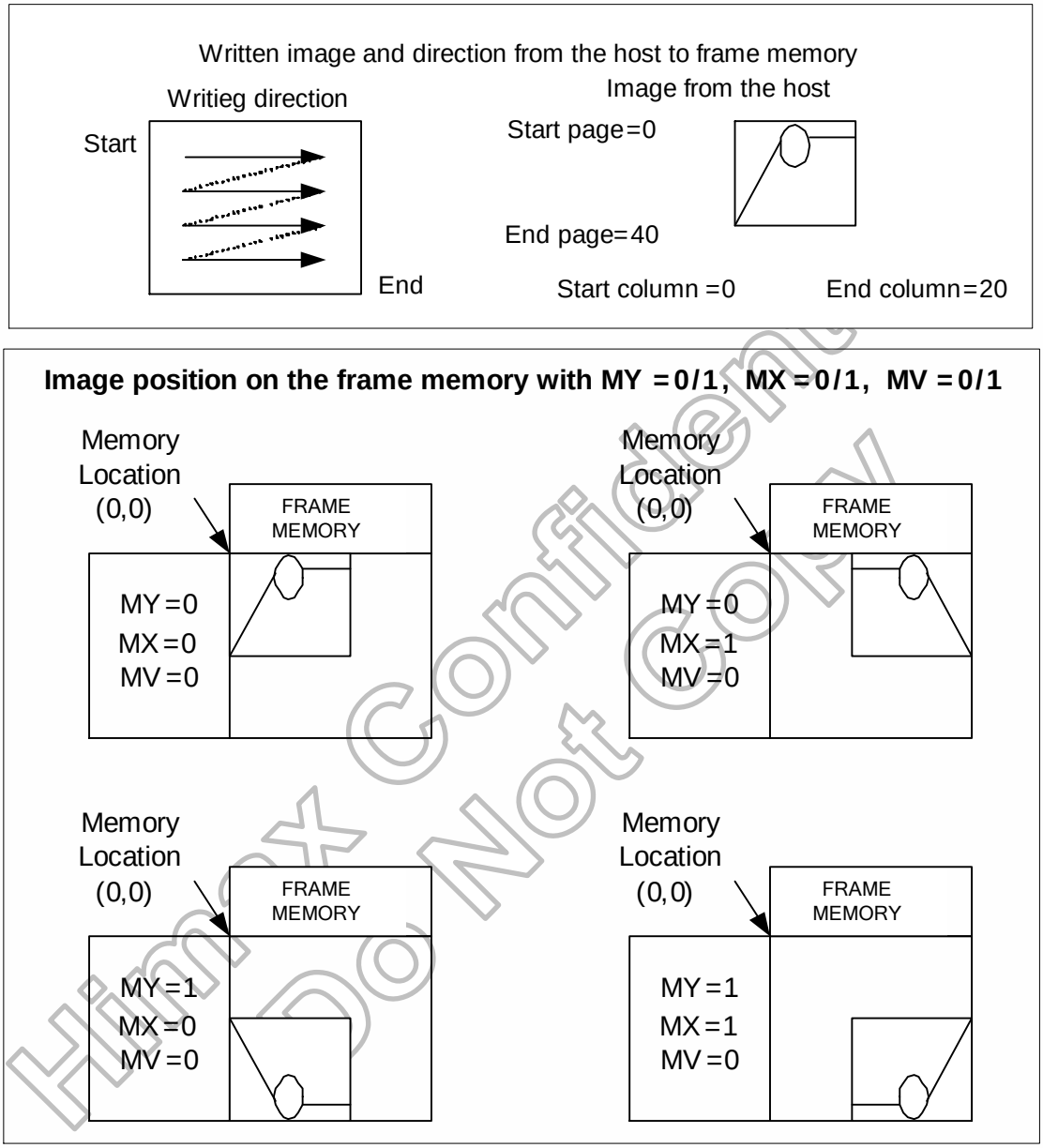

Figure 5-3: Example for rotation with MY, MX and MV – 1

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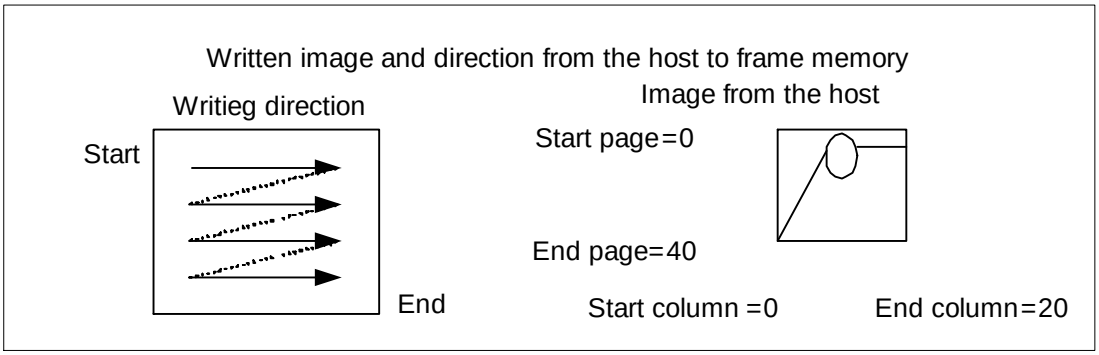

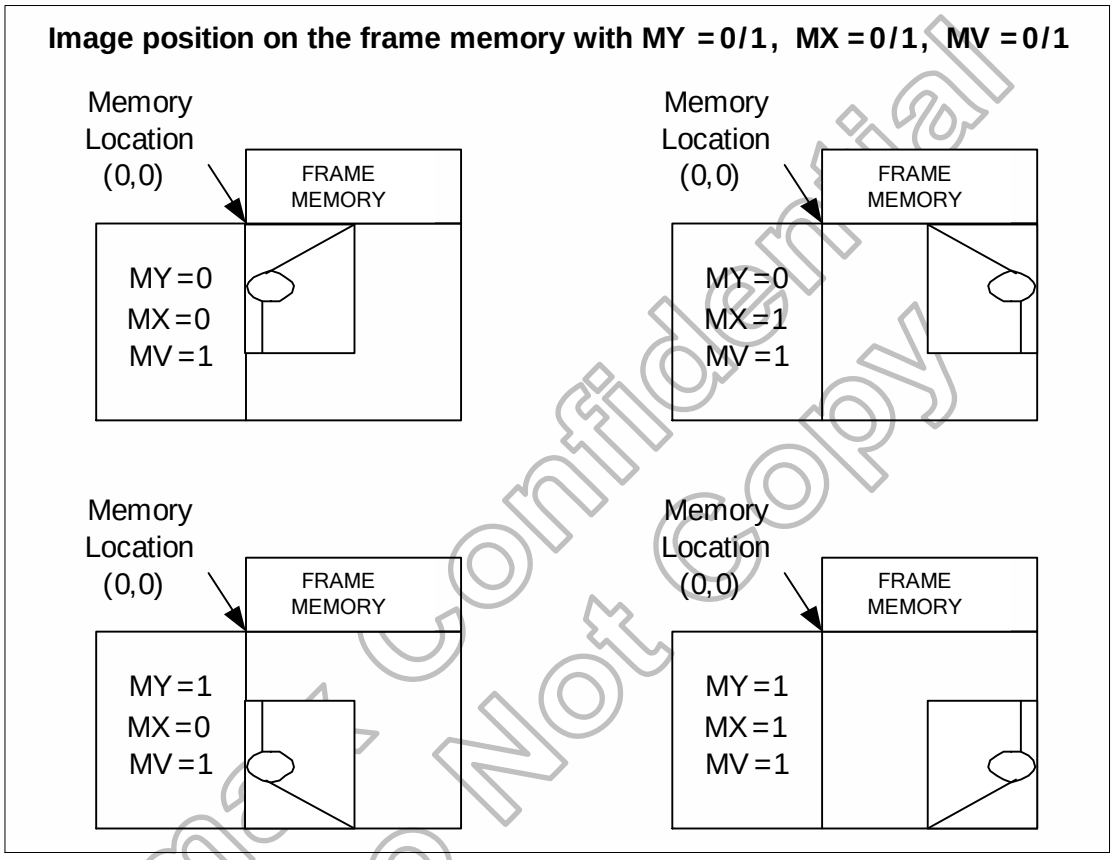

Figure 5-4: Example for rotation with MY, MX and MV - 2

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5.3 GRAM to display address mapping

By setting the **SS_Panel**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS_Panel** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR_Panel**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 5.5, Table 5.6 and Table 5.7 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

BGR_Panel = '0'														
Source	**SS_Panel = '0'**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**-------**	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
Output	**SS_Panel = '1'**	**S718**	**S719**	**S720**	**S715**	**S716**	**S717**	**-------**	**S4**	**S5**	**S6**	**S1**	**S2**	**S3**
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

BGR_Panel = '1'														
Source	**SS_Panel = '0'**	**S3**	**S2**	**S1**	**S6**	**S5**	**S4**	**-------**	**S717**	**S716**	**S715**	**S720**	**S719**	**S718**
Output	**SS_Panel = '1'**	**S720**	**S719**	**S718**	**S717**	**S716**	**S715**	**-------**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
Bit Allocation		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Table 5-5: GRAM X address and display panel position

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S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G1	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G311	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G312	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G313	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G314	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G315	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G316	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G317	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G318	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G319	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G320	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 5-6: GRAM address and display panel position (GS_Panel =’0’)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G320	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G319	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G318	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G317	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G316	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G315	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G314	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G313	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G312	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G9	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G8	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G7	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G6	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G5	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G4	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G3	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G2	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G1	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 5-7: GRAM address and display panel position (GS_Panel =’1’)

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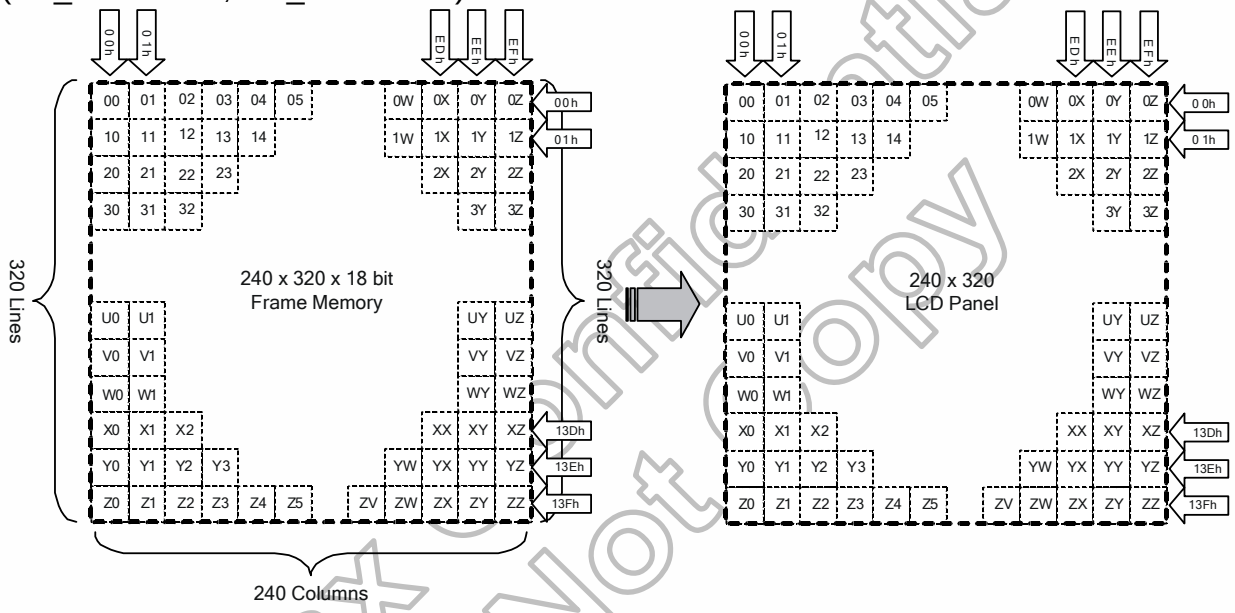
HX8347-I supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

By setting the command **PLTON** (R12h) command, HX8347-I will be into Partial Display Mode. The partial area location in display is depending on two issue: MADCTL's B4(**ML)** and **PLTAR**(R30h)'s **SR** and **ER** bits. By setting the command **NORON** (R13h), HX8347-I will leave Partial Display Mode to Normal Display Mode.

5.3.1 Normal display on or partial mode on, vertical scroll off

In this mode, a content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0) (SS_Panel = '0', GS_Panel = '0').



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Example:

(1) PLTON command (R12h),

(2) R30h's SR=11_{DEC}, ER=130_{DEC}, MADCTL's B4(ML)='0' (GS_Panel = '0').

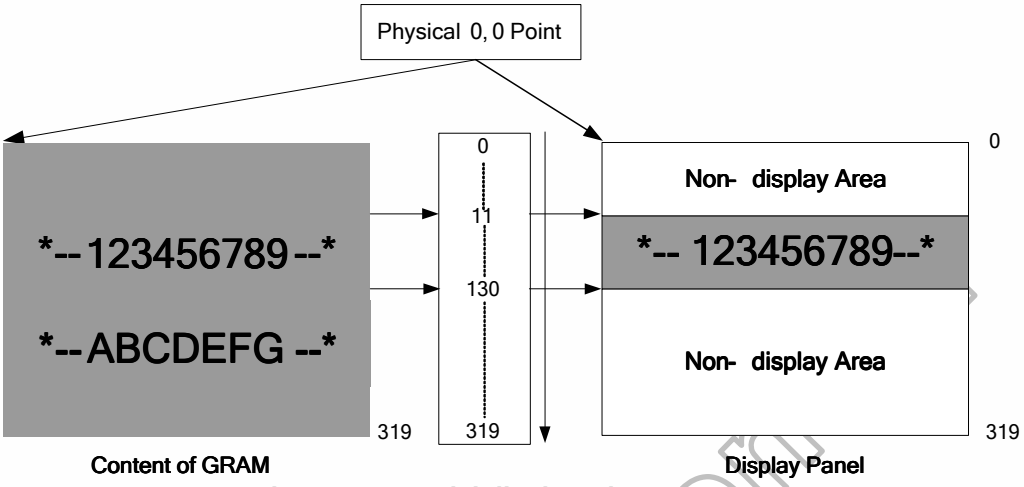

Figure 5-5: Partial display when ML= '0'

Example:

(1) PLTON command (R12h),

(2) R30h's SR= 11_{DEC}, ER=130_{DEC}, MADCTL's B4(ML)='1' (GS_Panel = '0').

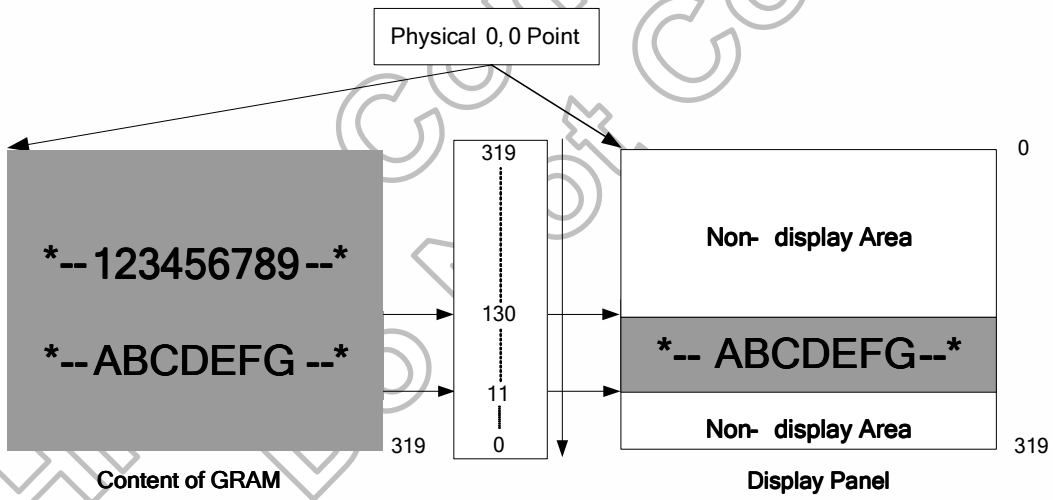

Figure 5-6: Partial display when ML= '1'

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The refresh gate scan cycle in the rest display area of the screen (non-display area) can be specified by **SETDISP's ISC[3:0]** bits. In the refresh gate scan cycle of non-display area in Partial Display Mode, the source and gate control signals output are followed as **SETDISP's PT[1:0] = (0,0).** The scan cycle is set to an odd number from 0~13.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	5 frames	84ms
0	0	1	0	9 frames	150ms
0	0	1	1	13 frames	217ms
:	:	:	:	:	
1	1	0	0	49 frames	813ms
1	1	0	1	53 frames	880ms
1	1	1	0	57 frames	946ms
1	1	1	1	Setting Inhibited	-

Table 5-8: ISC[3:0] bits definition

The rest display area (non-display area) in the screen, will be the white display if the type of LCD is normally white (**SET PANEL's REV_PANEL** = "0") and will be the black display if the type of LCD is normally black (**SET PANEL's REV_PANEL** = "1") in gate scan cycle.

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5.3.2 Vertical scroll display mode

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

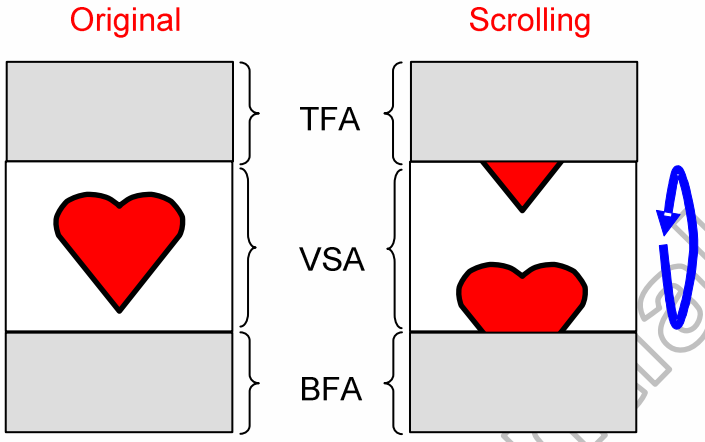

Figure 5-7: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, scrolling is applied as shown below.

Example (1) TFA='2d', VSA='318d', BFA='0d', VSP='3d' when MADCTL B4=0 (SS_Panel = '0', GS_Panel = '0').

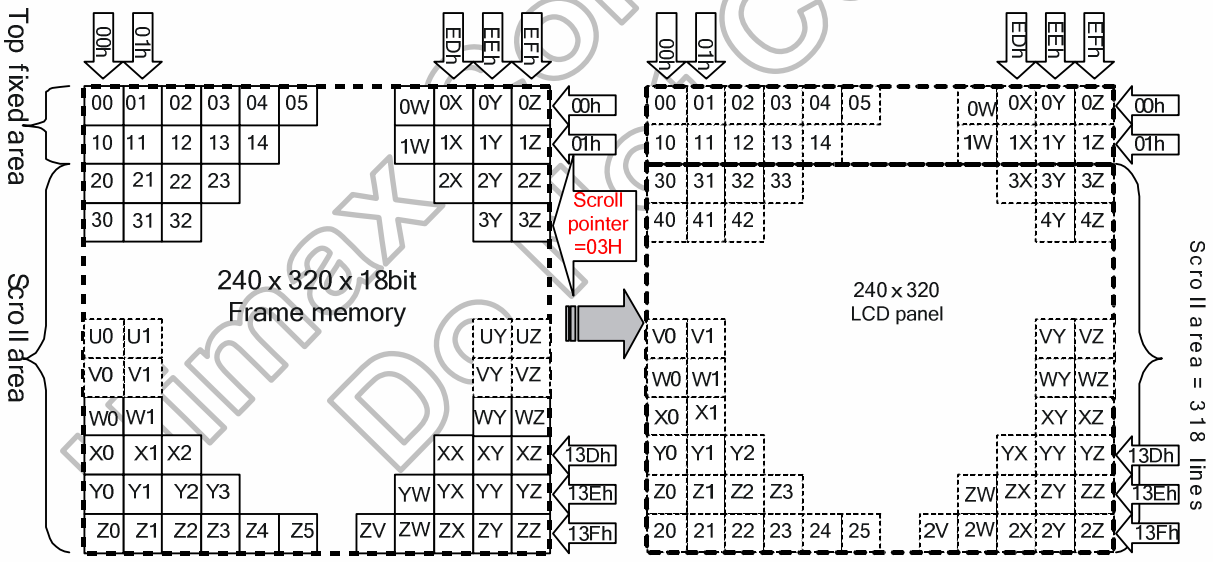

Figure 5-8: Memory map of vertical scrolling example 1

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Example (2) TFA='2d', VSA='316d', BFA='2d', VSP='3d' when MADCTL B4=0 (SS_Panel = '0', GS_Panel = '0').

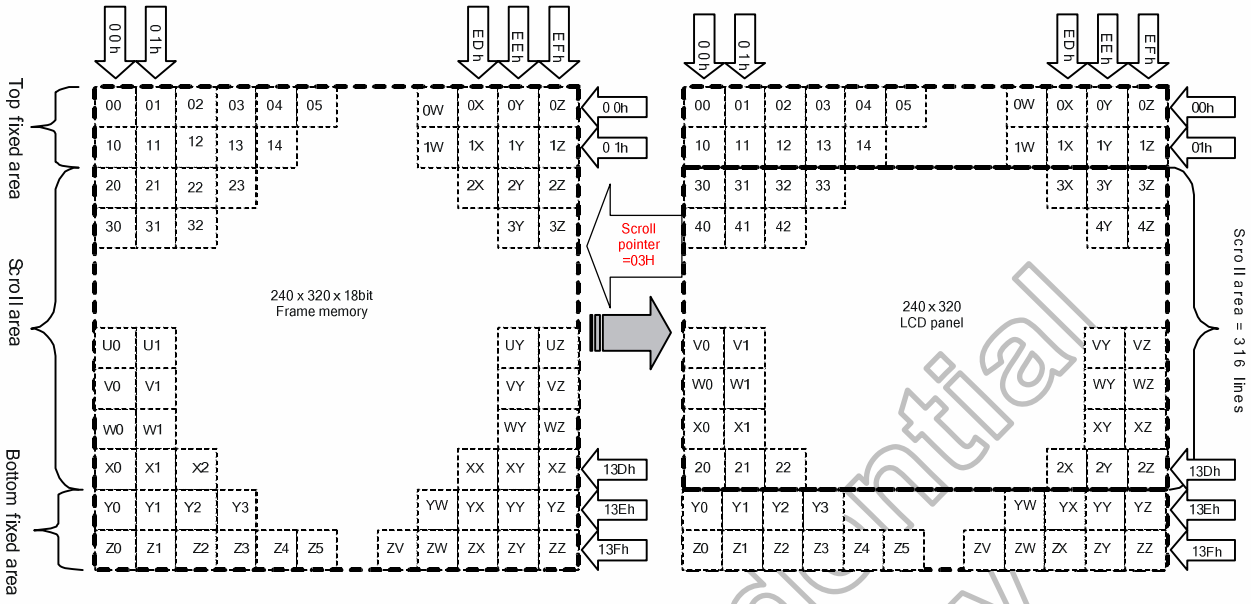

Figure 5-9: Memory map of vertical scrolling example 2

Example (3) TFA='2d', VSA='316d', BFA='2d', VSP='5d' when MADCTL B4=0 (SS_Panel = '0' = 'L', GS_Panel = '0').

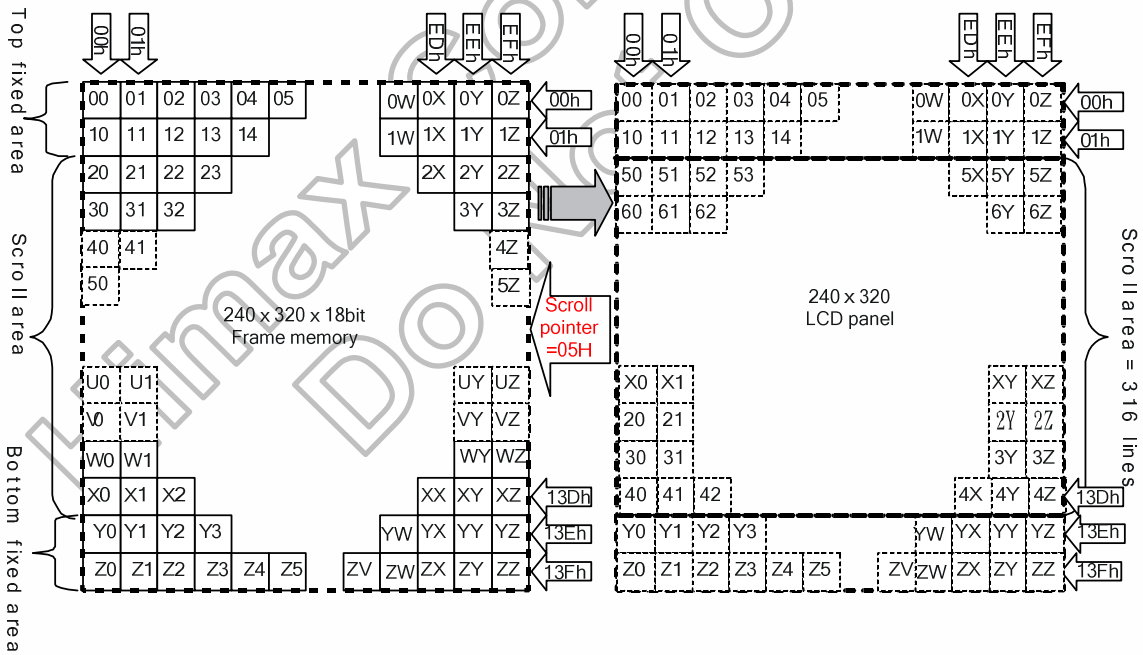

Figure 5-10: Memory map of vertical scrolling example 3

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Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA ≠ '320d'
Note: Do not set TFA + VSA + BFA ≠'320d'. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA= '320d' (Scrolling)
Example (1) When TFA='0d', VSA='320d', BFA='0d' and VSP='40d', MADCTL parameter B4="0"

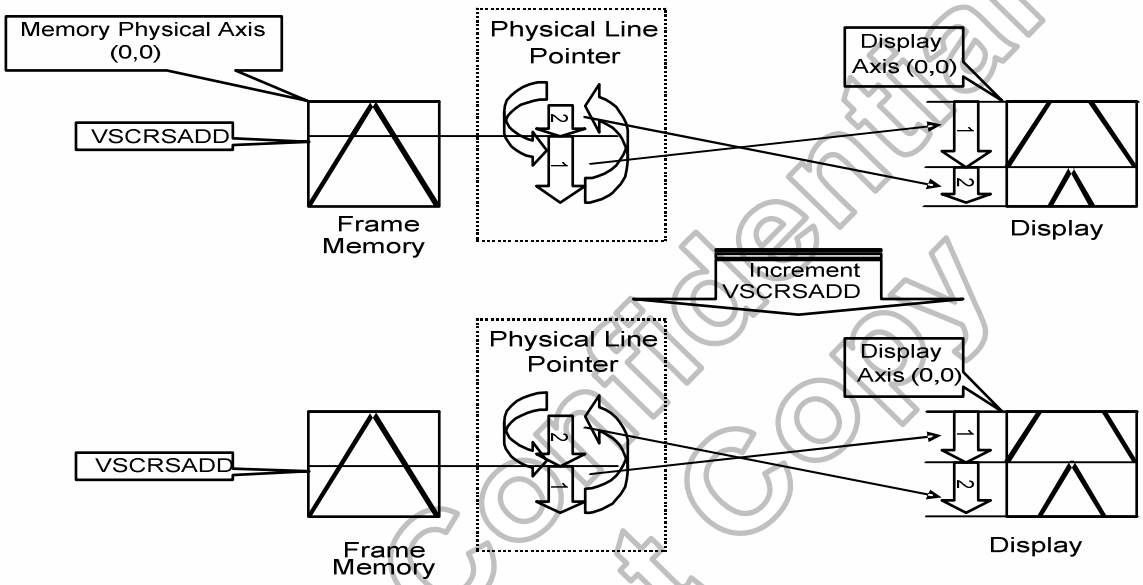

Figure 5-11: Vertical scrolling example when MADCTL_B4='0'

Example (2) TFA='30d', VSA='290d', BFA='0d' and VSP='80d', MADCTRL parameter B4="1"

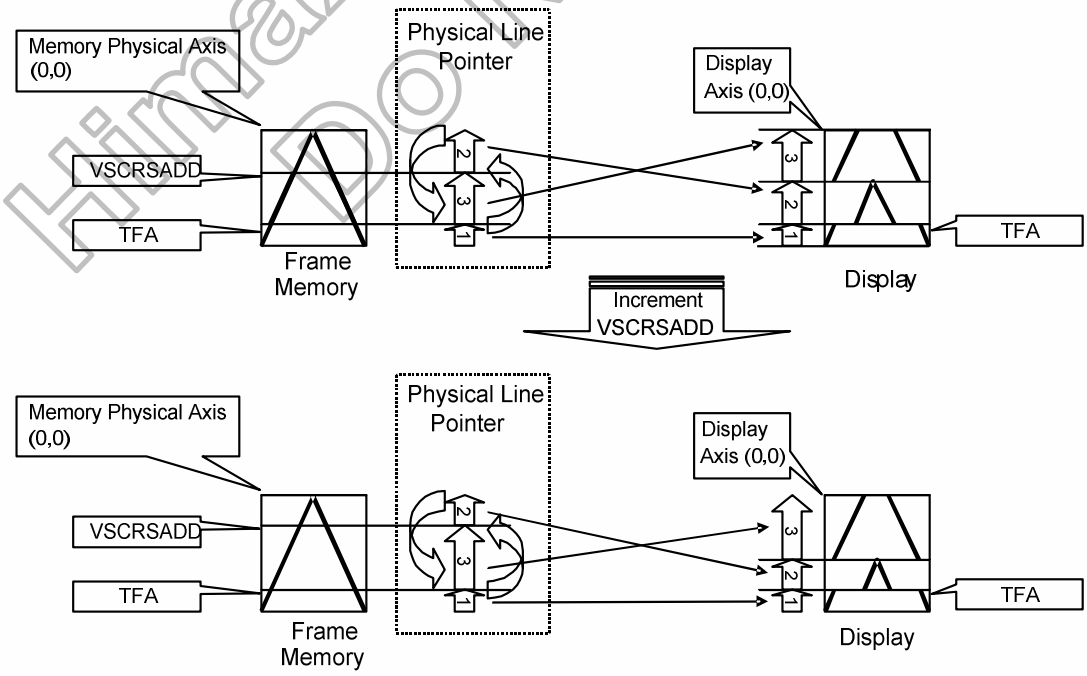

Figure 5-12: Vertical scrolling example when MADCTL_B4='1'

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5.3.3 Updating order on display active area in RGB interface mode (normal mode on + sleep out)

There is defined different kind of updating orders for display in RGB interface mode (**RCM[1:0] = '10' or '11'**). These updating are controlled by MADCTL's B7(MY) and B6(MX) bits.

Data streaming direction from the host to the display is described in the following figure.

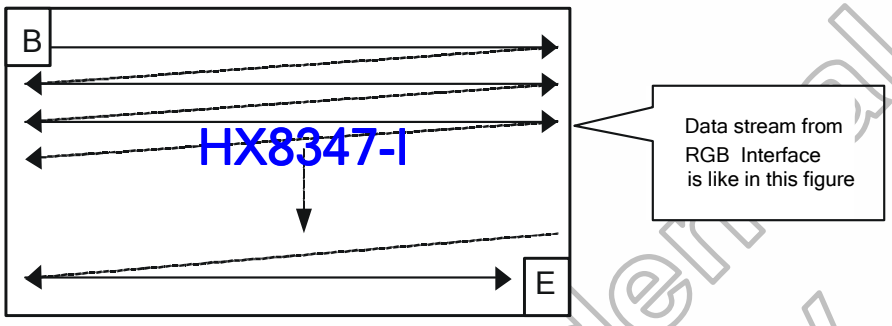

Figure 5-13: Data streaming order in RGB I/F

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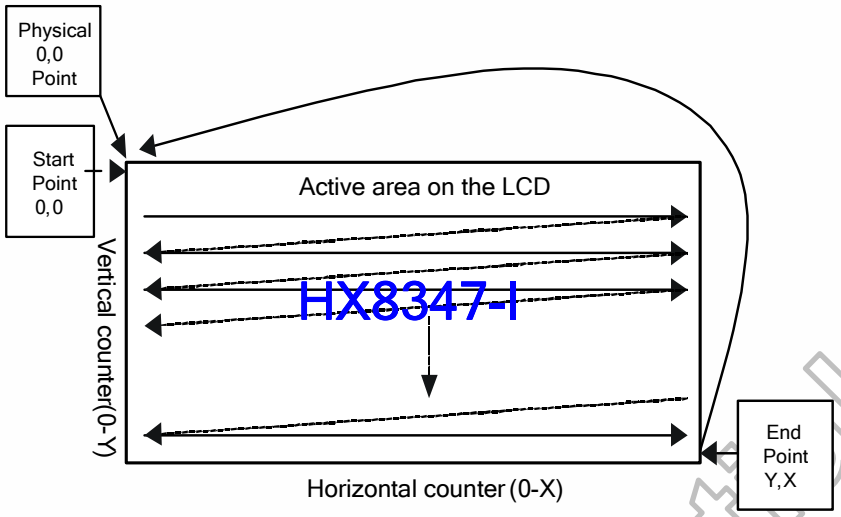

Figure 5-14: Updating order when MY = '0' and MX = '0'

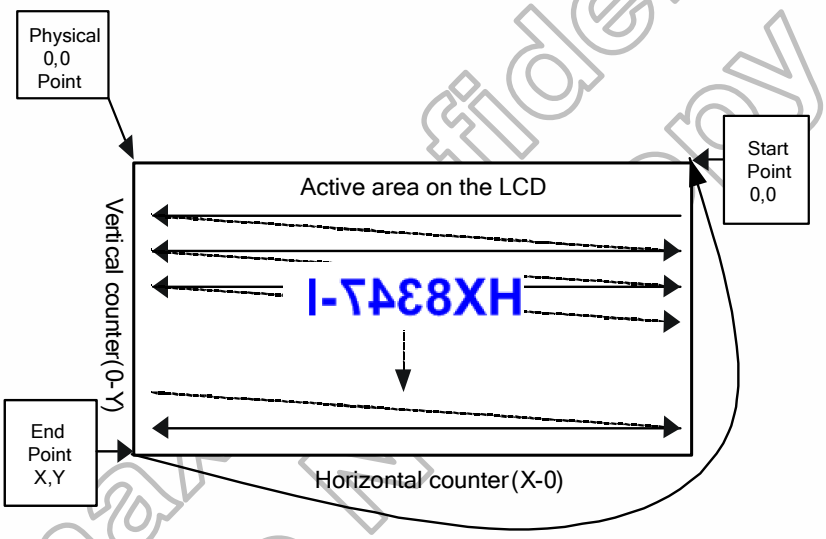

Figure 5-15: Updating order when MY = '0' and MX = '1'

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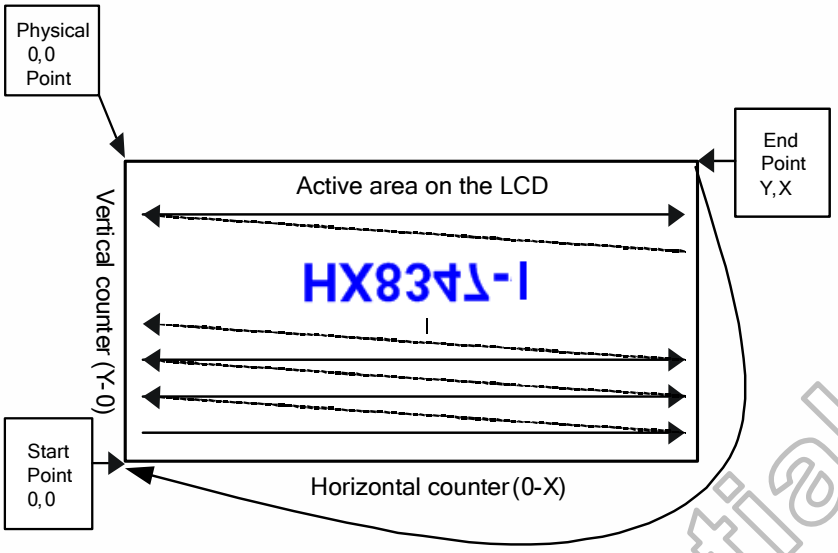

Figure 5-16: Updating order when MY = '1' and MX = '0'

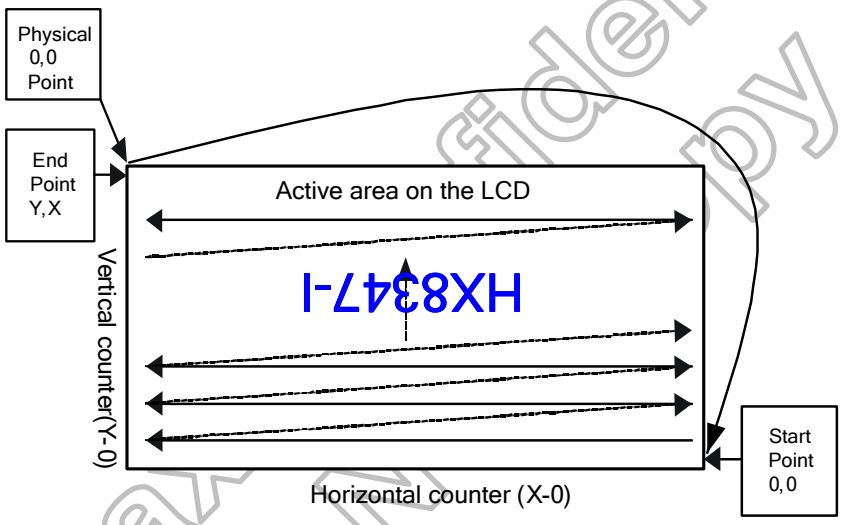

Figure 5-17: Updating order when MY = '1' and MX = '1'

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

Table 5-9: Rules for updating order on display active area in RGB interface display mode

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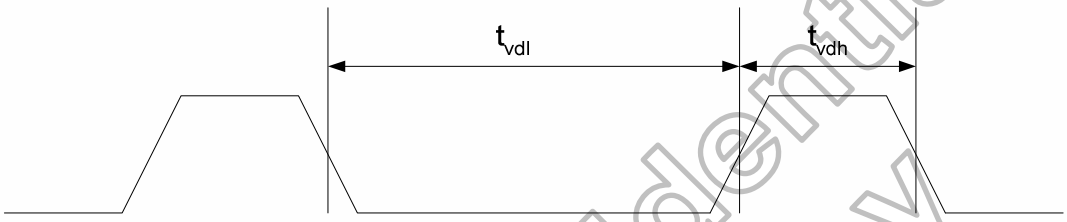
5.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing effect function is not support when at RGB interface (RCM[1:0]="1x").

5.4.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Figure 5-18: TE mode 1 output

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.
Ex:
1. TSEL[15:0]=0, then TE signal will output after last Line finished.
2. TSEL[15:0]=2, then TE signal will output at second Line start.

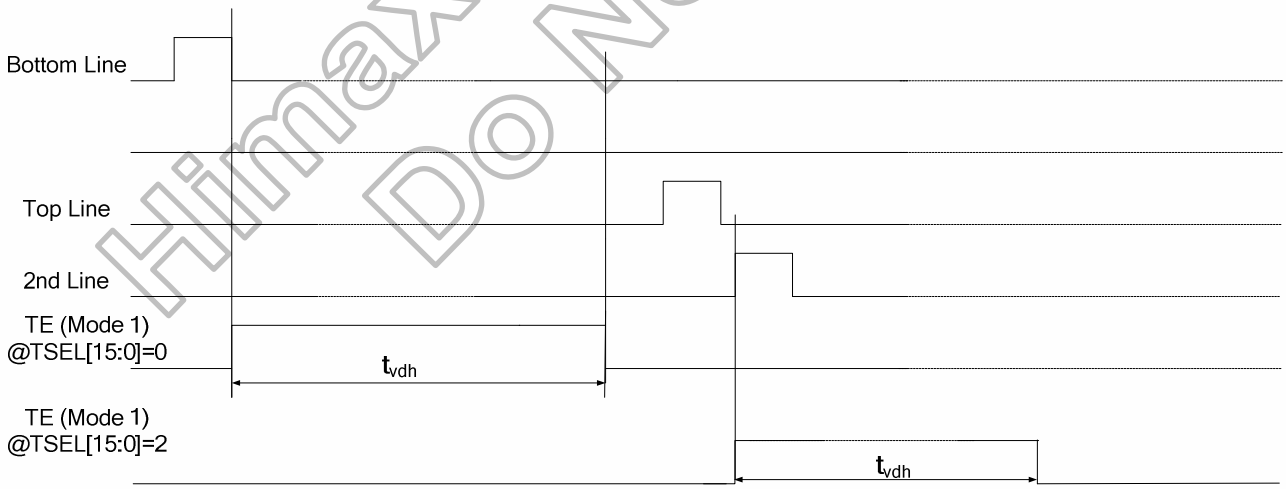


Figure 5-19: TE delay output

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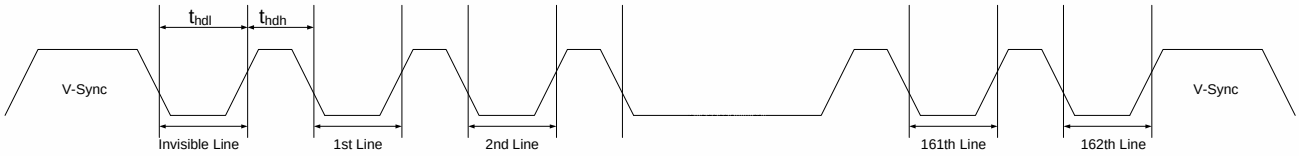
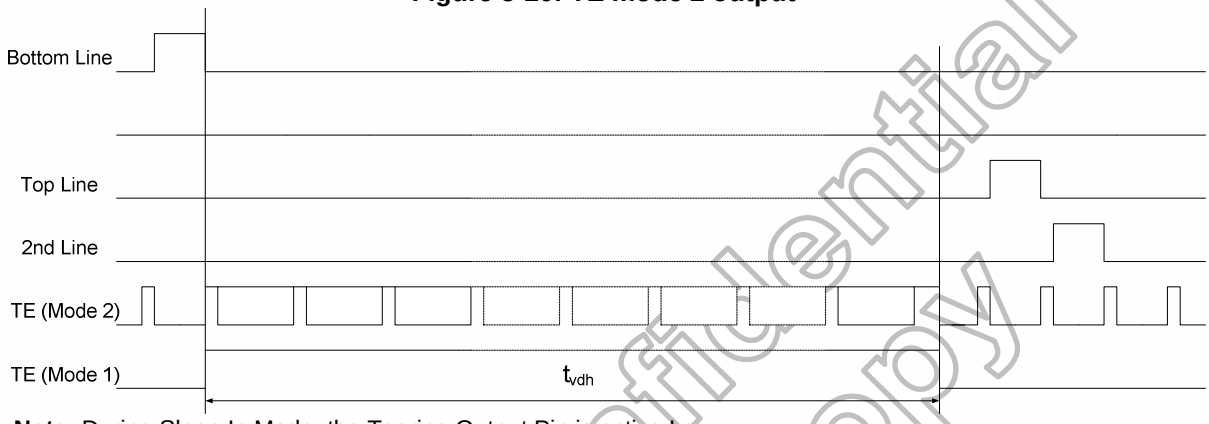
Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 5-20: TE mode 2 output



Note: During Sleep In Mode, the Tearing Output Pin is active Low

Figure 5-21: TE output waveform

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5.4.2 Tearing effect line timing

The Tearing Effect signal is described below.

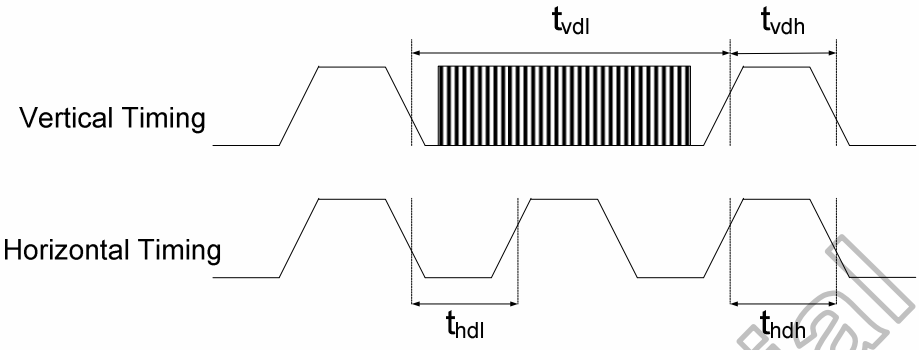

Figure 5-22: Waveform of tearing effect signal

Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Unit	Description
		Min.	Typ.	Max.		
tvdl	Vertical Timing Low Duration	13		-	ms	-
tvdh	Vertical Timing High Duration	1000		-	µs	-
thdl	Horizontal Timing Low Duration	40		-	µs	-
thdh	Horizontal Timing High Duration	0.5		500	µs	-

Table 5-10: AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

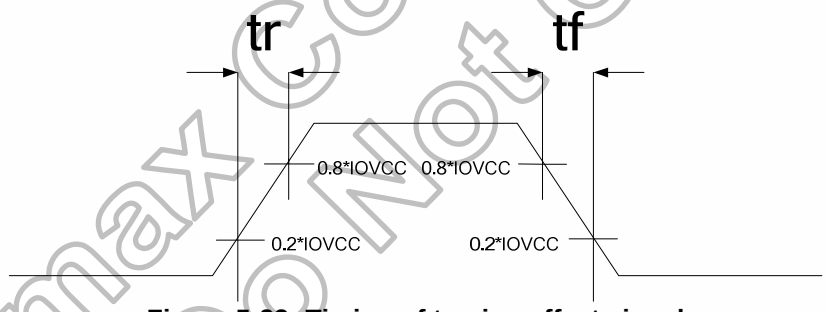

Figure 5-23: Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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5.4.3 Example 1: MPU write is faster than panel read

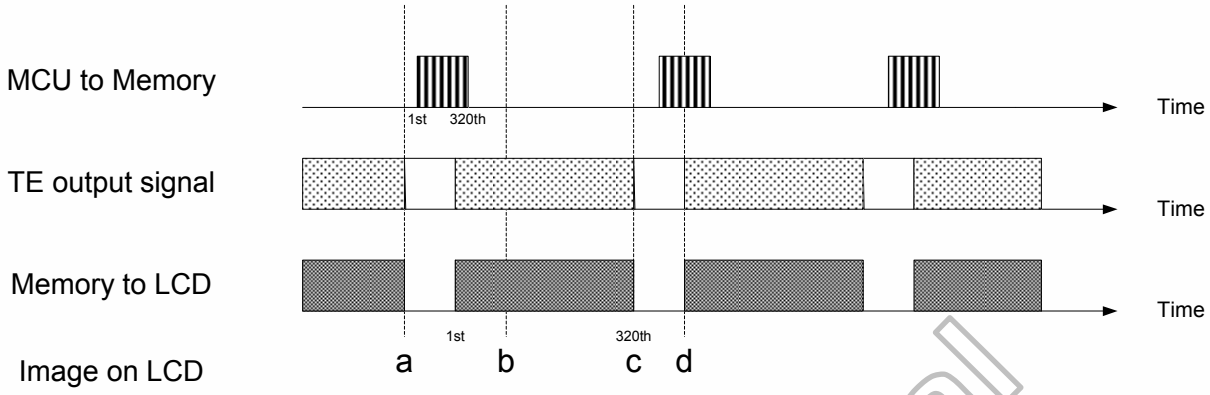

Figure 5-24: Timing of MPU write is faster than panel read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

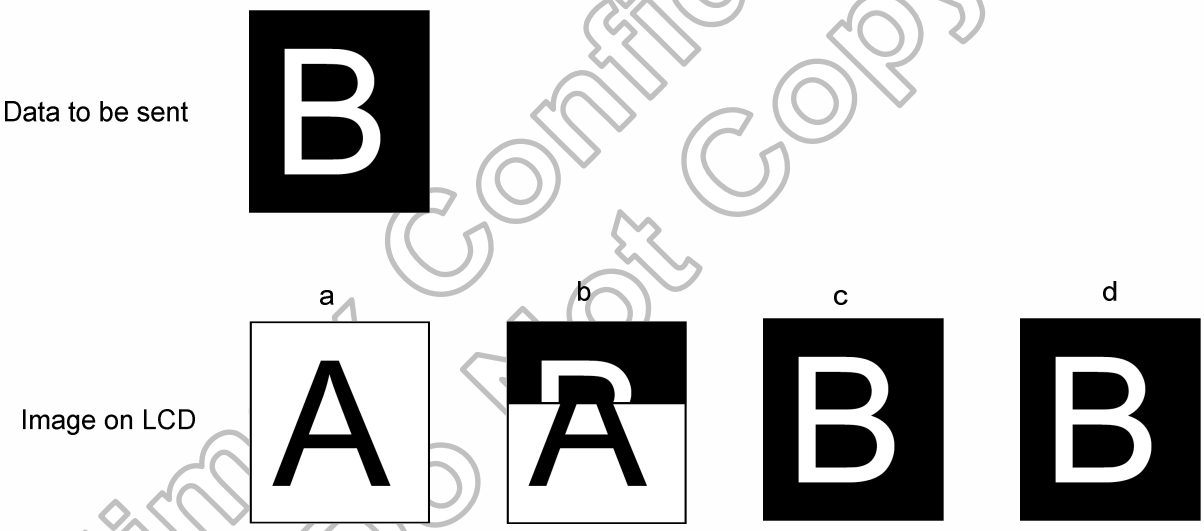

Figure 5-25: Display of MPU write is faster than panel read

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5.4.4 Example 2: MPU write is slower than panel read

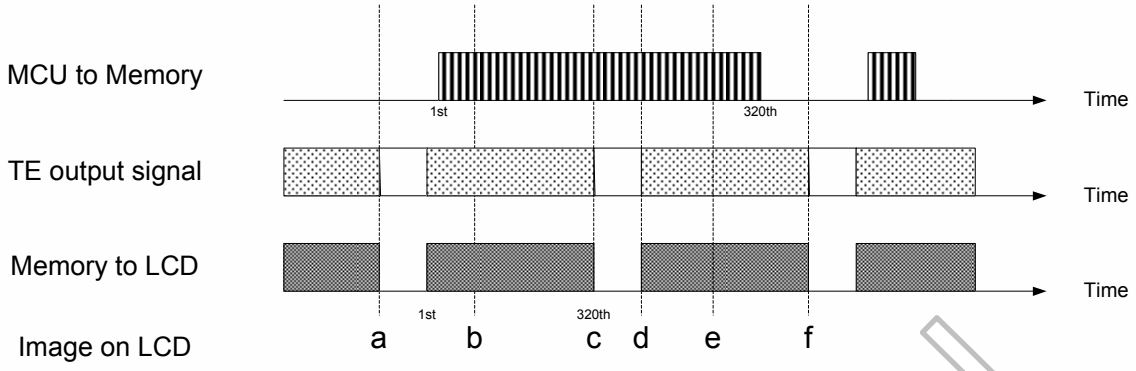

Figure 5-26: Timing of MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

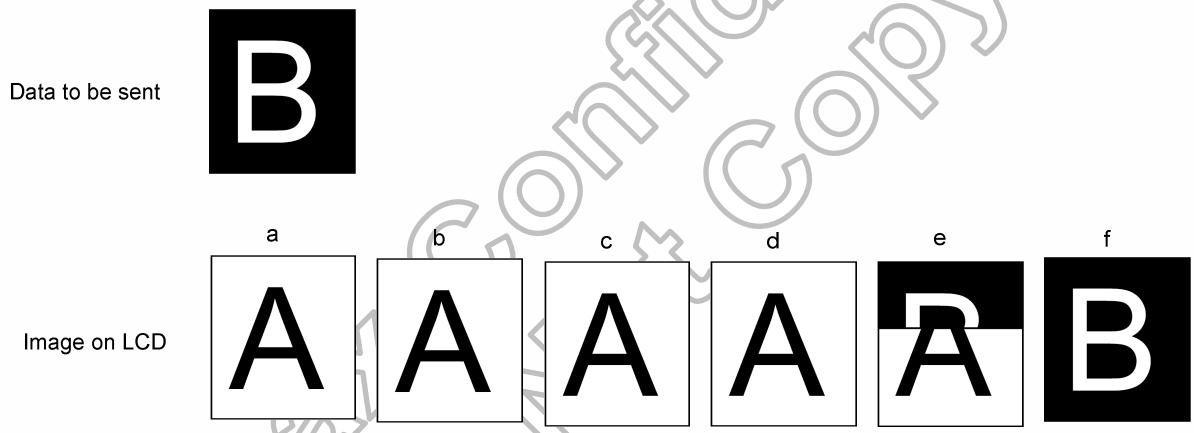

Figure 5-27: Display of MPU write is slower than panel read

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5.5 Oscillator

The HX8347-I can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, it can be adjusted by the **UADJ [3:0]** bits for initial 6MHz internal clock generation. With other dividers setting, the 6 MHz internal clock can be used to generate clock for other part of the chip using.

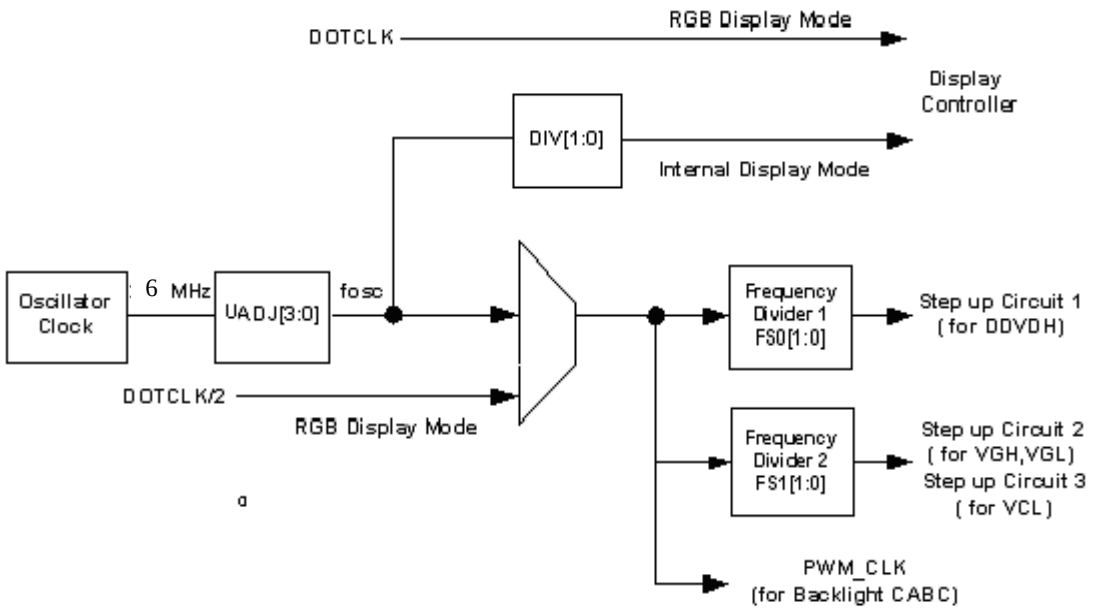

Figure 5-28: HX8347-I internal clock circuit

5.6 Source driver

The HX8347-I contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.7 Gate driver

The HX8347-I contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.8 Scan Mode Setting

HX8347-I can set internal register GS_PANEL bit to determine the pin assignment of gate. The GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8347-I.

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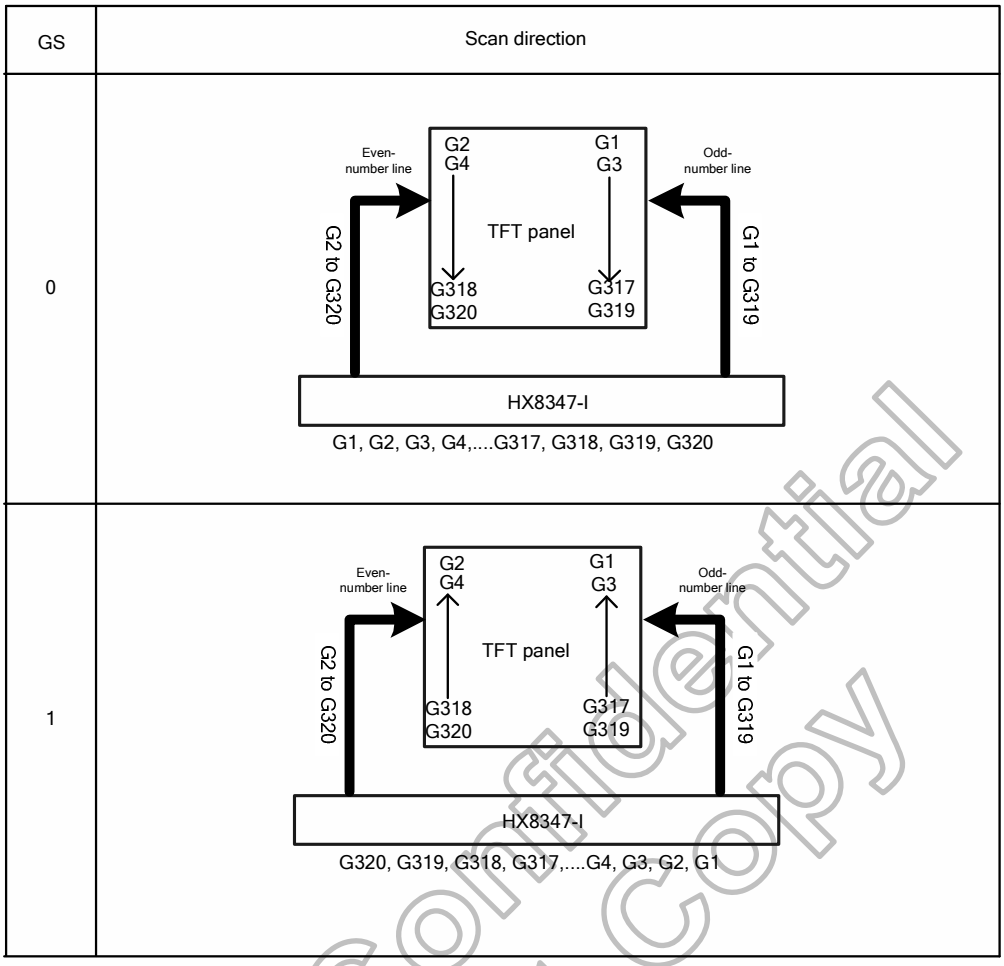

Figure 5-29: Gate scan mode

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5.9 LCD power generation circuit

5.9.1 Power supply circuit

The power circuit of HX8347-I is used to generate supply voltages for LCD panel driving.

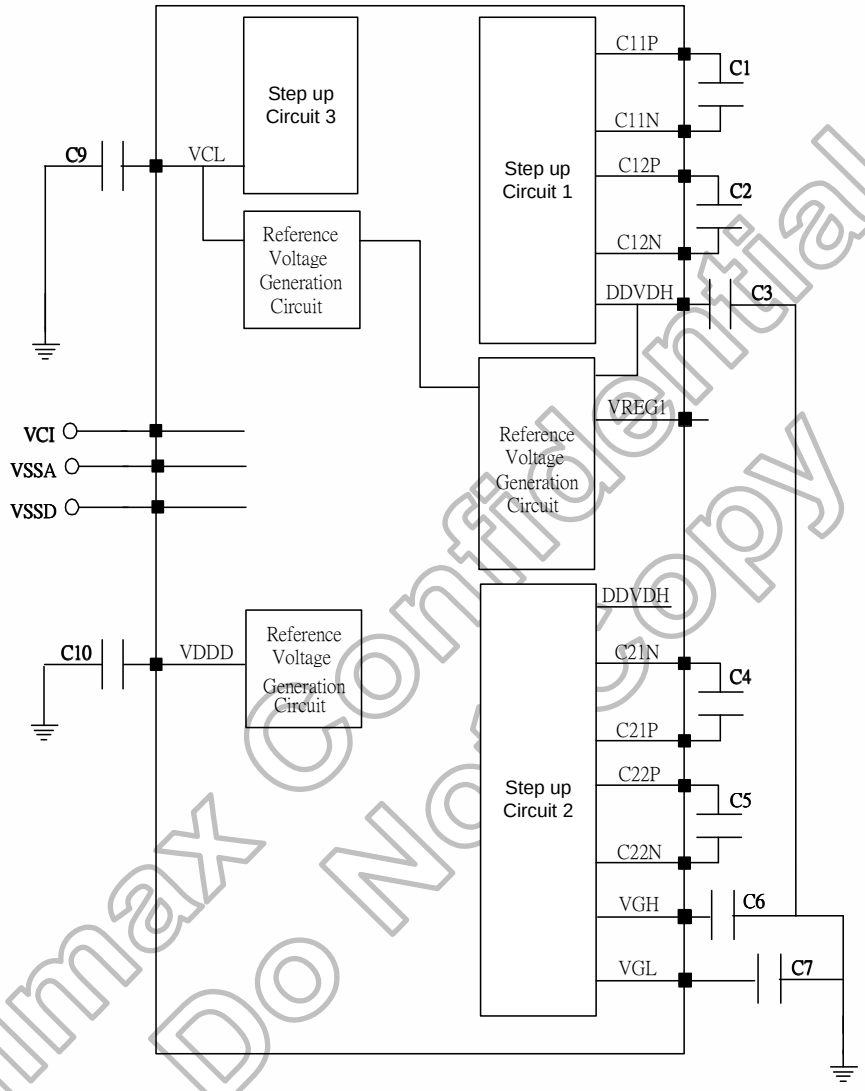

Figure 5-30: Block diagram of HX8347-I power circuit

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Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1 (C11P/N)	6V	1 µF (B characteristics)
C2 (C12P/N)	6V	1 µF (B characteristics)
C3 (DDVDH)	10V	1 µF (B characteristics)
C4 (C21P/N)	10V	1 µF (B characteristics)
C5 (C22P/N)	10V	1 µF (B characteristics)
C6 (VGH)	25V	1 µF (B characteristics)
C7 (VGL)	16V	1 µF (B characteristics)
C9 (VCL)	6V	1 µF (B characteristics)
C10(VDDD)	6V	1 µF (B characteristics)

Table 5-11: Adoptability of capacitor

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5.9.2 LCD power generation scheme

The boost voltage generated is shown as below.

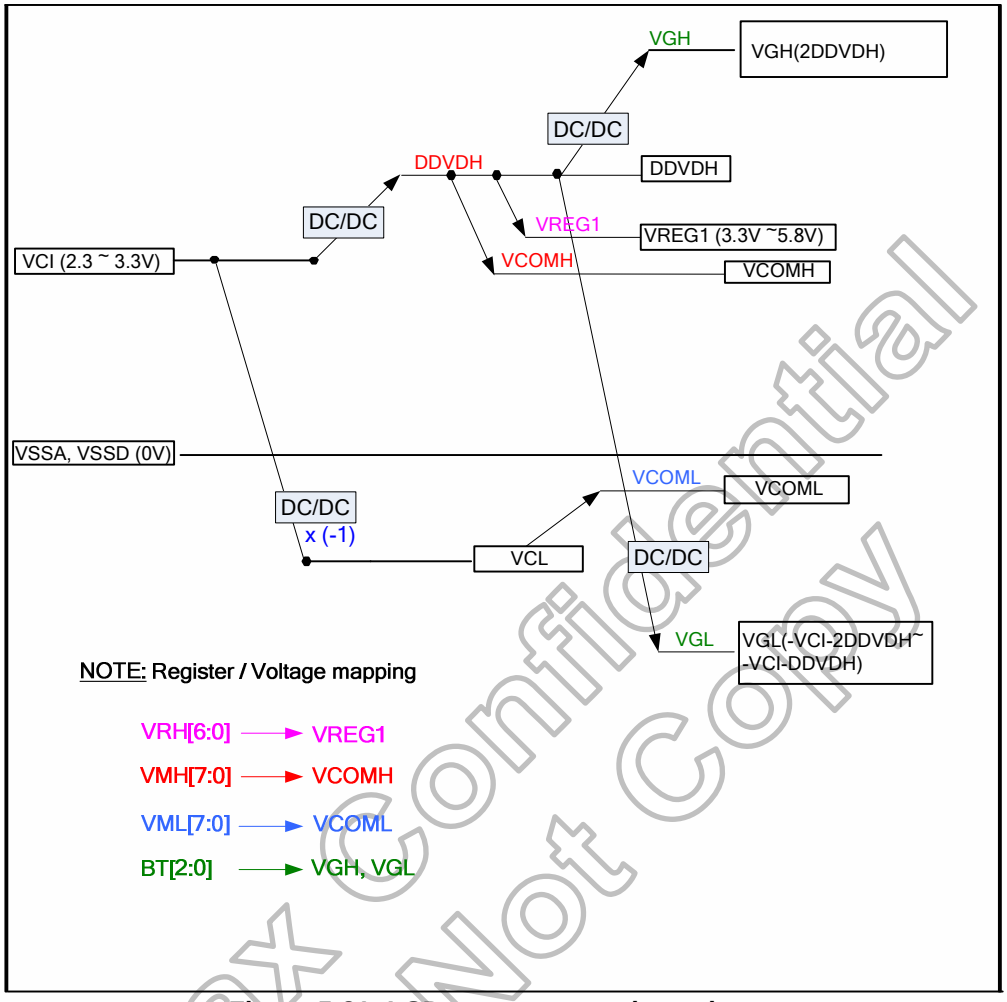

Figure 5-31: LCD power generation scheme

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5.10 Gamma characteristic correction function

The HX8347-I offers Gamma adjustment ways to come to accord with LC characteristic through Source Driver directly.

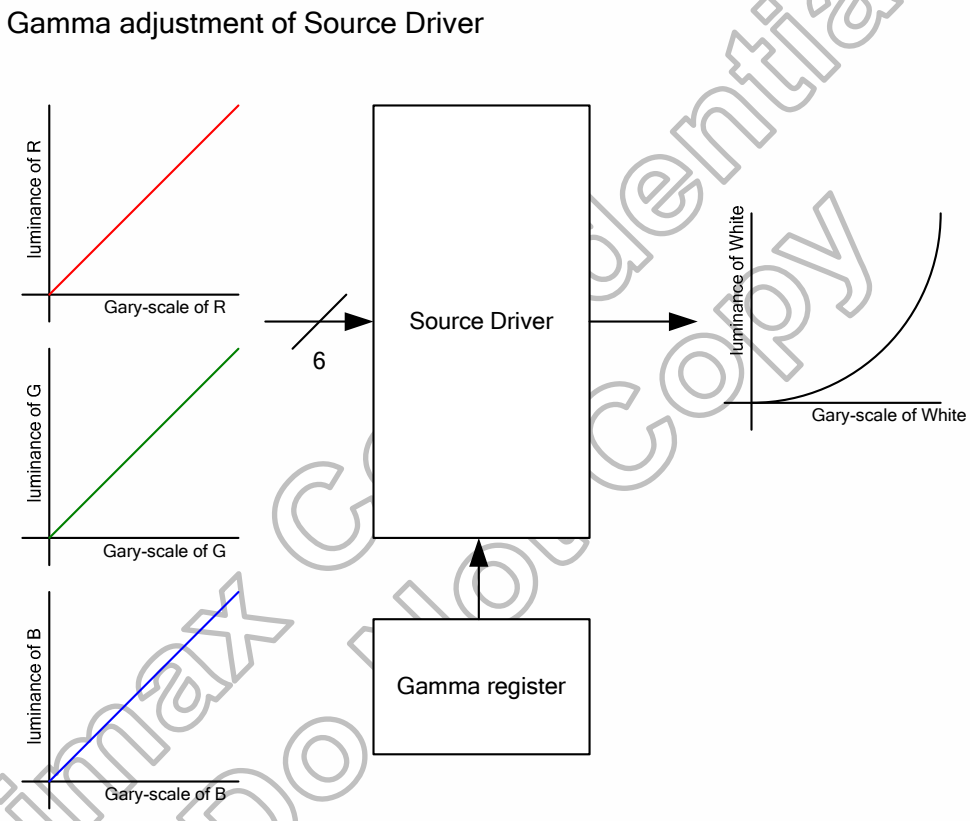

Figure 5-32: Gamma adjustments

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5.10.1 Gamma characteristic correction function

The HX8347-I incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

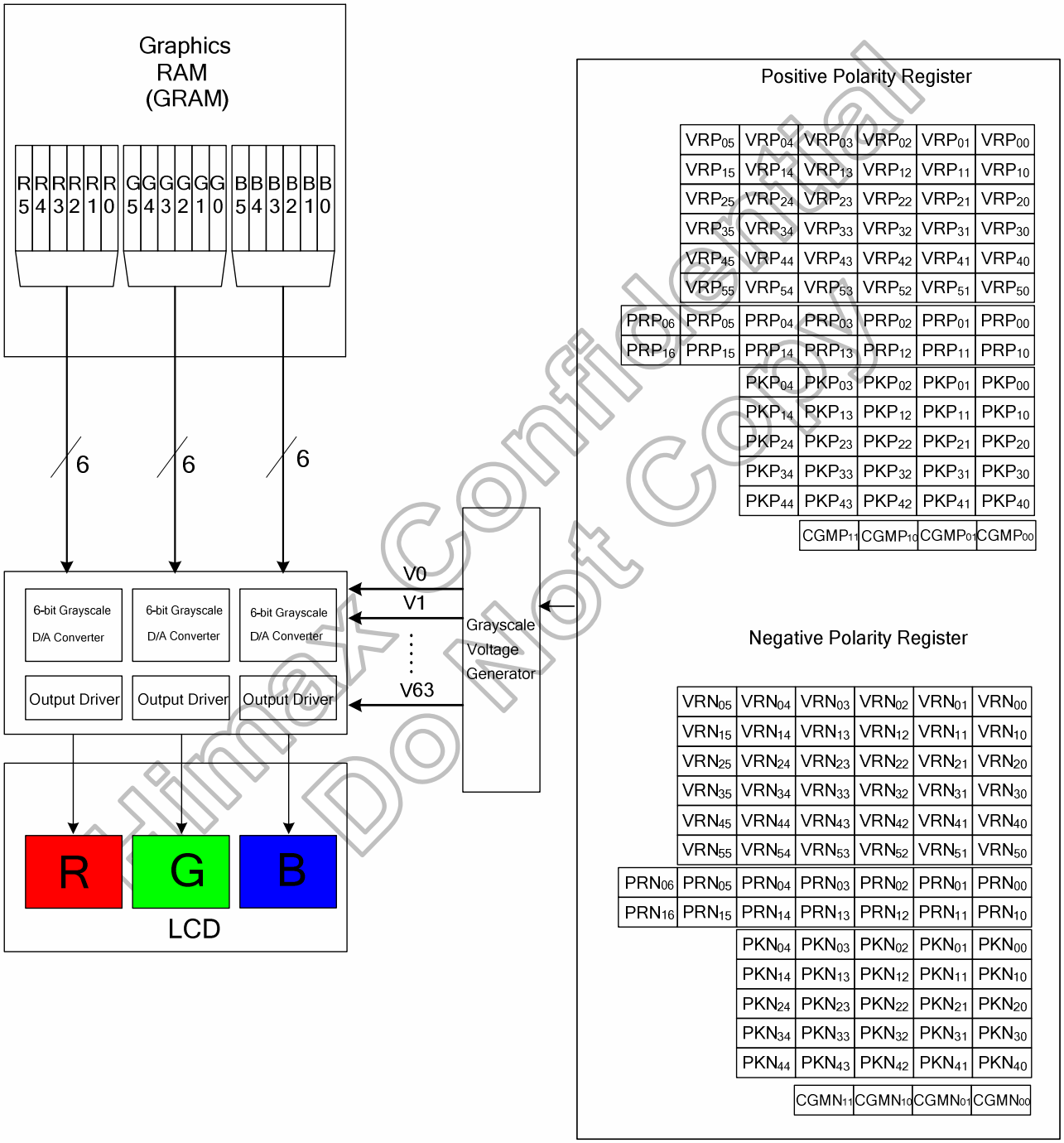

Figure 5-33: Grayscale control

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Gamma-characteristics adjustment registers

This HX8347-I has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by choosing one input of 64-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N) 3, 20, 32(31), 43, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	128-to-1 selector (voltage level of grayscale 8)
	PRP1 6-0	PRN1 6-0	128-to-1 selector (voltage level of grayscale 55)
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 43)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	64-to-1 selector (voltage level of grayscale 0)
	VRP1 5-0	VRN1 5-0	64-to-1 selector (voltage level of grayscale 1)
	VRP2 5-0	VRN2 5-0	64-to-1 selector (voltage level of grayscale 2)
	VRP3 5-0	VRN3 5-0	64-to-1 selector (voltage level of grayscale 61)
	VRP4 5-0	VRN4 5-0	64-to-1 selector (voltage level of grayscale 62)
	VRP5 5-0	VRN5 5-0	64-to-1 selector (voltage level of grayscale 63)

Table 5-12: Gamma-adjustment registers

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Gamma resister stream

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. VgP/N (0, 1, 2, 3, 8 20, 32(31), 43, 55, 60, 61, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

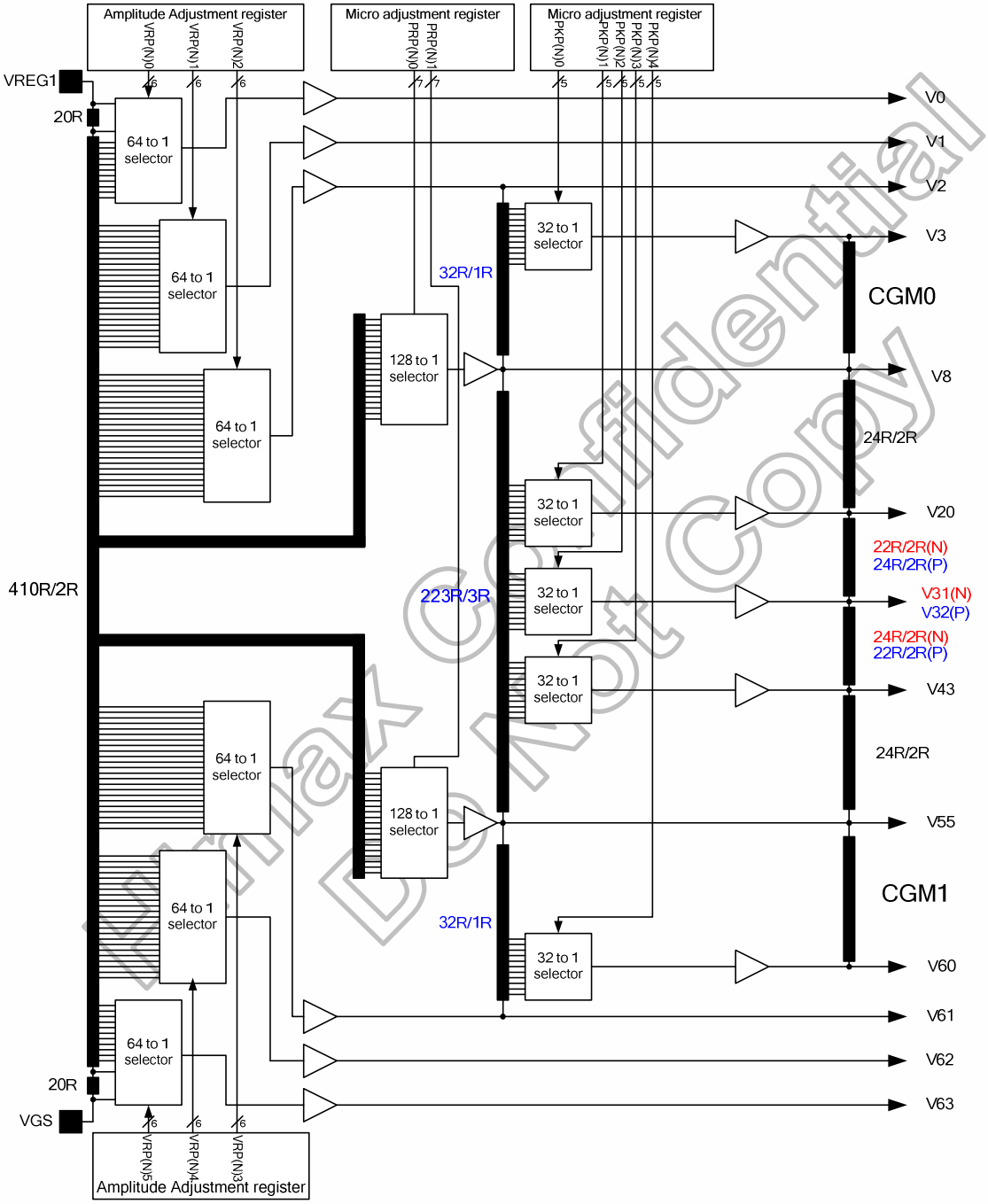

Figure 5-34: Gamma resister stream and gamma reference voltage

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Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0	Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1	Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	20R	000001	2R	000001	2R
000010	22R	000010	4R	000010	4R
000011	24R	000011	6R	000011	6R
• • •	• • •	• • •	• • •	• • •	• • •
011101	76R	011101	58R	011101	58R
011110	78R	011110	60R	011110	60R
011111	80R	011111	62R	011111	62R
100000	84R	100000	66R	100000	66R
100001	88R	100001	70R	100001	70R
100010	92R	100010	74R	100010	74R
• • •	• • •	• • •	• • •	• • •	• • •
111101	200R	111101	182R	111101	182R
111110	204R	111110	186R	111110	186R
111111	208R	111111	190R	111111	190R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3	Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4	Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	4R	000001	4R	000001	4R
000010	8R	000010	8R	000010	8R
• • •	• • •	• • •	• • •	• • •	• • •
011101	116R	011101	116R	011101	116R
011110	120R	011110	120R	011110	120R
011111	124R	011111	124R	011111	124R
100000	128R	100000	128R	100000	128R
100001	130R	100001	130R	100001	130R
100010	132R	100010	132R	100010	132R
• • •	• • •	• • •	• • •	• • •	• • •
111100	184R	111100	184R	111100	184R
111101	186R	111101	186R	111101	186R
111110	188R	111110	188R	111110	188R
111111	190R	111111	190R	111111	208R

Table 5-13: Offset adjustment 0 ~ 5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0	Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R	0000000	0R
0000001	2R	0000001	2R
0000010	4R	0000010	4R
• • •	• • •	• • •	• • •
1111101	250R	1010101	250R
1111110	252R	1111110	252R
1111111	254R	1111111	254R

Table 5-14: Center adjustment

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The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP/N0	VRP/N0 5-0 = 000000	VREG1
	VRP/N0 5-0 = 000001	((450R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000010	((450R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000011	((450R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000100	((450R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000101	((450R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000110	((450R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000111	((450R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001000	((450R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001001	((450R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001010	((450R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001011	((450R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001100	((450R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001101	((450R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001110	((450R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001111	((450R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010000	((450R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010001	((450R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010010	((450R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010011	((450R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010100	((450R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010101	((450R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010110	((450R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010111	((450R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011000	((450R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011001	((450R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011010	((450R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011011	((450R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011100	((450R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011101	((450R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011110	((450R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011111	((450R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100000	((450R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100001	((450R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100010	((450R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100011	((450R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100100	((450R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100101	((450R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100110	((450R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100111	((450R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101000	((450R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101001	((450R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101010	((450R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101011	((450R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101100	((450R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101101	((450R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101110	((450R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101111	((450R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110000	((450R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110001	((450R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110010	((450R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110011	((450R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110100	((450R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110101	((450R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110110	((450R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110111	((450R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111000	((450R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111001	((450R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111010	((450R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111011	((450R - 192R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111100	((450R - 196R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111101	((450R - 200R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111110	((450R - 204R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111111	((450R - 208R) / 450R) * (VREG1 - VGS) + VGS

Table 5-15: VinP/N 0

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Reference Voltage	Macro Adjustment Value	VinP/N1 Formula
VinP/N1	VRP/N1 5-0 = 000000	(430R / 450R) * (VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000001	((430R - 2R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000010	((430R - 4R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000011	((430R - 6R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000100	((430R - 8R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000101	((430R - 10R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000110	((430R - 12R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000111	((430R - 14R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001000	((430R - 16R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001001	((430R - 18R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001010	((430R - 20R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001011	((430R - 22R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001100	((430R - 24R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001101	((430R - 26R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001110	((430R - 28R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001111	((430R - 30R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010000	((430R - 32R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010001	((430R - 34R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010010	((430R - 36R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010011	((430R - 38R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010100	((430R - 40R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010101	((430R - 42R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010110	((430R - 44R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010111	((430R - 46R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011000	((430R - 48R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011001	((430R - 50R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011010	((430R - 52R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011011	((430R - 54R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011100	((430R - 56R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011101	((430R - 58R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011110	((430R - 60R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011111	((430R - 62R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100000	((430R - 66R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100001	((430R - 70R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100010	((430R - 74R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100011	((430R - 78R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100100	((430R - 82R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100101	((430R - 86R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100110	((430R - 90R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100111	((430R - 94R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101000	((430R - 98R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101001	((430R - 102R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101010	((430R - 106R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101011	((430R - 110R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101100	((430R - 114R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101101	((430R - 118R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101110	((430R - 122R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101111	((430R - 126R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110000	((430R - 130R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110001	((430R - 134R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110010	((430R - 138R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110011	((430R - 142R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110100	((430R - 146R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110101	((430R - 150R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110110	((430R - 154R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110111	((430R - 158R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111000	((430R - 162R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111001	((430R - 166R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111010	((430R - 170R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111011	((430R - 174R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111100	((430R - 178R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111101	((430R - 182R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111110	((430R - 186R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111111	((430R - 190R) / 450R) *(VREG1 - VGS) + VGS

Table 5-16: VinP/N 1

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Reference Voltage	Macro Adjustment Value	VinP/N2 Formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000001	((410R - 2R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000010	((410R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000011	((410R - 6R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000100	((410R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000101	((410R - 10R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000110	((410R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000111	((410R - 14R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001000	((410R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001001	((410R - 18R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001010	((410R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001011	((410R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001100	((410R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001101	((410R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001110	((410R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001111	((410R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010000	((410R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010001	((410R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010010	((410R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010011	((410R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010100	((410R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010101	((410R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010110	((410R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010111	((410R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011000	((410R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011001	((410R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011010	((410R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011011	((410R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011100	((410R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011101	((410R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011110	((410R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011111	((410R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100000	((410R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100001	((410R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100010	((410R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100011	((410R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100100	((410R - 82R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100101	((410R - 86R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100110	((410R - 90R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100111	((410R - 94R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101000	((410R - 98R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101001	((410R - 102R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101010	((410R - 106R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101011	((410R - 110R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101100	((410R - 114R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101101	((410R - 118R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101110	((410R - 122R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101111	((410R - 126R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110000	((410R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110001	((410R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110010	((410R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110011	((410R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110100	((410R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110101	((410R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110110	((410R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110111	((410R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111000	((410R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111001	((410R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111010	((410R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111011	((410R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111100	((410R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111101	((410R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111110	((410R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111111	((410R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 5-17: VinP/N 2

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Reference Voltage	Macro Adjustment Value	VinP/N10 Formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000001	((230R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000010	((230R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000011	((230R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000100	((230R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000101	((230R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000110	((230R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000111	((230R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001000	((230R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001001	((230R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001010	((230R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001011	((230R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001100	((230R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001101	((230R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001110	((230R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001111	((230R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010000	((230R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010001	((230R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010010	((230R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010011	((230R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010100	((230R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010101	((230R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010110	((230R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010111	((230R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011000	((230R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011001	((230R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011010	((230R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011011	((230R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011100	((230R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011101	((230R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011110	((230R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011111	((230R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100000	((230R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100001	((230R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100010	((230R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100011	((230R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100100	((230R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100101	((230R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100110	((230R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100111	((230R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101000	((230R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101001	((230R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101010	((230R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101011	((230R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101100	((230R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101101	((230R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101110	((230R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101111	((230R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110000	((230R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110001	((230R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110010	((230R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110011	((230R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110100	((230R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110101	((230R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110110	((230R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110111	((230R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111000	((230R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111001	((230R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111010	((230R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111011	((230R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111100	((230R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111101	((230R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111110	((230R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111111	((230R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 5-18: VinP/N 10

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Reference Voltage	Macro Adjustment Value	VinP/N11 Formula
VinP/N11	VRP/N4 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000001	((210R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000010	((210R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000011	((210R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000100	((210R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000101	((210R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000110	((210R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000111	((210R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001000	((210R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001001	((210R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001010	((210R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001011	((210R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001100	((210R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001101	((210R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001110	((210R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001111	((210R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010000	((210R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010001	((210R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010010	((210R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010011	((210R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010100	((210R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010101	((210R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010110	((210R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010111	((210R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011000	((210R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011001	((210R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011010	((210R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011011	((210R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011100	((210R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011101	((210R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011110	((210R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011111	((210R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100000	((210R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100001	((210R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100010	((210R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100011	((210R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100100	((210R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100101	((210R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100110	((210R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100111	((210R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101000	((210R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101001	((210R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101010	((210R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101011	((210R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101100	((210R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101101	((210R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101110	((210R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101111	((210R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110000	((210R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110001	((210R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110010	((210R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110011	((210R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110100	((210R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110101	((210R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110110	((210R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110111	((210R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111000	((210R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111001	((210R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111010	((210R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111011	((210R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111100	((210R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111101	((210R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111110	((210R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111111	((210R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 5-19: VinP/N 11

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Reference Voltage	Macro Adjustment Value	VinP/N12 Formula
VinP/N12	VRP/N5 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000001	((208R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000010	((208R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000011	((208R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000100	((208R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000101	((208R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000110	((208R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000111	((208R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001000	((208R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001001	((208R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001010	((208R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001011	((208R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001100	((208R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001101	((208R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001110	((208R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001111	((208R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010000	((208R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010001	((208R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010010	((208R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010011	((208R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010100	((208R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010101	((208R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010110	((208R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010111	((208R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011000	((208R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011001	((208R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011010	((208R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011011	((208R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011100	((208R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011101	((208R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011110	((208R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011111	((208R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100000	((208R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100001	((208R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100010	((208R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100011	((208R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100100	((208R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100101	((208R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100110	((208R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100111	((208R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101000	((208R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101001	((208R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101010	((208R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101011	((208R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101100	((208R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101101	((208R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101110	((208R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101111	((208R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110000	((208R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110001	((208R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110010	((208R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110011	((208R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110100	((208R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110101	((208R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110110	((208R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110111	((208R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111000	((208R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111001	((208R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111010	((208R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111011	((208R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111100	((208R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111101	((208R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111110	((208R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111111	VGS

Table 5-20: VinP/N 12

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Reference Voltage	Macro Adjustment Value	VinP/N4 Formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000001	((350R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000010	((350R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000111	((350R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010001	((350R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011011	((350R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100000	((350R - 64R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101010	((350R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111110	((350R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000010	((350R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VREG1 - VGS) + VGS

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	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001100	((350R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010111	((350R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101111	((350R – 223R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111001	((350R – 243R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VREG1 - VGS) + VGS

Table 5-21: VinP/N4

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Reference Voltage	Macro Adjustment Value	VinP/N8 Formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000001	((354R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000010	((354R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000111	((354R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010001	((354R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011011	((354R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100000	((354R - 64R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101010	((354R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111110	((354R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000010	((354R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VREG1 - VGS) + VGS

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	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001100	((354R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010111	((354R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011001	((354R - 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011100	((354R - 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011110	((354R - 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100001	((354R - 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100011	((354R - 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100110	((354R - 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100111	((354R - 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101000	((354R - 208R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101011	((354R - 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101101	((354R - 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110000	((354R - 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110010	((354R - 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110101	((354R - 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110111	((354R - 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111010	((354R - 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111100	((354R - 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111111	((354R - 254R) / 450R) * (VREG1 - VGS) + VGS

Table 5-22: VinP/N 8

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Reference Voltage	Macro Adjustment Value	VinP/N3 Formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4

Table 5-23: VinP/N 3

Reference Voltage	Macro Adjustment Value	VinP/N7 Formula
VinP/N5	PKP/N1 4-0 = 00000	(193R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00001	((193R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00010	((193R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00011	((193R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N14-0 = 00100	((193R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00101	((193R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00110	((193R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00111	((193R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01000	((193R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01001	((193R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01010	((193R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01011	((193R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01100	((193R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01101	((193R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01110	((193R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01111	((193R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10000	((193R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10001	((193R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10010	((193R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10011	((193R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10100	((193R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10101	((193R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10110	((193R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10111	((193R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11000	((193R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11001	((193R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11010	((193R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11011	((193R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11100	((193R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11101	((193R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11110	((193R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11111	((193R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 5-24: VinP/N 5

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Reference Voltage	Macro Adjustment Value	VinP/N6 Formula
VinP/N6	PKP/N2 4-0 = 00000	(158R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00001	((158R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00010	((158R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00011	((158R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00100	((158R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00101	((158R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00110	((158R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00111	((158R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01000	((158R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01001	((158R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01010	((158R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01011	((158R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01100	((158R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01101	((158R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01110	((158R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01111	((158R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10000	((158R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10001	((158R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10010	((158R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10011	((158R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10100	((158R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10101	((158R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10110	((158R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10111	((158R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11000	((158R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11001	((158R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11010	((158R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11011	((158R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11100	((158R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11101	((158R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11110	((158R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11111	((158R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 5-25: VinP/N 6

Reference Voltage	Macro Adjustment Value	VinP/N7 Formula
VinP/N7	PKP/N3 4-0 = 00000	(123R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((123R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((123R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((123R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((123R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((123R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((123R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((123R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((123R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((123R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((123R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((123R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((123R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((123R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((123R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((123R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((123R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((123R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((123R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((123R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((123R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((123R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((123R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((123R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((123R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((123R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((123R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((123R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((123R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((123R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((123R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((123R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 5-26: VinP/N 7

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Reference Voltage	Macro Adjustment Value	VinP/N9 Formula
VinP/N9	PKP/N4 4-0 = 00000	(31R / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00001	((31R - 1R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00010	((31R - 2R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00011	((31R - 3R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00100	((31R - 4R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00101	((31R - 5R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00110	((31R - 6R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00111	((31R - 7R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01000	((31R - 8R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01001	((31R - 9R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10

Table 5-27: VinP/N 9

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VinP0	V32	VinP6
V1	VinP1	V33	VinP7+(VinP6- VinP7)*(20R/22R)
V2	VinP2	V34	VinP7+(VinP6- VinP7)*(18R/22R)
V3	VinP3	V35	VinP7+(VinP6- VinP7)*(16R/22R)
V4	VinP4+ (VinP3 - VinP4)*CT1	V36	VinP7+(VinP6- VinP7)*(14R/22R)
V5	VinP4+ (VinP3 - VinP4)*CT2	V37	VinP7+(VinP6- VinP7)*(12R/22R)
V6	VinP4+ (VinP3 - VinP4)*CT3	V38	VinP7+(VinP6- VinP7)*(10R/22R)
V7	VinP4+ (VinP3 - VinP4)*CT4	V39	VinP7+(VinP6- VinP7)*(8R/22R)
V8	VinP4	V40	VinP7+(VinP6- VinP7)*(6R/22R)
V9	VinP5+(VinP4- VinP5)*0.875	V41	VinP7+(VinP6- VinP7)*(4R/22R)
V10	VinP5+(VinP4- VinP5)*0.75	V42	VinP7+(VinP6- VinP7)*(2R/22R)
V11	VinP5+(VinP4- VinP5)*0.6806	V43	VinP7
V12	VinP5+(VinP4- VinP5)*0.5833	V44	VinP8+(VinP7- VinP8)*0.9444
V13	VinP5+(VinP4- VinP5)*0.4861	V45	VinP8+(VinP7- VinP8)*0.875
V14	VinP5+(VinP4- VinP5)*0.4028	V46	VinP8+(VinP7- VinP8)*0.7917
V15	VinP5+(VinP4- VinP5)*0.3333	V47	VinP8+(VinP7- VinP8)*0.7083
V16	VinP5+(VinP4- VinP5)*0.2639	V48	VinP8+(VinP7- VinP8)*0.6250
V17	VinP5+(VinP4- VinP5)*0.1944	V49	VinP8+(VinP7- VinP8)*0.5417
V18	VinP5+(VinP4- VinP5)*0.125	V50	VinP8+(VinP7- VinP8)*0.4583
V19	VinP5+(VinP4- VinP5)*0.0556	V51	VinP8+(VinP7- VinP8)*0.3611
V20	VinP5	V52	VinP8+(VinP7- VinP8)*0.2778
V21	VinP6+(VinP5- VinP6)*0.8889	V53	VinP8+(VinP7- VinP8)*0.1806
V22	VinP6+(VinP5- VinP6)*0.8056	V54	VinP8+(VinP7- VinP8)*0.0972
V23	VinP6+(VinP5- VinP6)*0.6944	V55	VinP8
V24	VinP6+(VinP5- VinP6)*0.6389	V56	VinP9+ (VinP8 – VinP9)*CB1
V25	VinP6+(VinP5- VinP6)*-0.5556	V57	VinP9+ (VinP8 – VinP9)*CB2
V26	VinP6+(VinP5- VinP6)*0.4722	V58	VinP9+ (VinP8 – VinP9)*CB3
V27	VinP6+(VinP5- VinP6)*0.3889	V59	VinP9+ (VinP8 – VinP9)*CB4
V28	VinP6+(VinP5- VinP6)*0.3056	V60	VinP9
V29	VinP6+(VinP5- VinP6)*0.2222	V61	VinP10
V30	VinP6+(VinP5- VinP6)*0.1389	V62	VinP11
V31	VinP6+(VinP5- VinP6)*0.0556	V63	VinP12

Table 5-28: Voltage calculation formula of 64-grayscale voltage (positive polarity)

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CGMP0[1:0]	"00"	"01"	"10"	"11"
CT1	169/216	28/45	146/198	3/4
CT2	127/216	4/15	100/198	21/40
CT3	7/18	7/45	63/198	13/40
CT4	43/216	1/15	30/198	3/20

CGMP1[1:0]	"00"	"01"	"10"	"11"
CB1	4/5	18/19	240/282	91/120
CB2	3/5	50/57	193/282	37/72
CB3	2/5	15/19	138/282	113/360
CB4	1/5	23/57	77/282	17/120

Table 5-29: Voltage calculation formula of grayscale voltage V4~V7 and V56~V59

Grayscale Voltage	Formula
V63	VinN0
V62	VinN1
V61	VinN2
V60	VinN3
V59	VinN4+ (VinN3 - VinN4)*CT1
V58	VinN4+ (VinN3 - VinN4)*CT2
V57	VinN4+ (VinN3 - VinN4)*CT3
V56	VinN4+ (VinN3 - VinN4)*CT4
V55	VinN4
V54	VinN5+(VinN4- VinN5)*0.9028
V53	VinN5+(VinN4- VinN5)*0.8194
V52	VinN5+(VinN4- VinN5)*0.7222
V51	VinN5+(VinN4- VinN5)*0.6389
V50	VinN5+(VinN4- VinN5)*0.5417
V49	VinN5+(VinN4- VinN5)*0.4583
V48	VinN5+(VinN4- VinN5)*0.3750
V47	VinN5+(VinN4- VinN5)*0.2917
V46	VinN5+(VinN4- VinN5)*0.2083
V45	VinN5+(VinN4- VinN5)*0.1250
V44	VinN5+(VinN4- VinN5)*0.0556
V43	VinN5
V42	VinN6+(VinN5- VinN6)*(20R/22R)
V41	VinN6+(VinN5- VinN6)*(18R/22R)
V40	VinN6+(VinN5- VinN6)*(16R/22R)
V39	VinN6+(VinN5- VinN6)*(14R/22R)
V38	VinN6+(VinN5- VinN6)*(12R/22R)
V37	VinN6+(VinN5- VinN6)*(10R/22R)
V36	VinN6+(VinN5- VinN6)*(8R/22R)
V35	VinN6+(VinN5- VinN6)*(6R/22R)
V34	VinN6+(VinN5- VinN6)*(4R/22R)
V33	VinN6+(VinN5- VinN6)*(2R/22R)
V32	VinN6

Grayscale Voltage	Formula
V31	VinN7+(VinN6- VinN7)*0.9444
V30	VinN7+(VinN6- VinN7)*0.8611
V29	VinN7+(VinN6- VinN7)*0.7778
V28	VinN7+(VinN6- VinN7)*0.6944
V27	VinN7+(VinN6- VinN7)*0.6111
V26	VinN7+(VinN6- VinN7)*0.5278
V25	VinN7+(VinN6- VinN7)*0.4444
V24	VinN7+(VinN6- VinN7)*0.3611
V23	VinN7+(VinN6- VinN7)*0.3056
V22	VinN7+(VinN6- VinN7)*0.1944
V21	VinN7+(VinN6- VinN7)*0.1111
V20	VinN7
V19	VinN8+(VinN7- VinN8)*0.9444
V18	VinN8+(VinN7- VinN8)*0.875
V17	VinN8+(VinN7- VinN8)* 0.8056
V16	VinN8+(VinN7- VinN8)*0.7361
V15	VinN8+(VinN7- VinN8)*0.6667
V14	VinN8+(VinN7- VinN8)*0.5972
V13	VinN8+(VinN7- VinN8)*0.5139
V12	VinN8+(VinN7- VinN8)*0.4167
V11	VinN8+(VinN7- VinN8)*0.3194
V10	VinN8+(VinN7- VinN8)*0.25
V9	VinN8+(VinN7- VinN8)*0.125
V8	VinN8
V7	VinN9+ (VinN8 – VinN9)*CB1
V6	VinN9+ (VinN8 – VinN9)*CB2
V5	VinN9+ (VinN8 – VinN9)*CB3
V4	VinN9+ (VinN8 – VinN9)*CB4
V3	VinN9
V2	VinN10
V1	VinN11
V0	VinN12

Table 5-30: Voltage calculation formula of 64-grayscale voltage (negative polarity)

CGMN1[1:0]	"00"	"01"	"10"	"11"
CT1	4/5	34/57	205/282	103/120
CT2	3/5	4/19	24/47	247/360
CT3	2/5	7/57	89/282	35/72
CT4	1/5	1/19	7/47	29/120

CGMN0[1:0]	"00"	"01"	"10"	"11"
CB1	173/216	14/15	28/33	17/20
CB2	11/18	38/45	23/33	27/40
CB3	89/216	11/15	49/99	19/40
CB4	47/216	17/45	26/99	1/4

Table 5-31: Voltage calculation formula of grayscale voltage V59~V56 and V7~V4

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Relationship between GRAM Data and Output Level ("Normally White Panel", GRAM data=0)

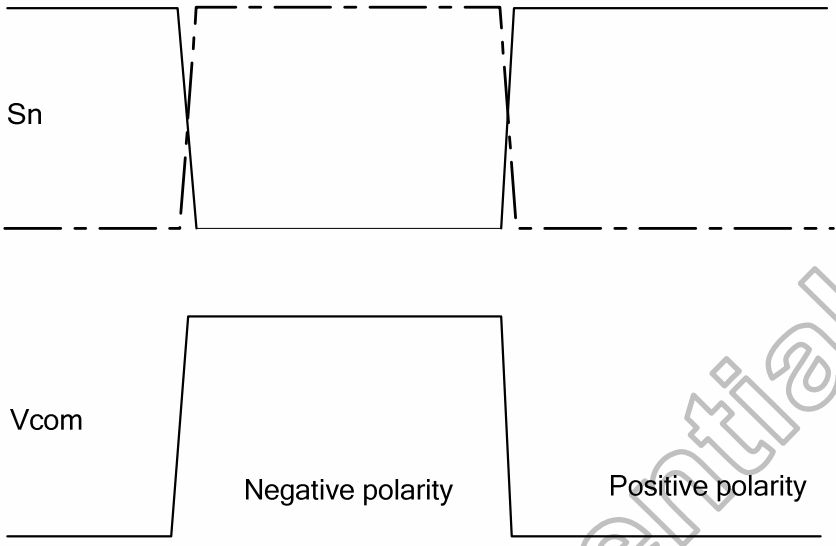
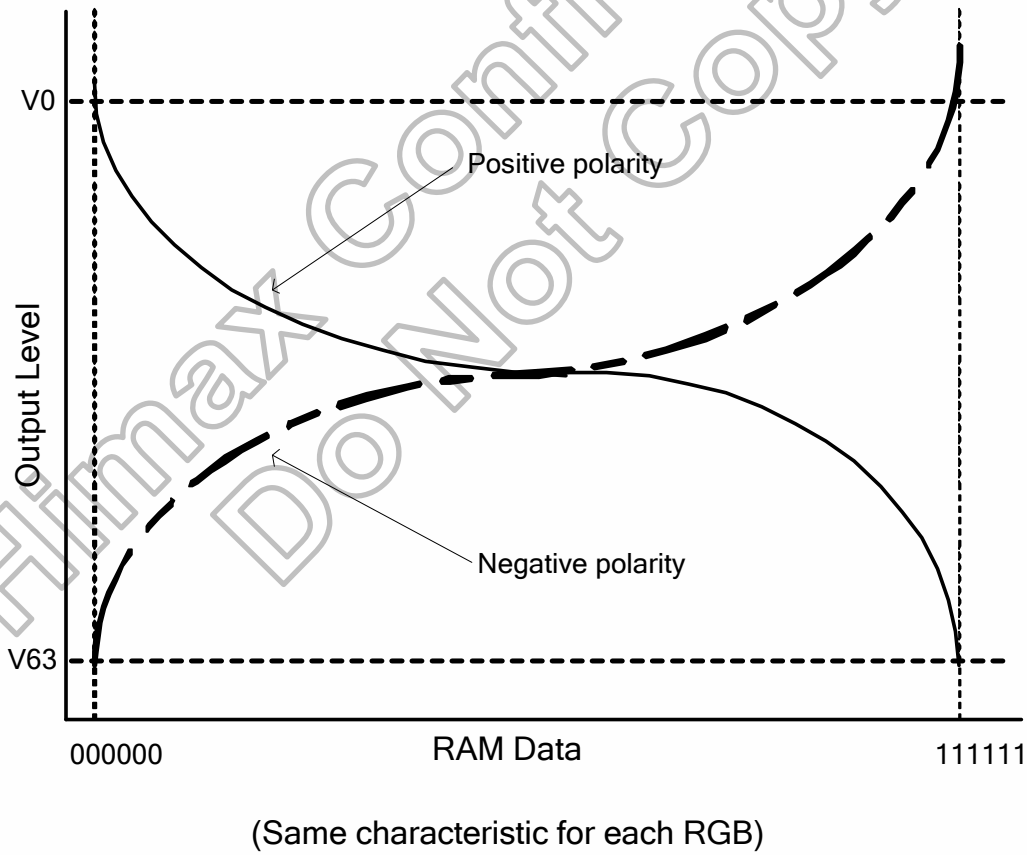


Figure 5-35: Relationship between source output and Vcom



(Same characteristic for each RGB)

Figure 5-36: Relationship between GRAM data and output level (normal white panel REV_Panel="0")

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Four-characteristic gamma curve selection

There are four kinds of Gamma Curve which can be selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

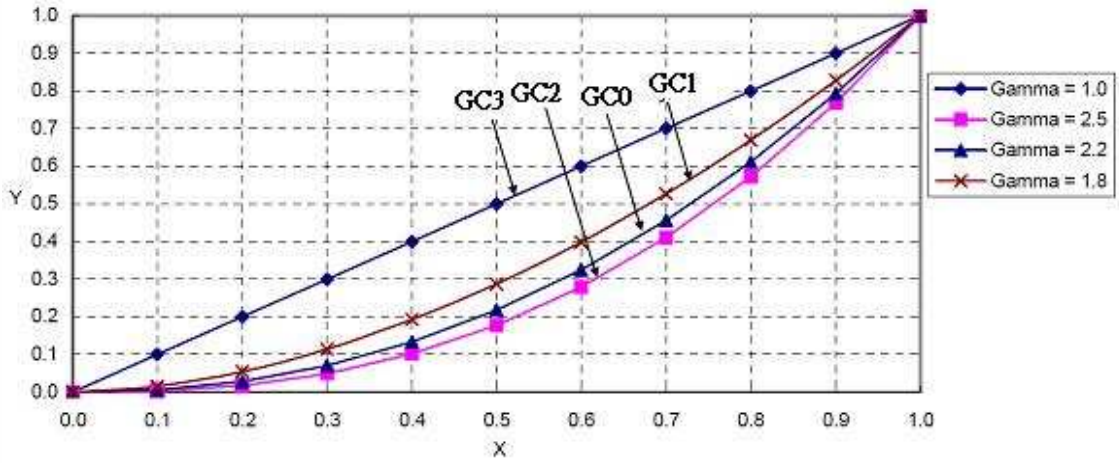

Figure 5-37: Gamma curve according to GC0 to GC3 bit

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5.11 Power function

5.11.1 Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order.
IOVCC, VCI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.
During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

Note: (1) There will be no damage to the display module if the power sequences are not met.
(2) There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
(3) There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
(4) If NRESET line is not held stable by host during Power on Sequence as defined in Sections 6.6.1.1 and 6.6.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence to ensure correct operation. Otherwise correct function is not guaranteed.

If NRESET line is not held stable by host during Power on Sequence as defined in Sections 5.11.1.1 and 5.11.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence is complete to ensure correct operation, otherwise correct functionality is not guaranteed. The power on/off sequence is illustrated as below

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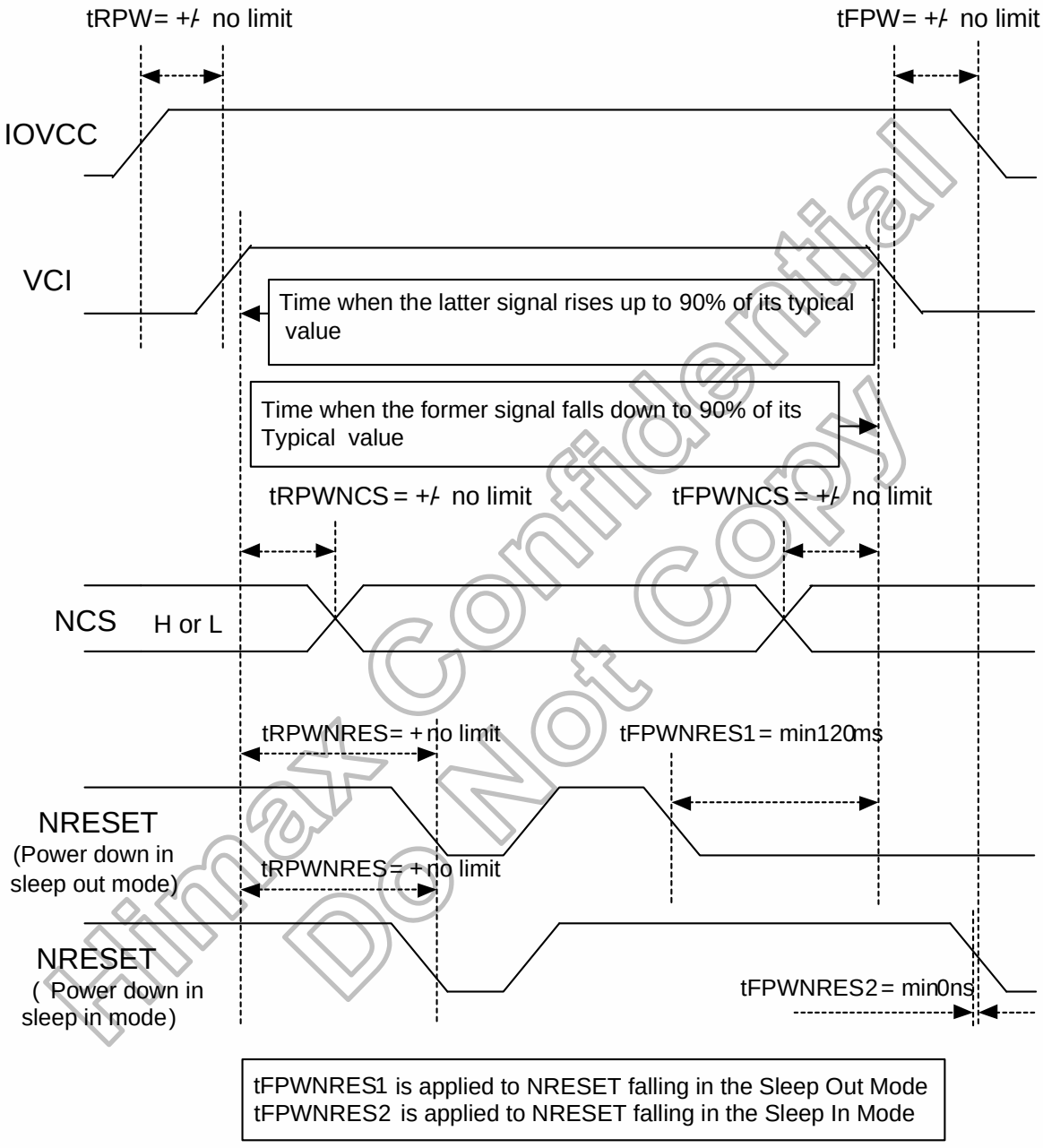
5.11.1.1 Case 1 – NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCI have been applied, otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5-38: Case 1 – NRESET line is held high or unstable by host at power on

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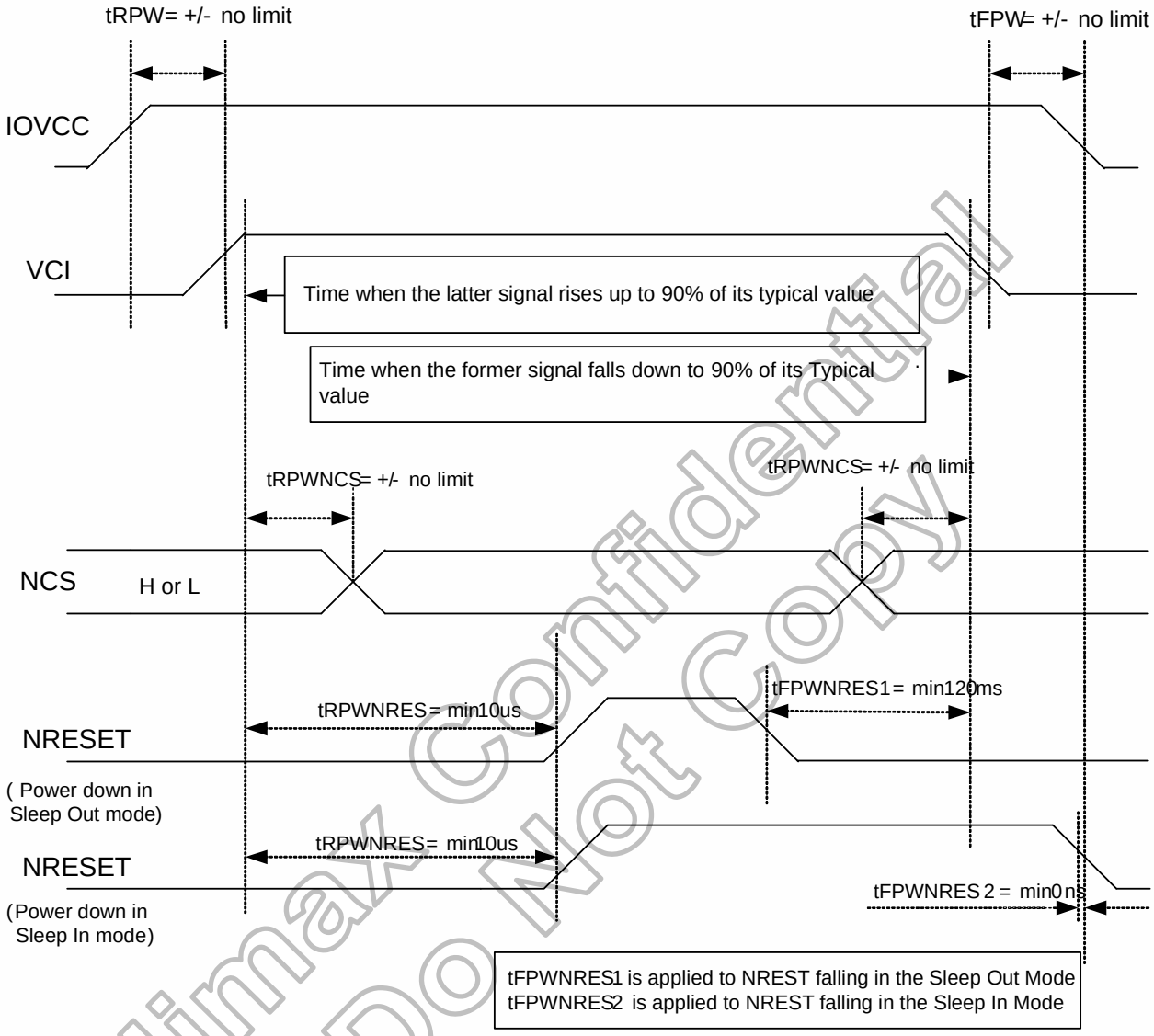
5.11.1.2 Case 2 – NRESET line is held low by host at power on

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after VCI have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5-39: NRESET line is held low by host at power on

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5.11.2 Power levels definition

5.11.2.1 General definition for power levels on system interface (RCM[1:0]="0x")

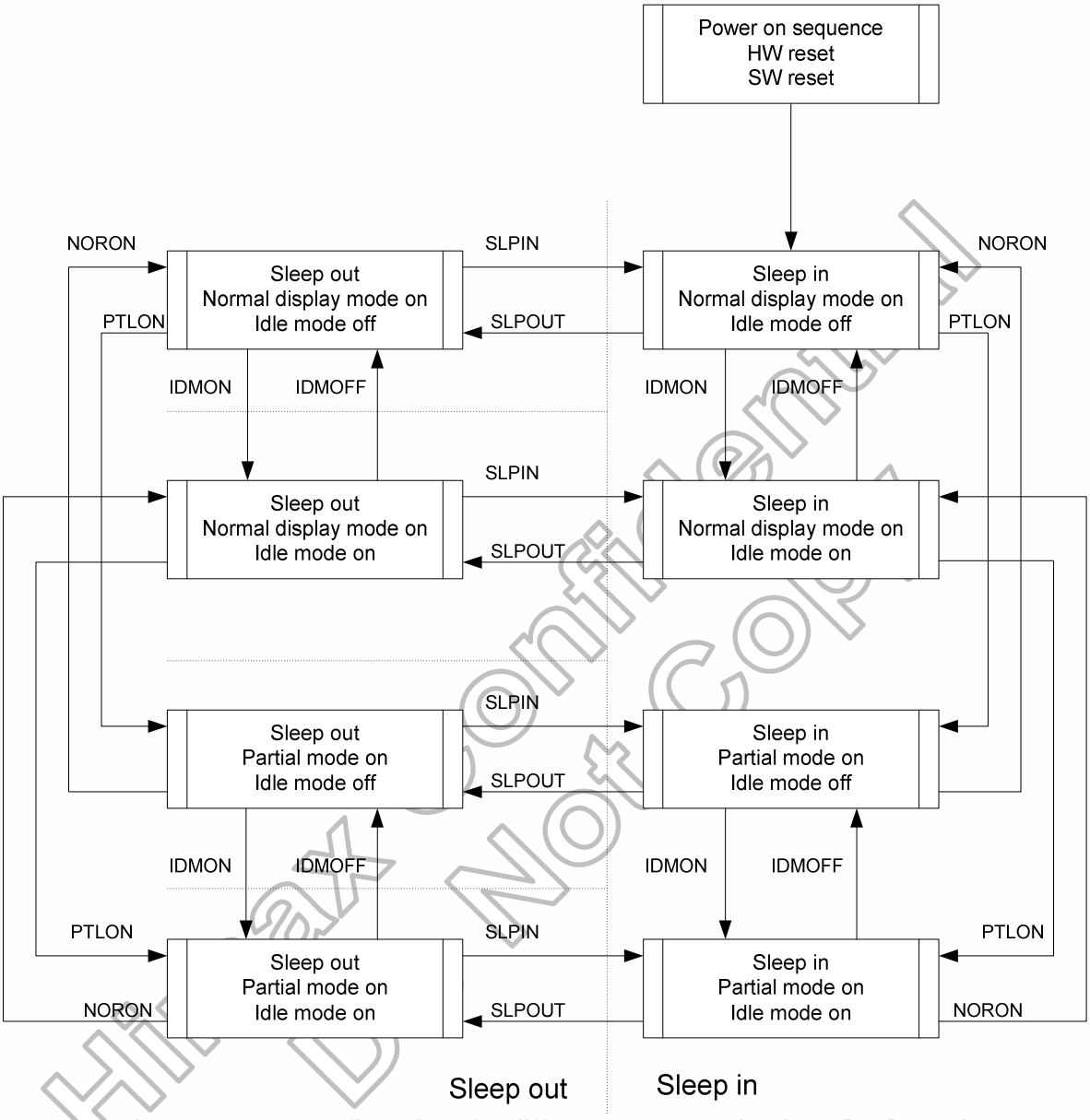

Figure 5-40: Power flow chart for different power modes (RCM[1:0]="0x")

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5.11.2.2 General definition for power levels on RGB interface (RCM[1:0]=”1x”)

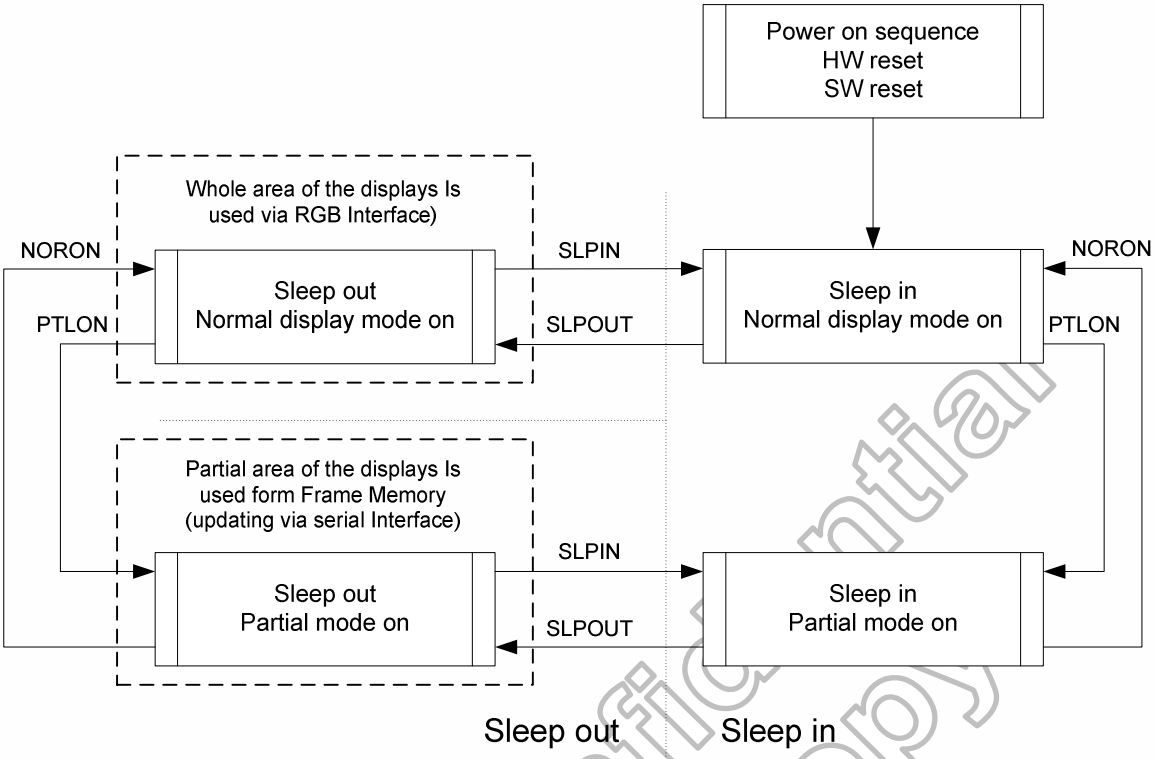

Figure 5-41: Power flow chart for different power modes (RCM[1:0]=”1x”)

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5.12 Input / output pin state

5.12.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
BC_CTRL	Low	Low
CABC_PWM_OUT	Low	Low

Table 5-32: Characteristics of output pins

5.12.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
NRESET	Input valid	Input valid	Input valid	Input valid
NCS	Input invalid	Input valid	Input valid	Input invalid
NWR_SCL	Input invalid	Input valid	Input valid	Input invalid
NRD	Input invalid	Input valid	Input valid	Input invalid
DNC_SCL	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
OSC, IM3, IM2, IM1,IM0, IFSEL	Input invalid	Input valid	Input valid	Input invalid
TEST2-1	Input invalid	Input valid	Input valid	Input invalid

Table 5-33: Characteristics of input pins

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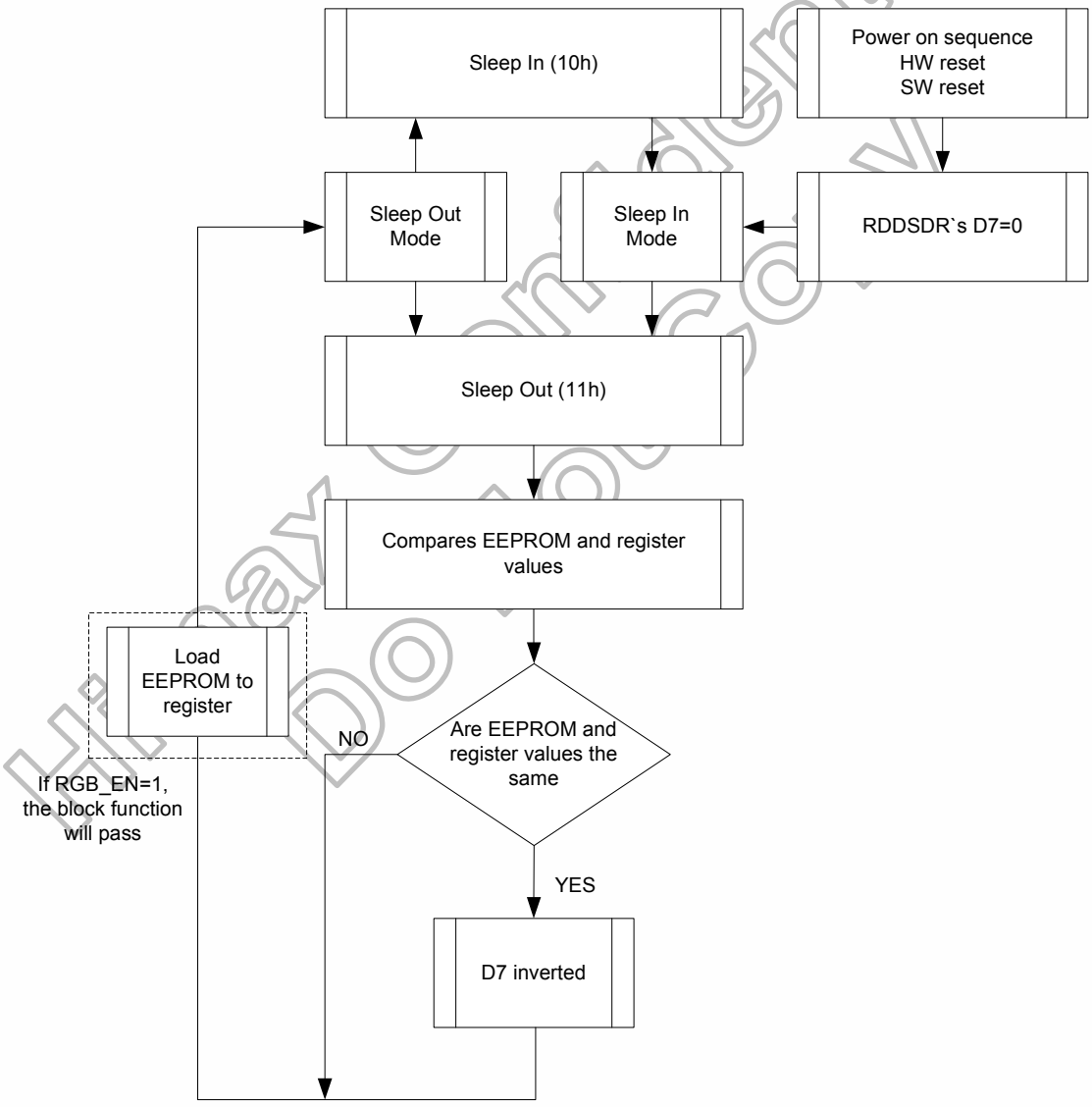
5.13 Sleep out – command and self-diagnostic functions of display module

5.13.1 Register loading detection

Sleep Out-command (See section 6.2.15 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in section 6.2.13 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The bit used for this command is D7). If those both values are not the same, this bit (D7) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

Figure 5-42: RDDSDR register loading detection flow

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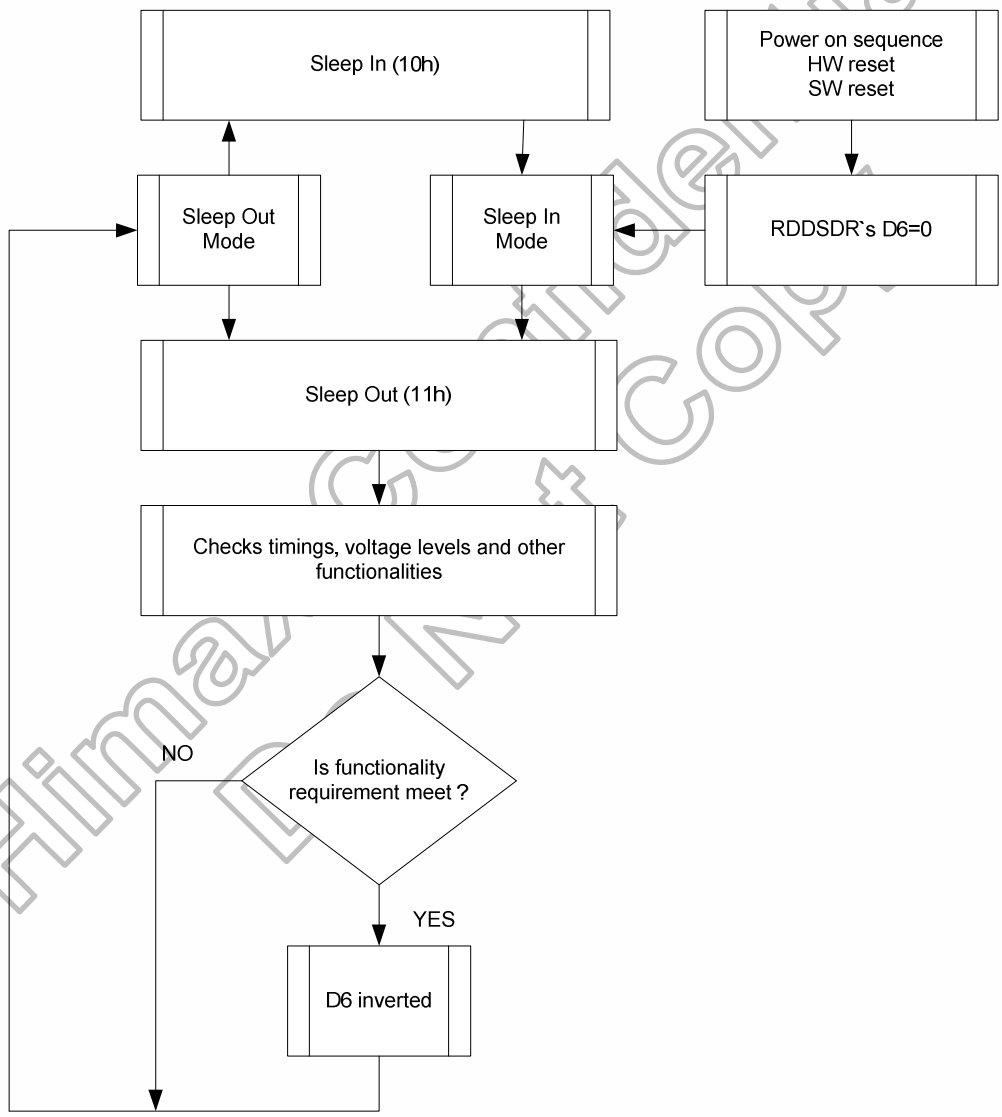
5.13.2 Functionality detection

Sleep Out-command (See section 6.2.15 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in section 6.2.13 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5-43: Functionality detection flow

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5.14 OTP table

	YA[2:0]=111	YA[2:0]=110	YA[2:0]=101	YA[2:0]=100	YA[2:0]=011	YA[2:0]=010	YA[2:0]=001	YA[2:0]=000	Non-Program
XA[4:0]=00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00h
XA[4:0]=01h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00h
XA[4:0]=02h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00h
XA[4:0]=03h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00h
XA[4:0]=04h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00h
XA[4:0]=05h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00h
XA[4:0]=06h	VMF17	VMF16	VMF15	VMF14	VMF13	VMF12	VMF11	VMF10	00h
XA[4:0]=07h	VMF27	VMF26	VMF25	VMF24	VMF23	VMF22	VMF21	VMF20	00h
XA[4:0]=08h	VMF37	VMF36	VMF35	VMF34	VMF33	VMF32	VMF31	VMF30	00h
XA[4:0]=09h	Valid_IDG1	Valid_IDG2	-			Valid_VMF1	Valid_VMF2	Valid_VMF3	00h

Table 5-34: OTP address mapping

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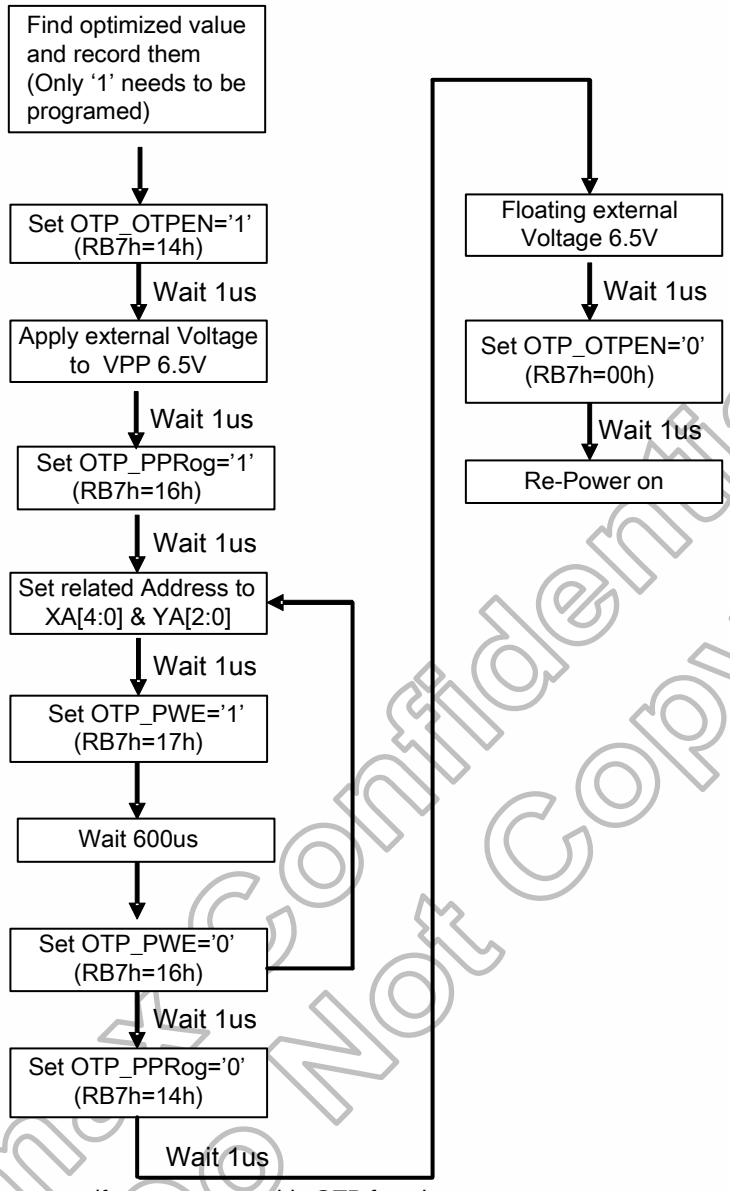
5.14.1 OTP programming flow



Note: Valid bit must program if user want use this OTP function

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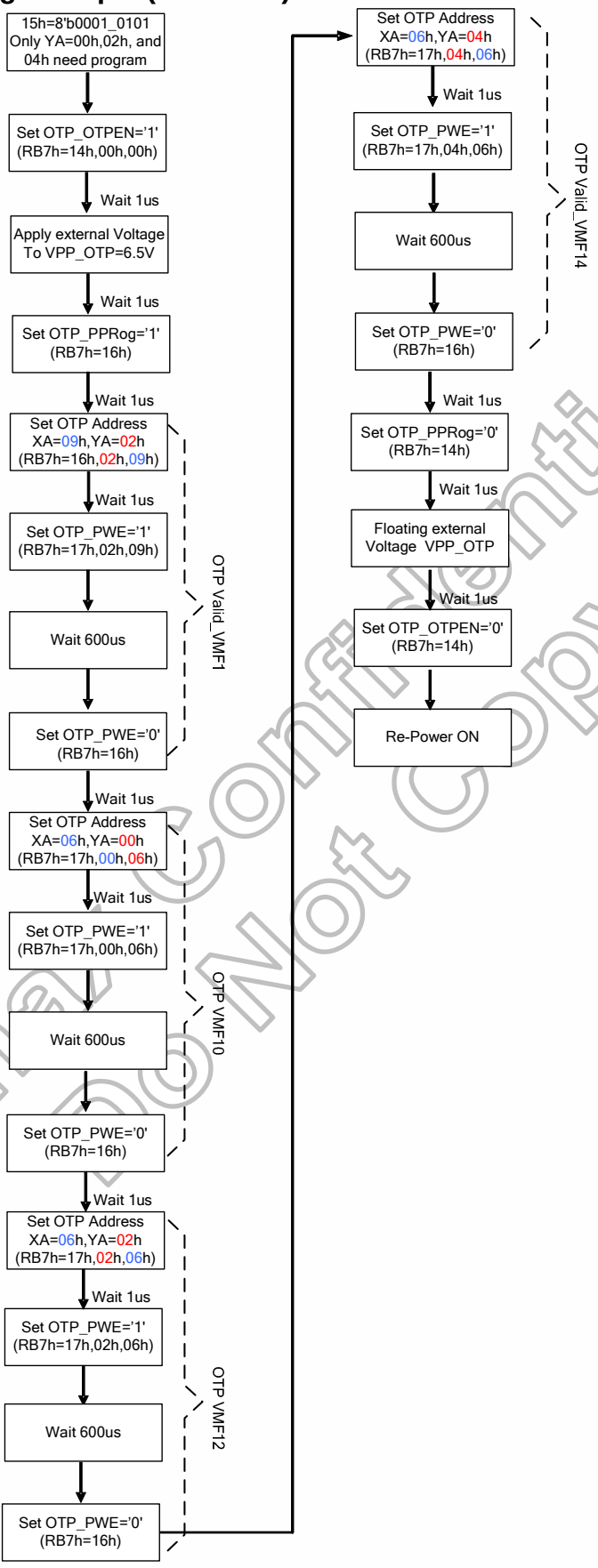
OTP programming example (VMF=15h)



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5.15 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

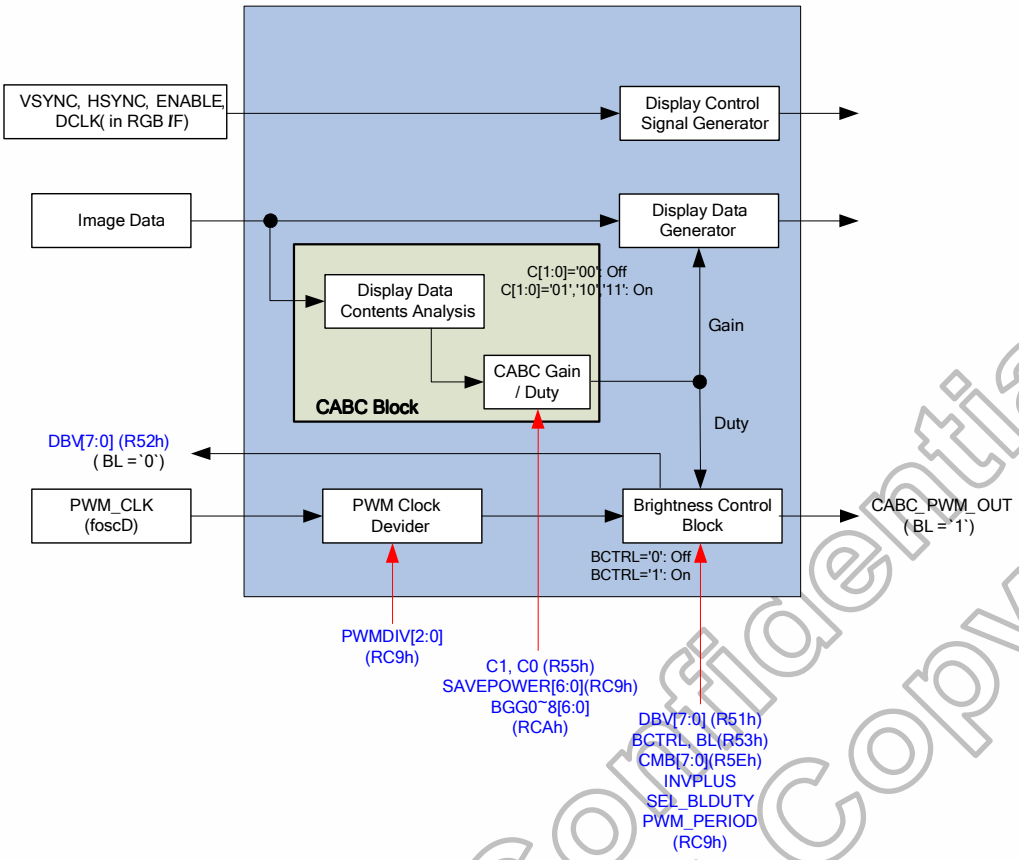

Figure 5-44: CABC block diagram

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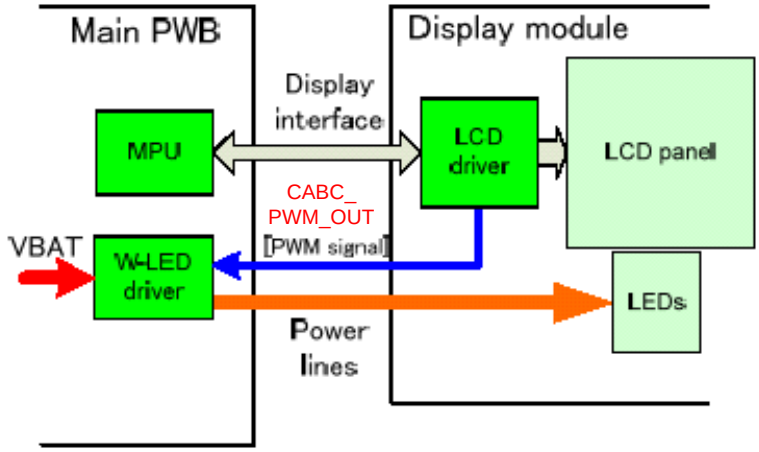
5.15.1 Module architectures

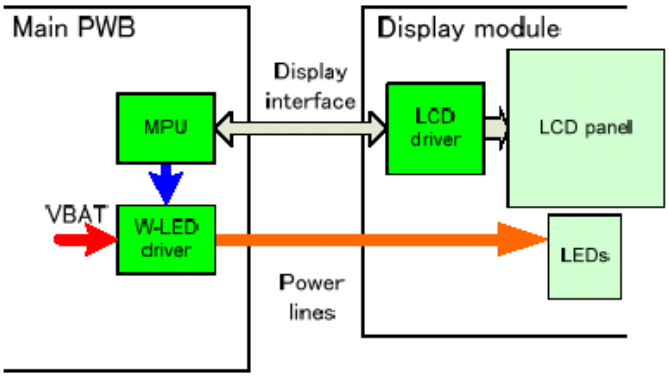
The HX8347-I can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- **Architecture I**



1. **BL** =`1` of R53h
2. LED backlight brightness for the display is controlled by external output "CABC_PWM_OUT".

- **Architecture II**



1. **BL** =`0` of R53h
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R52h.
3. Read commands R52h should be synchronized with V-sync.

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5.15.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness. The CABC_PWM_OUT output active polarity is defined by **INVPULS** bit of RC9h.

The CABC_PWM_OUT output period is controlled by **PWMDIV[2:0]** and **PWM_PERIOD[7:0]** bits of RC9h setting.

Ex: PWM CLK is 5.5MHz (period 180ns), PWMDIV=110(divide by 64),
and PWM_PERIOD=00h (the value is 0+1).
➔ CABC_PWM_OUT period = 180ns x 64 x (1x256) = 2.95 ms

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as DBV[7:0]/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = 228 / 255 x 74% ≡ 66.16%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.95ms, and the low-level of CABC_PWM_OUT = 1.00ms.

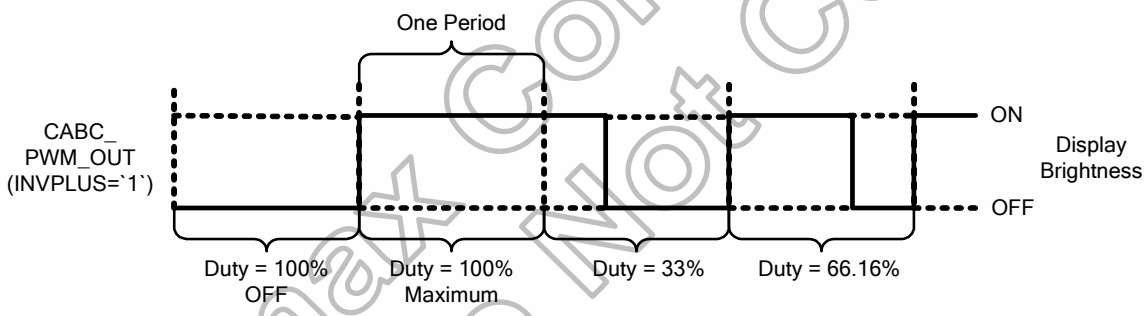

Figure 5-45: CABC_PWM_OUT output duty

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low (**INVPULS='1'**) and the DBV[7:0](R52h) will be read a value as 169_{DEC} (169/255≡ 66.27%).

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5.15.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. "**CMB[7:0],** Read CABC minimum brightness (R5Fh) "always read the setting value of "**CMB[7:0],** Write CABC minimum brightness (R5Eh)".

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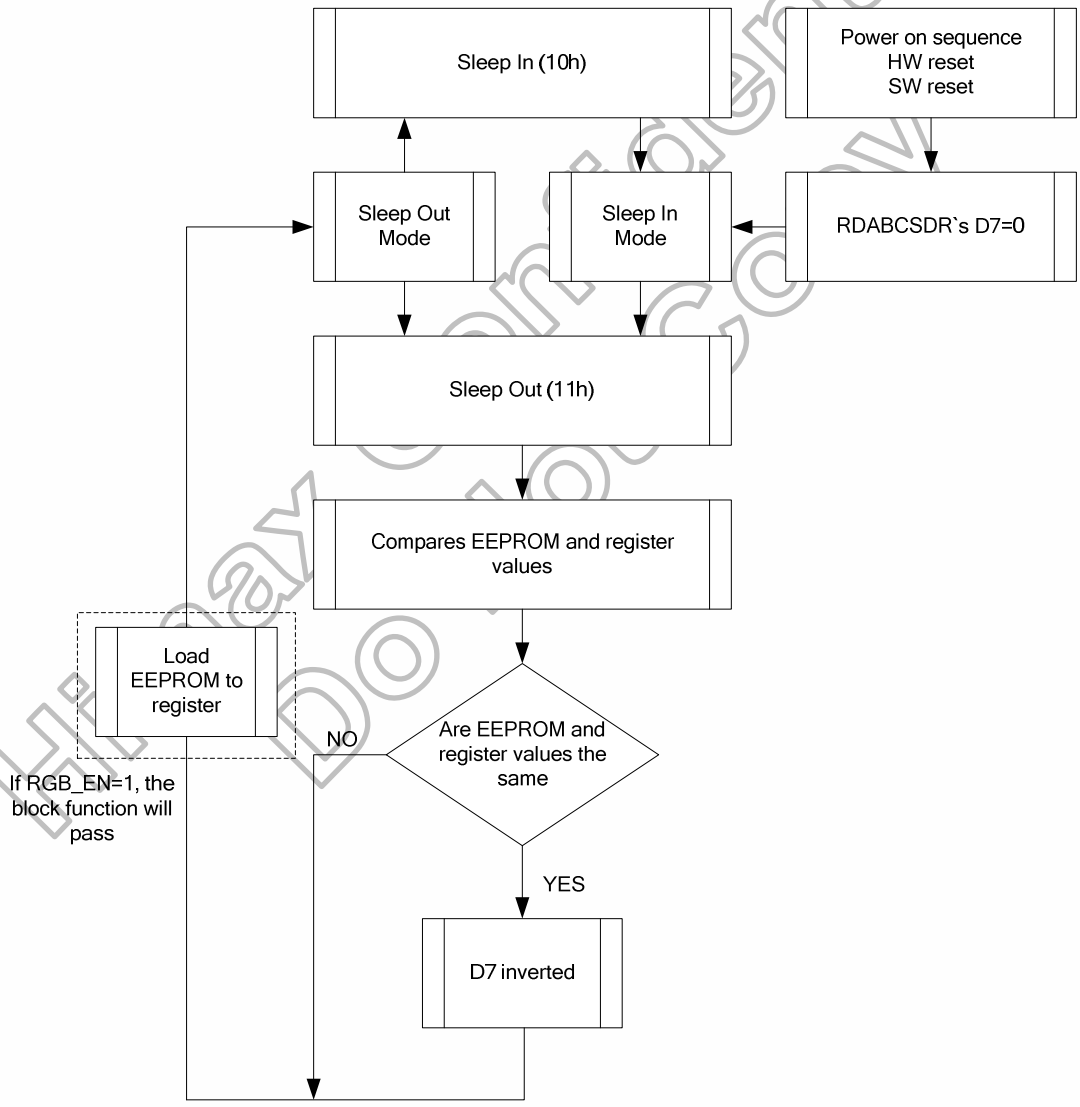
5.15.3.1 Register loading detection

Sleep Out command (See section 6.2.15, Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: compares register and EEPROM values, 2nd step: loads EEPROM values to registers). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.2.46 “Read Automatic Brightness Control Self-Diagnostic Result (68h)” (=RDABCSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).
The flow chart for this internal function is following:



Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module

Figure 5-46: RDABCSDR register loading detection flow

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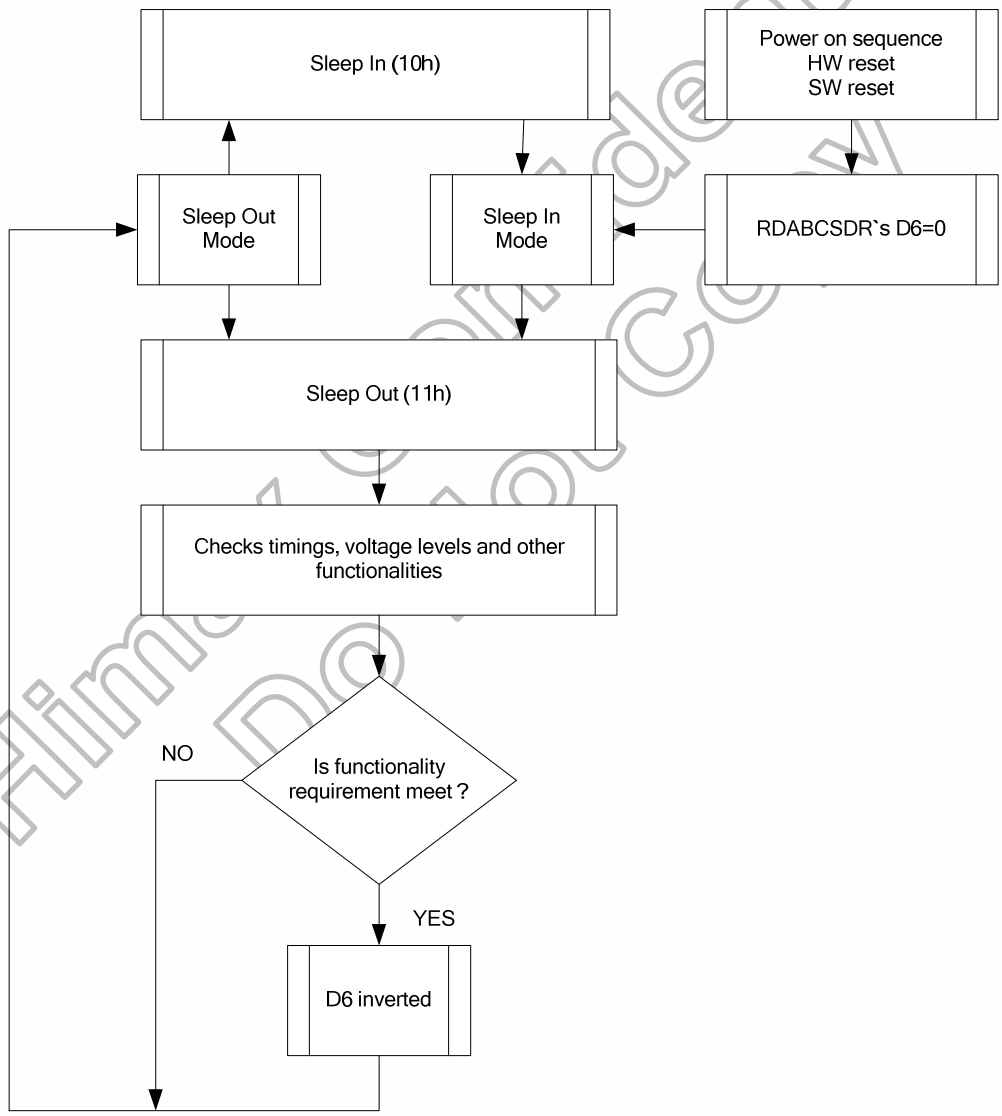
5.15.3.2 Functionality detection

Sleep Out command (See section 6.2.15, Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets Nokia's functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting Nokia's functionality requirements (e.g. booster voltage levels, timings, etc.). If Nokia's functionality requirement is met, there is inverted (increased by 1) a bit, which defined in command 6.2.46 "Read Automatic Brightness Control Self-Diagnostic Result (68h)" (=RDABCSDR) (The used bit of this command is D6). If Nokia's functionality requirement is not same, this bit (D6) is not inverted (=not increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDABCSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5-47: RDABCSDR functionality detection flow

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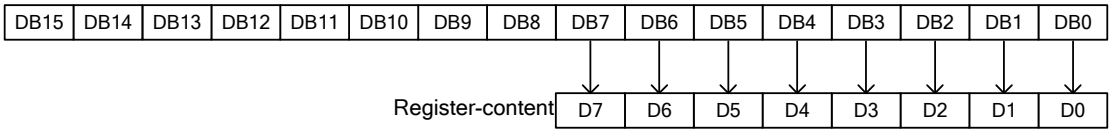
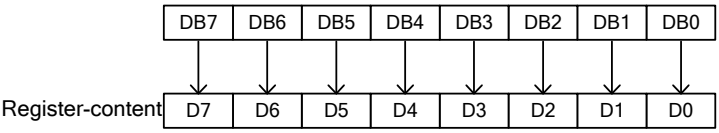
6. GCommand Set

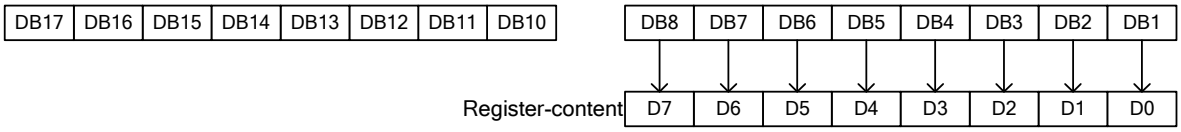
IM3~IM0 = “0001” 8080 MCU 16-bits Parallel type I



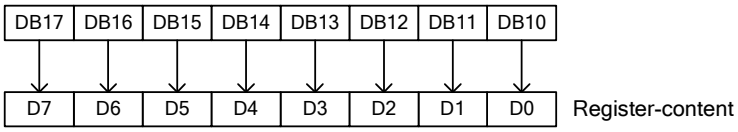
IM3~IM0 = “0000” 8080 MCU 8-bits Parallel type I



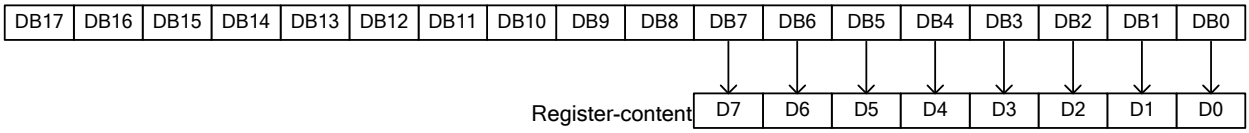
IM3~IM0 = “1000” 8080 MCU 16-bits Parallel type II



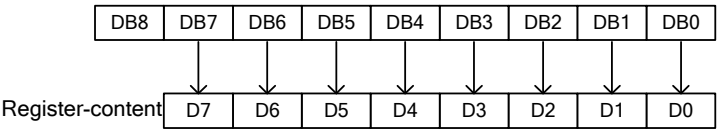
IM3~IM0 = “1001” 8080 MCU 8-bits Parallel type II



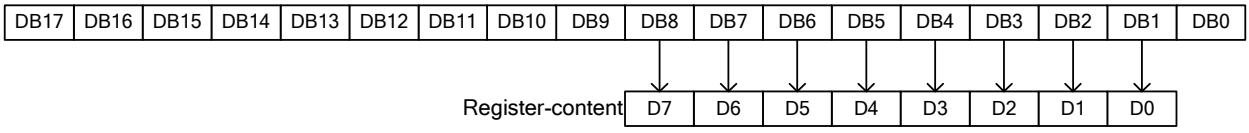
IM3~IM0 = “0011” 8080 MCU 18-bits Parallel type I



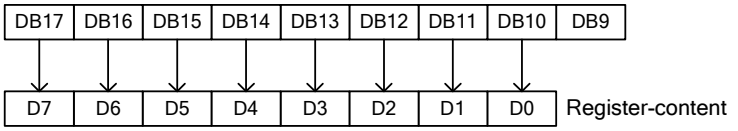
IM3~IM0 = “0010” 8080 MCU 9-bits Parallel type I



IM3~IM0 = “1010” 8080 MCU 18-bits Parallel type II



IM3~IM0 = “1011” 8080 MCU 9-bits Parallel type II



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6.1 Command set list

Normal command set in system interface display mode (RCM[1:0]="0x")

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	0	↑	1	0	0	0	0	0	0	0	0	No Operation
01	SWRESET	0	↑	1	0	0	0	0	0	0	0	1	Software reset
04	RDDIDIF	0	↑	1	0	0	0	0	0	1	0	0	Read Display Identification Information
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID1[7:0]								ID1 read
		1	1	↑	ID2[7:0]								ID2 read
		1	1	↑	ID3[7:0]								ID3 read
09	RDDST	0	↑	1	0	0	0	0	1	0	0	1	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D31	D30	D29	D28	D27	D26	0	0	-
		1	1	↑	0	D22	D21	D20	D19	D18	D17	D16	-
		1	1	↑	D15	0	D13	0	0	D10	D9	D8	-
		1	1	↑	D7	D6	D5	0	0	0	0	0	-
0A	RDDPM	0	↑	1	0	0	0	0	1	0	1	0	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	D3	D2	0	0	-
0B	RDDMADCTL	0	↑	1	0	0	0	0	1	0	1	1	Read Display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	D3	0	0	0	-
0C	RDDCOLMOD	0	↑	1	0	0	0	0	1	1	0	0	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	0	0	0	0	0	D2	D1	D0	-
0D	RDDIM	0	↑	1	0	0	0	0	1	1	0	1	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	0	D5	0	0	D2	D1	D0	-
0E	RDDSM	0	↑	1	0	0	0	0	1	1	1	0	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	0	0	0	0	0	0	-
0F	RDDSDR	0	↑	1	0	0	0	0	1	1	1	1	Read Display Self-Diagnostic Result
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	0	0	0	0	-
10	SLPIN	0	↑	1	0	0	0	1	0	0	0	0	Sleep in and charge-pump off
11	SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	Sleep out and charge-pump on
12	PTLON	0	↑	1	0	0	0	1	0	0	1	0	Partial Mode On
13	NORON	0	↑	1	0	0	0	1	0	0	1	1	Normal Display Mode On

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(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
20	INVOFF	0	↑	1	0	0	1	0	0	0	0	0	Display Inversion Off
21	INVON	0	↑	1	0	0	1	0	0	0	0	1	Display Inversion On
26	GAMSET	0	↑	1	0	0	1	0	0	1	1	0	Gamma Set
		1	↑	1	GC[7:0]								-
28	DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	Display off
29	DISPON	0	↑	1	0	0	1	0	1	0	0	1	Display on
2A	CASET	0	↑	1	0	0	1	0	1	0	1	0	Read Display Status
		1	↑	1	SC[15:8]								Column address start
		1	↑	1	SC[7:0]								Column address start
		1	↑	1	EC[15:8]								Column address end
		1	↑	1	EC[7:0]								Column address end
2B	PASET	0	↑	1	0	0	1	0	1	0	1	1	Row address set
		1	↑	1	SP[15:8]								Row address start
		1	↑	1	SP[7:0]								Row address start
		1	↑	1	EP[15:8]								Row address end
		1	↑	1	EP[7:0]								Row address end
2C	RAMWR	0	↑	1	0	0	1	0	1	1	0	0	Memory write
		1	↑	1	D[15:0]								Write data
2E	RAMRD	0	↑	1	0	0	1	0	1	1	1	0	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D[15:0]								Read data
30	PLTAR	0	↑	1	0	0	1	1	0	0	0	0	Partial start end address set
		1	↑	1	SR[15:8]								Start row
		1	↑	1	SR[7:0]								Start row
		1	↑	1	ER[15:8]								End row
		1	↑	1	ER[7:0]								End row
33	VSCRDEF	0	↑	1	0	0	1	1	0	0	1	1	Vertical Scrolling Definition
		1	↑	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	-
		1	↑	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	-
		1	↑	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	-
		1	↑	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	-
		1	↑	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	-
		1	↑	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	-
34	TEOFF	0	↑	1	0	0	1	1	0	1	0	0	Tear Effect On/Off
35	TEON	0	↑	1	0	0	1	1	0	1	0	1	Tear Effect Mode
		1	↑	1	-	-	-	-	-	-	-	TEMODE	-
36	MADCTL	0	↑	1	0	0	1	1	0	1	1	0	Memory Access Control
		1	↑	1	MY	MX	MV	ML	BGR	0	0	0	-
37	VSCRSADD	0	↑	1	0	0	1	1	0	1	1	1	Vertical Scrolling Start Address
		1	↑	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	-
		1	↑	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	-

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(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
38	IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	Idle Mode off
39	IDMON	0	↑	1	0	0	1	1	1	0	0	1	Idle Mode on
3A	COLMOD	0	↑	1	0	0	1	1	1	0	1	0	Interface pixel format
		1	↑	1	0	0	0	0	0	D2	D1	D0	-
44	TESL	0	1	↑	0	1	0	0	0	1	0	0	TESL
		1	1	↑	TELINE15	TELINE14	TELINE13	TELINE12	TELINE11	TELINE10	TELINE9	TELINE8	-
		1	1	↑	TELINE7	TELINE6	TELINE5	TELINE4	TELINE3	TELINE2	TELINE1	TELINE0	-
51	WRDISBV	0	↑	1	0	1	0	1	0	0	0	1	Write Display Brightness Value
		1	↑	1	DBV[7:0]								-
52	RDDISBV	0	↑	1	0	1	0	1	0	0	1	0	Read Display Brightness Value
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	DBV[7:0]								-
53	WRCTRLD	0	↑	1	0	1	0	1	0	0	1	1	Write Control Display
		1	↑	1	-	-	BCTRL	-	DD	BL	-	-	-
54	RDCTRLD	0	↑	1	0	1	0	1	0	1	0	0	Read Control Display Value
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	-	BCTRL	-	DD	BL	-	-	-
55	WRCABC	0	↑	1	0	1	0	1	0	1	0	1	Write Content Adaptive Brightness Control
		1	↑	1	-	-	-	-	-	-	C1	C0	-
56	RDCABC	0	↑	1	0	1	0	1	0	1	1	0	Read Content Adaptive Brightness Control
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	-	-	-	-	-	C1	C0	-
5E	WRCABCMB	0	↑	1	0	1	0	1	1	1	1	0	Write CABC Minimum Brightness
		1	↑	1	CMB[7:0]								-
5F	RDCABCMB	0	↑	1	0	1	0	1	1	1	1	1	Read CABC Minimum Brightness
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	CMB[7:0]								-

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(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
68	RDABCSDR	0	↑	1	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	0	0	0	0	0	0	
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	module's manufacturer[7:0]								
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	LCD module/driver version [7:0]								
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	LCD module/driver ID[7:0]								

Table 6-1: System interface command set

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Normal Command Set in RGB Interface Display Mode (RCM = '1x')

(Hex)	Operation Code	DNC_SCL	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	0	0	0	0	0	0	0	0	0	No Operation
01	SWRESET	0	0	0	0	0	0	0	0	1	Software reset
04	RDDIDIF	0	0	0	0	0	0	1	0	0	Read Display Identification Information
		Dummy Clock									-
		-	ID1[7:0]								ID1 read
		-	ID2[7:0]								ID2 read
		-	ID3[7:0]								ID3 read
06	RDREAD	0	0	0	0	0	0	1	1	0	Read Red Color
		-	0	0	R[5:0]						-
07	RDGREN	0	0	0	0	0	0	1	1	1	Read Green Color
		-	0	0	G[5:0]						-
08	RDBLUE	0	0	0	0	0	1	0	0	0	Read Blue Color
		-	0	0	B[5:0]						-
09	RDDST	0	0	0	0	0	1	0	0	1	Read Display Status
		Dummy Clock									-
		-	D31	D30	D29	0	0	D26	0	0	-
		-	0	D22	D21	D20	0	0	D17	1	-
		-	0	0	0	0	0	D10	0	D8	-
		-	D7	D6	0	D4	D3	D2	D1	0	-
0A	RDDPM	0	0	0	0	0	1	0	1	0	Read Display Power Mode
		-	D7	0	0	D4	1	D2	0	0	-
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1	Read Display MADCTL
		-	D7	D6	0	0	D3	0	0	0	-
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0	Read Display Pixel Format
		-	0	D6	D5	D4	0	0	0	0	-
0D	RDDIM	0	0	0	0	0	1	1	0	1	Read Display Image Mode
		-	0	0	0	0	0	D2	D1	D0	-
0E	RDDSM	0	0	0	0	0	1	1	1	0	Read Display Signal Mode
		-	0	0	D5	D4	D3	D2	0	0	-
0F	RDDSDR	0	0	0	0	0	1	1	1	1	Read Display Self-Diagnostic Result
		-	D7	D6	D5	D4	0	0	0	0	-
10	SLPIN	0	0	0	0	1	0	0	0	0	Sleep in and charge-pump off
11	SLPOUT	0	0	0	0	1	0	0	0	1	Sleep out and charge-pump on
13	NORON	0	0	0	0	1	0	0	1	1	Normal Display Mode On
26	GAMSET	0	0	0	1	0	0	1	1	0	Gamma Set
		1	GC[7:0]								-
28	DISPOFF	0	0	0	1	0	1	0	0	0	Display off
29	DISPON	0	0	0	1	0	1	0	0	1	Display on

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(Hex)	Operation Code	DNC_SCL	D7	D6	D5	D4	D3	D2	D1	D0	Function
36	MADCTL	0	0	0	1	1	0	1	1	0	Memory Access Control
		0	MY	MX	0	0	BGR	0	-	-	-
3A	COLMOD	0	0	0	1	1	1	0	1	0	Interface Pixel Format
		1	-	CSEL[2:0]			-	-	-	-	-
51	WRDISBV	0	0	1	0	1	0	0	0	1	Write Display Brightness Value
		1	DBV[7:0]								-
52	RDDISBV	0	0	1	0	1	0	0	1	0	Read Display Brightness Value
		-	DBV[7:0]								-
53	WRCTRLD	0	0	1	0	1	0	0	1	1	Write Control Display
		1	-	-	BCTRL	-	DD	BL	-	-	-
54	RDCTRLD	0	0	1	0	1	0	1	0	0	Read Control Display Value
		-	-	-	BCTRL	-	DD	BL	-	-	-
55	WRCABC	0	0	1	0	1	0	1	0	1	Write Content Adaptive Brightness Control
		1	-	-	-	-	-	-	C1	C0	-
56	RDCABC	0	0	1	0	1	0	1	1	0	Read Content Adaptive Brightness Control
		-	-	-	-	-	-	-	C1	C0	-
5E	WRCABCMB	0	0	1	0	1	1	1	1	0	Write CABC Minimum Brightness
		1	CMB[7:0]								-
5F	RDCABCMB	0	0	1	0	1	1	1	1	1	Read CABC Minimum Brightness
		-	CMB[7:0]								-
68	RDABCSDR	0	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result
		-	D1	D0	0	0	0	0	0	0	-
DA	RD1D1	0	1	1	0	1	1	0	1	0	Read ID1
		1	module's manufacturer[7:0]								-
DB	RDID2	0	1	1	0	1	1	0	1	1	Read ID2
		1	LCD module/driver version [7:0]								-
DC	RDID3	0	1	1	0	1	1	1	0	0	Read ID3
		1	LCD module/driver ID[7:0]								-

Table 6-2: RGB interface command set

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Extended command set

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
B0	SETOSC	0	↑	1	-	1	0	1	1	0	0	0	0	Set Internal Oscillator
		1	↑	1	-	I/P UADJ[3:0] (0011)				N/P UADJ[3:0] (0100)				
		1	↑	1	-	-	-	-	-	-	-	-	OSC_EN (0)	
B1	SETPWCTR	0	↑	1	-	1	0	1	1	0	0	0	1	Set power control
		1	↑	1	-	-	-	-	-	-	-	-	DP_STB (0)	
		1	↑	1	-	-	-	-	-	-	BT[2:0](001)			
		1	↑	1	-	-	-	VRH[5:0](01_1011)						
		1	↑	1	-	-	-	-	-	-	AP[2:0](011)			
		1	↑	1	-	-	I /IP_FS0[2:0](100)			-	N/P_FS0[2:0](100)			
		1	↑	1	-	-	I/IP_FS1[2:0](100)			-	N/P_FS1[2:0](100)			
		1	↑	1	-	GASEN(1)	VCOMGG (0)	-	PON(0)	DK(1)	-	-	STB (1)	
B2	SETDISPLAY	0	↑	1	-	1	0	1	1	0	0	1	0	Set Display control
		1	↑	1	-	-	-	-	-	ISC[3:0] (0011)				
		1	↑	1	-	PT[1:0] (10)		PTV[1:0] (10)		-	-	PTG (1)	REF (1)	
						NL[5:0] (100111)								
						SCN[6:0] (0000000)								
		1	↑	1	-	-	-	GON (1)	DTE (0)	D[1:0] (00)		-	-	
B3	SETRGB	0	↑	1	-	1	0	1	1	0	0	1	1	Set RGB I/F
		1	↑	1	-	-	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	
		1	↑	1	-	-	-	-	-	-	-	RCM[1:0] (00)		
		1	↑	1	-	HBP[7:0](0000_1000)								
		1	↑	1	-	HBP[9:8]		VBP[5:0](00_0100)						
B4	SETCYC	0	↑	1	-	1	0	1	1	0	1	0	0	Set Display cycle
		1	↑	1	-	-	I/IP_NW[2:0] (001)			-	N/P_NW[2:0] (001)			
		1	↑	1	-	I/IP_RTN[3:0](1000)				N/P_RTN[3:0](1000)				
		1	↑	1	-	-	-	IP_DIV[1:0] (00)		-	-	NP_DIV[1:0] (00)		
		1	↑	1	-	N/P_DUM[7:0](0011_0010)								
		1	↑	1	-	I/IP_DUM[7:0](0011_0010)								
		1	↑	1	-	GDON[7:0] (0000_1101)								
		1	↑	1	-	GDOF[7:0] (0111_1000)								
B6	SETVCOM	0	↑	1	-	1	0	1	1	0	1	1	0	Set VCOM voltage
		1	↑	1	-	VMH[7:0](0010_1111)								
		1	↑	1	-	VML[7:0](0101_0111)								
B7	SETEFUSE	0	↑	1	-	-	-		1	0	1	1	1	SET OTP
		1	↑	1	-	PTM[1:0]		VARDJ[1:0]		POR	OPTEN	PPRO	PWE	
		1	↑	1	-	-	-	-	-	-	OTP_YA[2:0]			
		1	↑	1	-	-	-	-	OTP_XA[4:0]					
		1	↑	1	-	OTPDATA[7:0]								
B9	SETEXTC	0	↑	1	-	1	0	1	1	1	0	0	1	Enter extention command
		1	↑	1	-	1	1	1	1	1	1	1	1	
		1	↑	1	-	1	0	0	0	0	0	1	1	
		1	↑	1	-	0	1	0	0	0	1	1	1	

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(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
C9	SETCABC	0	↑	1	--	1	1	0	0	1	0	0	1	SET CABC
		1	↑	1	--	BC_CTL	PWMDIV[2:0](100)			SEL_GAIN[1:0](11)		INVPULS(1)	SEL_BLDUTY(1)	
		1	↑	1	--	PWM_PERIOD[7:0](0010_0011)								
CC	SETPANEL	0	↑	1	--	1	1	0	0	1	1	0	0	Set Panel characteristics
		1	↑	1	--	--	--	--	--	SS_PANEL(0)	GS_PANEL(0)	REV_PANEL(0)	BGR_PANEL(0)	
E0	SETGAMMA	0	↑	1	-	1	0	1	1	1	0	1	1	Set Gamma
		1	↑	1	-	-	-	VRP0[5:0]						
		1	↑	1	-	-	-	VRP1[5:0]						
		1	↑	1	-	-	-	VRP2[5:0]						
		1	↑	1	-	-	-	VRP3[5:0]						
		1	↑	1	-	-	-	VRP4[5:0]						
		1	↑	1	-	-	-	VRP5[5:0]						
		1	↑	1	-	-	PRP0[6:0]							
		1	↑	1	-	-	PRP1[6:0]							
		1	↑	1	-	-	-	-	PKP0[4:0]					
		1	↑	1	-	-	-	-	PKP1[4:0]					
		1	↑	1	-	-	-	-	PKP2[4:0]					
		1	↑	1	-	-	-	-	PKP3[4:0]					
		1	↑	1	-	-	-	-	PKP4[4:0]					
		1	↑	1	-	-	-	-	VRN0[5:0]					
		1	↑	1	-	-	-	-	VRN1[5:0]					
		1	↑	1	-	-	-	-	VRN2[5:0]					
		1	↑	1	-	-	-	-	VRN3[5:0]					
		1	↑	1	-	-	-	-	VRN4[5:0]					
		1	↑	1	-	-	-	-	VRN5[5:0]					
		1	↑	1	-	-	PRN0[6:0]							
		1	↑	1	-	-	PRN1[6:0]							
		1	↑	1	-	-	-	-	PKN0[4:0]					
		1	↑	1	-	-	-	-	PKN1[4:0]					
		1	↑	1	-	-	-	-	PKN2[4:0]					
		1	↑	1	-	-	-	-	PKN3[4:0]					
		1	↑	1	-	-	-	-	PKN4[4:0]					
		1	↑	1	-	CGMN1[1:0]		CGMN0[1:0]		CGMP1[1:0]		CGMP0[1:0]		

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(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
E5	SETCE	0	↑	1	-	1	1	1	0	0	1	0	1	Set Color Enhancement
		1	↑	1	-	-								
		1	↑	1	-				-					
		1	↑	1	-				-					
		1	↑	1	-				-					
		1	↑	1	-				-					
		1	↑	1	-				-					
		1	↑	1	-								CE_EN	
FD	SETVMF	0	↑	1	-	1	1	1	1	1	1	0	1	SetVMF
		1	↑	1	VMF[7:0]									
		1	↑	1							VCOM_OTP_TIMES[2:0]			

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6.2 Command description

6.2.1 NOP

<table>
<tr><td>00 H</td><td colspan="13">NOP (No Operation)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR (Memory Write) or RAMRD (Memory Read) command.</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">-</td></tr>
</table>

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6.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. Note: The GRAM contents are unaffected by this command.												
Restriction	It will be necessary to wait 5m sec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.												

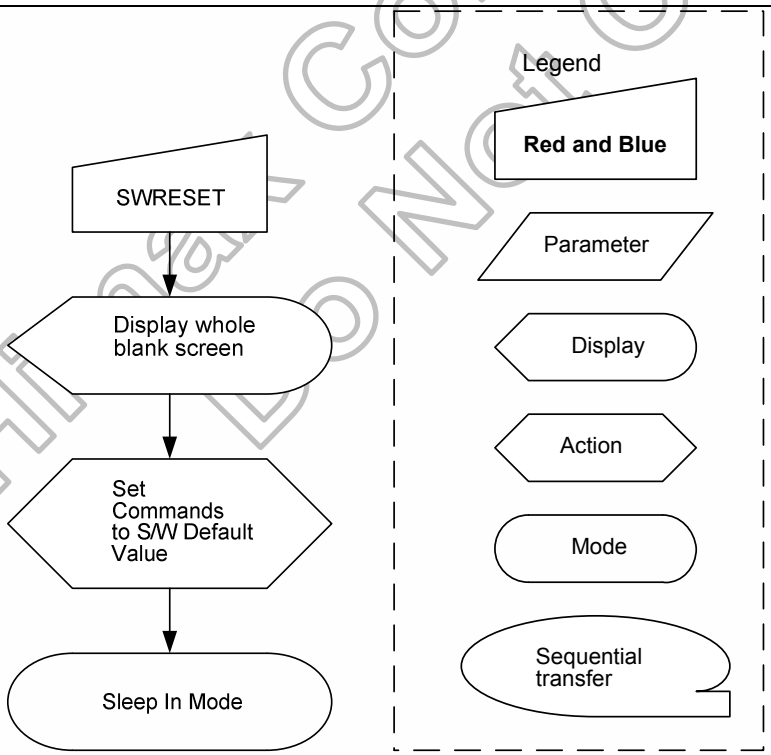
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



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6.2.3 Read display identification information (04h)

04 H	RDDIDIF (Read Display Identification Information)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	This read byte returns 24-bit display identification information. The 1st parameter is dummy data. The 2nd parameter: LCD module's manufacturer ID. The 3rd parameter: LCD module/driver version ID. The 4th parameter: LCD module/driver ID. **Note:** Commands RDID1/2/3(DAh, DBh and DCh) read data correspond to the parameters 2, 3, 4 of the command 04h, respectively.												
Restriction													

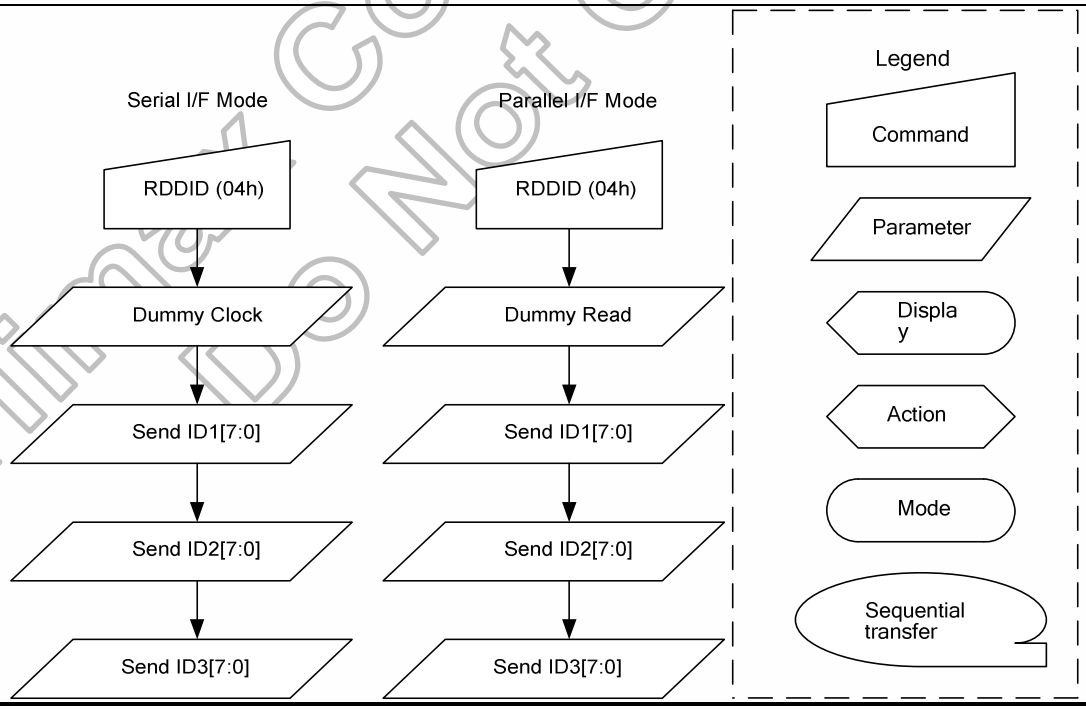
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	TBD
S/W Reset	TBD
H/W Reset	TBD

Flow Chart



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6.2.4 Read red color (06h)

06 H	RDRED (Read Red Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	1	0	06
1st parameter	1	1	↑	-	-	-	R5	R4	R3	R2	R1	R0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: R5 is MSB and R1 is LSB. R0 is set to '0'. 18 bit format: R5 is MSB and R0 is LSB. See: 5.2.2 One Pixel Display Data Memory.												
Restriction	RCM [1:0]= "0X"(RGB I/F disable), this command is working as a NOP (00h) command.												

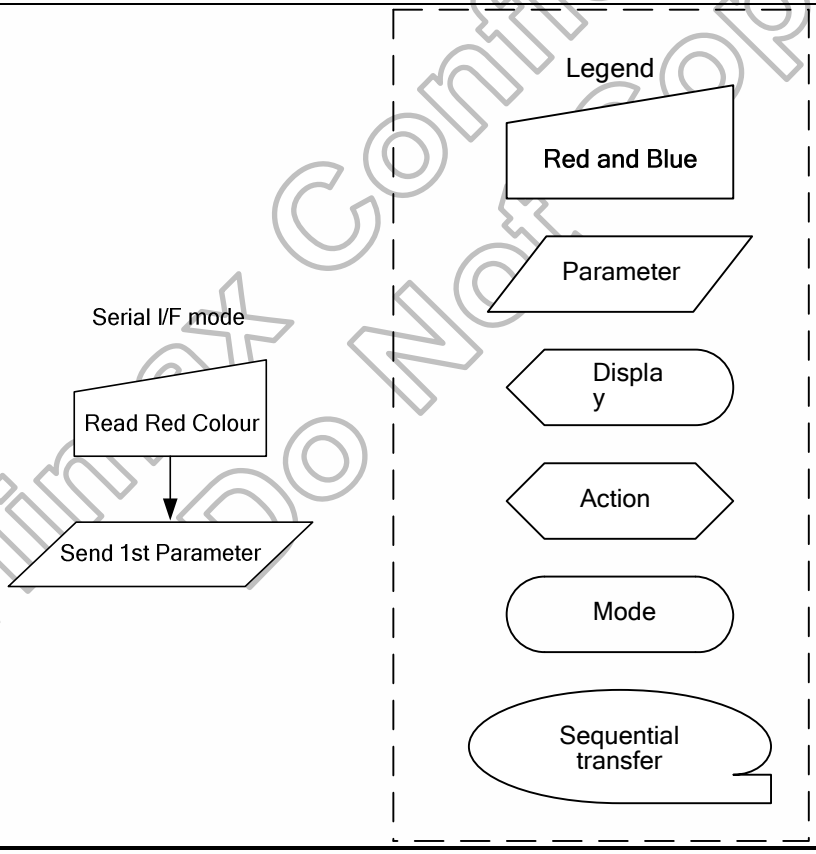
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.5 Read green color (07h)

07 H	RDGREEN (Read Green Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	1	1	07
1st parameter	1	1	↑	-	-	-	G5	G4	G3	G2	G1	G0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16, 18 bit formats: G5 is MSB and G0 is LSB. See: 5.2.2 One Pixel Display Data Memory.												
Restriction	RCM [1:0]= “0X”(RGB I/F disable), this command is working as a NOP (00h) command.												

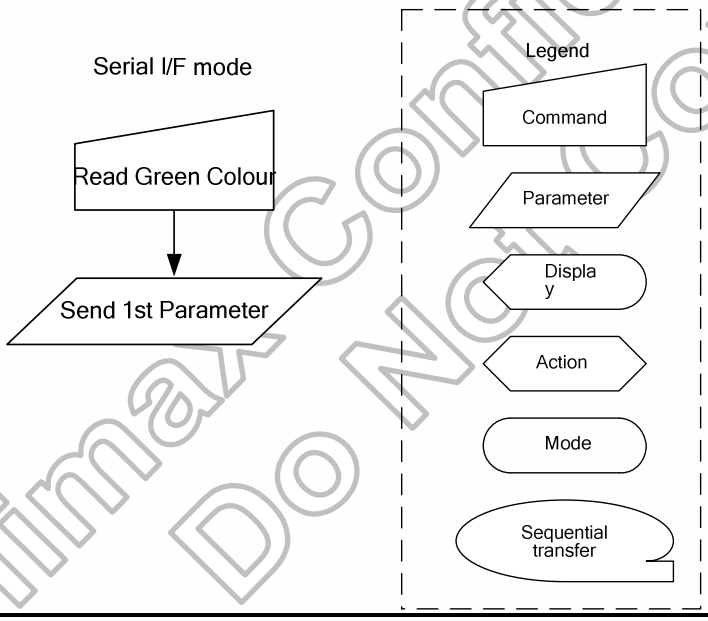
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.6 Read blue color (08h)

08 H	RDBLUE (Read Blue Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	0	08
1st parameter	1	1	↑	-	-	-	B5	B4	B3	B2	B1	B0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: B5 is MSB and B1 is LSB. B0 is set to '0'. 18 bit format: B5 is MSB and B0 is LSB. See: 5.2.2 One Pixel Display Data Memory.												
Restriction	RCM [1:0]= "0X"(RGB I/F disable), this command is working as a NOP (00h) command.												

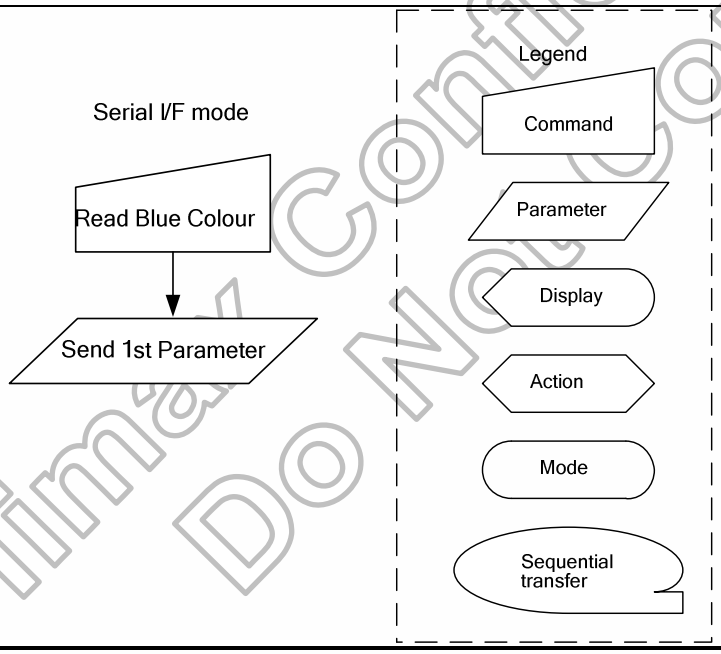
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.7 Read display status (09h)

09 H	RDDST (Read Display Status)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	1	09
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D31	D30	D29	D28	D27	D26	0	0	-
3rd parameter	1	1	↑	-	0	D22	D21	D20	D19	D18	D17	D16	-
4th parameter	1	1	↑	-	D15	0	D13	0	0	D10	D9	D8	-
5th parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D31	Booster Voltage Status	-
D30	Page Address Order (MY)	-
D29	Column Address Order (MX)	-
D28	Page/Column Order (MV)	-
D27	Line Address Order (ML)	-
D26	RGB/BGR Order	-
D25	Display Data Latch Order	Set to '0'
D24	Switching between Segment outputs and RAM	Set to '0'
D23	Switching between Common outputs and RAM	Set to '0'
D22	Interface Color Pixel Format Definition	-
D21		-
D20		-
D19	Idle Mode On/Off	-
D18	Partial Mode On/Off	-
D17	Sleep In/Out	-
D16	Display Normal Mode On/Off	-
D15	Vertical Scrolling Status	-
D14	Horizontal Scrolling Status	Set to '0'
D13	Inversion Status	-
D12	All Pixels On	Set to '0'
D11	All Pixels Off	Set to '0'
D10	Display On/Off	-
D9	Tearing Effect Line On/Off	-
D8	Gamma Curve Selection	-
D7		-
D6		-
D5	Tearing Effect Output Line Mode	-
D4	Horizontal Sync. (HS, RGB I/F)	-
D3	Vertical Sync. (VS,RGB I/F)	-
D2	Pixel Clock (DOTCLK,RGB I/F))	-
D1	Data Enable (DE,RGB I/F)	-
D0		Set to '0'

Bit Values are explained overleaf.

Bit D31 – Booster Voltage Status

'0' = Booster Off or has a fault.

'1' = Booster On and working OK.

Bit D30 – Page Address Order

'0' = Top to Bottom (When MADCTL B7(MY) = '0').

'1' = Bottom to Top (When MADCTL B7(MY) ='1').

Bit D29 – Column Address Order

'0' = Left to Right (When MADCTL B6(MX) = '0').

'1' = Right to Left (When MADCTL B6(MX) = '1').

Bit D28 –Page / Column Order

'0' = Normal Mode (When MADCTL B5(MV) = '0').

'1' = Reverse Mode (When MADCTL B5(MV) = '1').

Bit D27 – Line Address Order

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'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').

Bit D26 – RGB/BGR Order

'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').

Note : For bits D27 and D26 also refer to 8.2.32 Memory Access Control (R36h)

Bit D25 – Display Data Latch Order

This bit is not applicable for this project, so it is set to '0'.

Bit D24 – Switching Between Segment Outputs and RAM

This bit is not applicable for this project, so it is set to '0'.

Bit D23 – Switching Between Common Outputs and RAM

This bit is not applicable for this project, so it is set to '0'.

Bits D22, D21, D20 –Interface Color Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 bit/pixel	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Bit D19 – Idle Mode On/Off

'0' = Idle Mode Off.
'1' = Idle Mode On.

Bit D18 – Partial Mode On/Off

'0' = Partial Mode Off.
'1' = Partial Mode On.

Bit D17 – Sleep In/Out

'0' = Sleep In Mode.
'1' = Sleep Out Mode.

Bit D16 – Display Normal Mode On/Off

'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.

Bit D15 – Vertical Scrolling On/Off

'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.

Bit D14 – Horizontal Scrolling Status

This bit is not applicable for this project, so it is set to '0'.

Bit D13 – Inversion On/Off

'0' = Inversion is Off.
'1' = Inversion is On.

Bit D12 – All Pixels On

This bit is not applicable for this project, so it is set to '0'.

Bit D11 – All Pixels Off

This bit is not applicable for this project, so it is set to '0'.

Bit D10 – Display On/Off

'0' = Display is Off.
'1' = Display is On.

Bit D9 – Tearing Effect Line On/Off

'0' =Tearing Effect Line Off.
'1' = Tearing Effect On.

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Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0 (Gamma 2.2)
Gamma Curve 2	0	0	1	GC1 (Gamma 1.8)
Gamma Curve 3	0	1	0	GC2 (Gamma 2.5)
Gamma Curve 4	0	1	1	GC3 (Gamma 1)
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Bit D5 – Tearing Effect Line Output Mode.
'0' = Mode 1, V-Blanking only.
'1' = Mode 2, both H-Blanking and V-Blanking.
Bit D4 – Horizontal Sync. (HS) RGB I/F On/Off, Note
'0' = Horizontal Sync. line is Off ("Low").
'1' = Horizontal Sync. line is On ("High").
Bit D3 – Vertical Sync. (VS) RGB I/F On/Off, Note
'0' = Vertical Sync. line is Off ("Low").
'1' = Vertical Sync. line is On ("High").
Bit D2 – Pixel Clock (DOTCLK) RGB I/F On/Off, Note
'0' = DCK line is Off ("Low").
'1' = DCK line is On ("High").
Bit D1 – Data Enable (DE) RGB I/F On/Off, Note
'0' = ENABLE line is Off ("Low").
'1' = ENABLE line is On ("High").
Bit D0 – Parity Error
This bit is not applicable for this project, so it is set to '0'
Note: This bit indicates current status of the line when this command has been sent.

Restriction

RCM [1:0]= "0X"(RGB I/F disable) , D4,D3,D2,D1 bit = '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00000000, 01100001, 00000000, 00000000
S/W Reset	0xxxxx00, 0xxx0001, 00000000, 00000000
H/W Reset	00000000, 01100001, 00000000, 00000000

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6.2.8 Read display power mode (0Ah)

0A H	RDDPM (Read Display Power Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Booster Voltage Status	-
D6	Idle Mode On/Off	-
D5	Partial Mode On/Off	-
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	-
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status
'0' = Booster Off or has a fault.
'1' = Booster On and working OK (Meets display supplier's optical requirements).
Bit D6 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D5 – Partial Display Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D3 – Normal Display Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D1 – Not Defined
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Not Defined
This bit is not applicable for this project, so it is set to '0'.

Restrictions

RCM [1:0]= "1X"(RGB I/F enable) , D5,D6 bit = '0', D3='1'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

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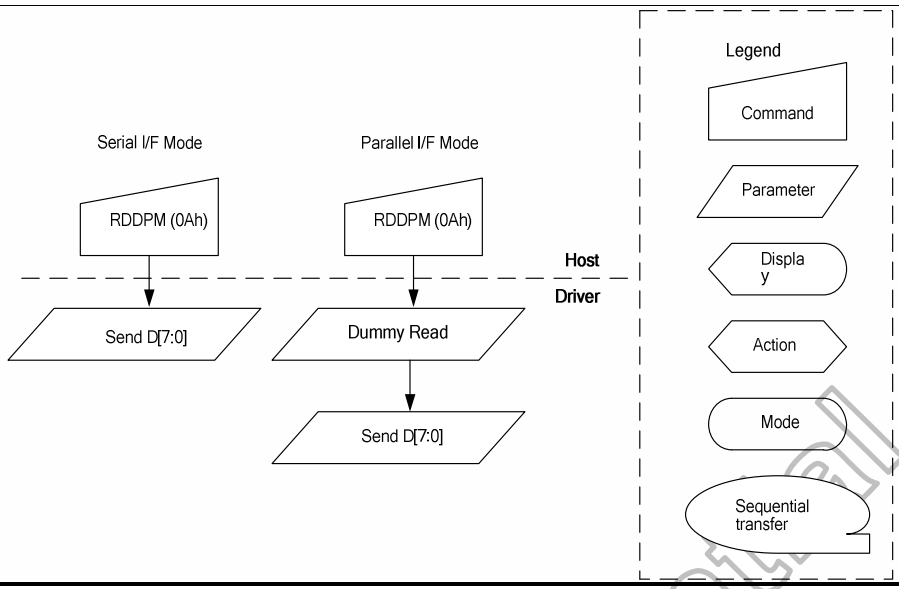
Flow Chart



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6.2.9 Read display MADCTL (0Bh)

0B H	RDDMADCTL (Read Display MADCTL)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	Set to '0'
D1	Switching between Segment outputs and RAM	Set to '0'
D0	Switching between Common outputs and RAM	Set to '0'

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7(MY) = '0').
'1' = Bottom to Top (When MADCTL B7(MY) ='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6(MX) = '0').
'1' = Right to Left (When MADCTL B6(MX) = '1').
Bit D5 –Page / Column Order
'0' = Normal Mode (When MADCTL B5(MV) = '0').
'1' = Reverse Mode (When MADCTL B5(MV) = '1').
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').
Note: For bits D4, D3 and D2 also refer to 8.2.32 Memory Access Control (R36h)
Bit D2 – Display Data Latch Order
This bit is not applicable for this project, so it is set to '0'.
Bit D1 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Switching Between Common Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.

Restrictions

RCM [1:0]= "1X"(RGB I/F enable) , D2,D4,D5, bit = '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

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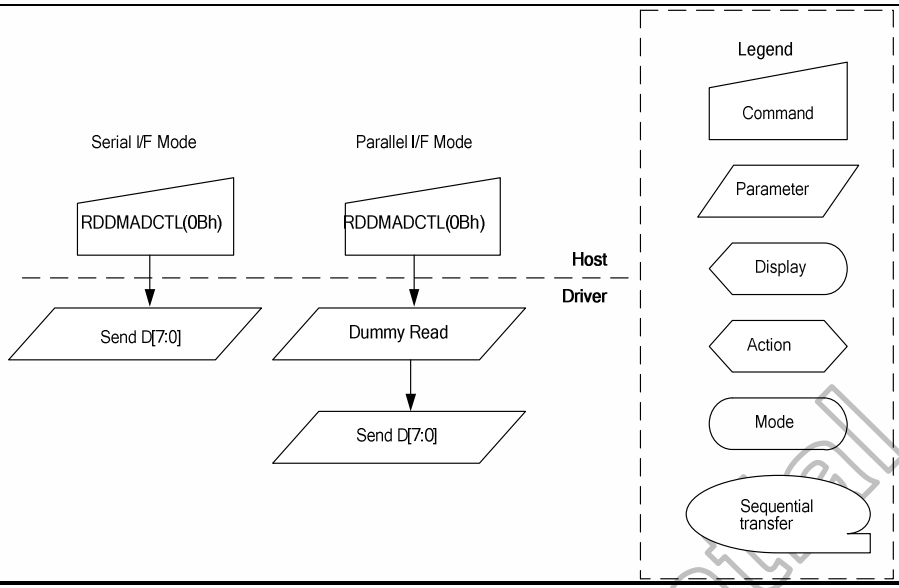
Flow Chart



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6.2.10 Read display pixel format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	RGB Interface Color Format	Set to '0'
D6		-
D5		-
D4		-
D3	System Interface Color Format	Set to '0'
D2		-
D1		-
D0		-

Bit D7 – RGB Interface Color Format Selection

This bit is not applicable for this project, so it is set to '0'.

Bits D6, D5, D4 – RGB Interface Color Pixel Format Definition

See section"8.2.36 Interface Pixel Format (R3Ah)".

RGB Interface Format	D6	D5	D4
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Bit D3 – System Interface Color Format Selection

This bit is not applicable for this project, so it is set to '0'.

Bit D2, D1, D0 – Control Interface Color Pixel Format Definition.

See section"8.2.36 Interface Pixel Format (R3Ah)".

System Interface Color Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Restrictions

RCM [1:0]= "0X"(RGB I/F disable) , D6,D5,D4bit = '0'.
RCM [1:0]= "1X"(RGB I/F enable) , D2,D1, D0 bit = '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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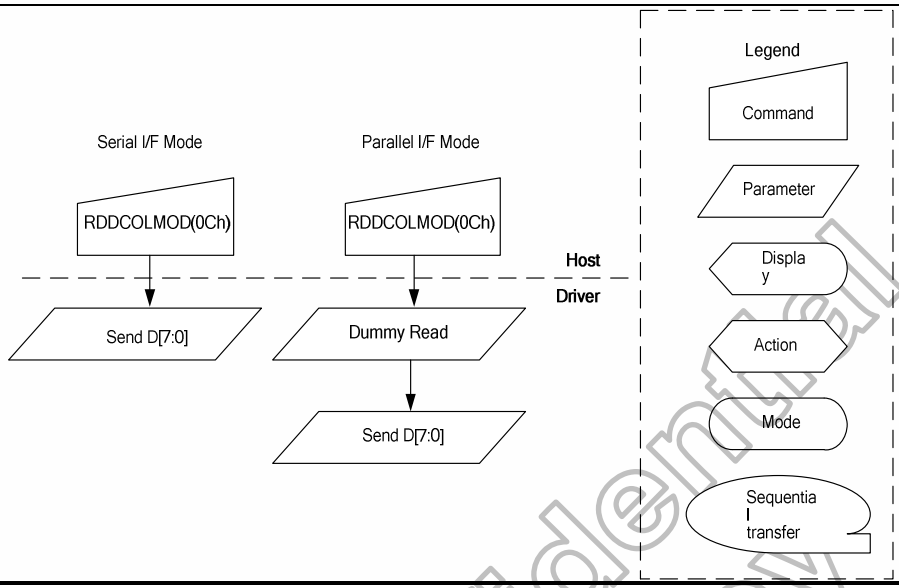
Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	No Change
H/W Reset	18-bit/pixel

Flow Chart



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6.2.11 Read display image mode (0Dh)

0D H	RDDIM (Read Display Image Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 – Vertical Scrolling On/Off

'0' = Vertical Scrolling is Off.

'1' = Vertical Scrolling is On.

Bit D6 – Horizontal Scrolling Status

This bit is not applicable for this project, so it is set to '0'

Bit D5 – Inversion On/Off

'0' = Inversion is Off.

'1' = Inversion is On.

This bit is not applicable for this project, so it is set to '0'

Bit D4 – All Pixels On

This bit is not applicable for this project, so it is set to '0'

Bit D3 – All Pixels Off

This bit is not applicable for this project, so it is set to '0'

Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (R26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

RCM [1:0]= "1X"(RGB I/F enable) , D5,D7bit = '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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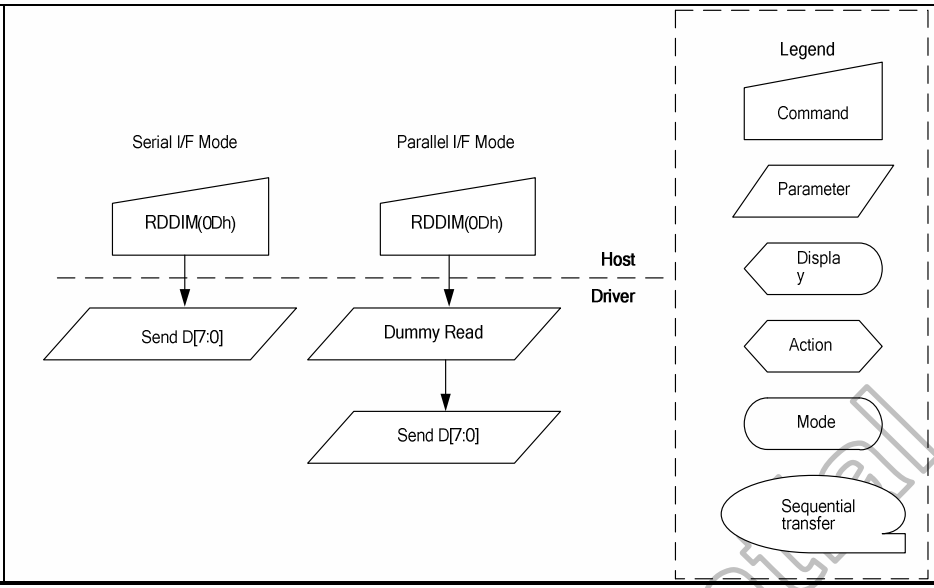
Flow Chart	

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6.2.12 Read display signal mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 – Tearing Effect Line On/Off
'0' = Tearing Effect Line Off.
'1' = Tearing Effect On.

Bit D6 – Tearing Effect Line Output Mode, see section 7.3 for mode definitions.
'0' = Mode 1.
'1' = Mode 2.

Bit D5 – Horizontal Sync. (VSYNC, RGB I/F) On/Off
'0' = Horizontal Sync Bit / Line Off ("Low").
'1' = Horizontal Sync Bit / Line On. ("High").

Bit D4 – Vertical Sync. (HSYNC, RGB I/F) On/Off
'0' = Vertical Sync Bit / Line Off ("Low").
'1' = Vertical Sync Bit / Line On ("High").

Bit D3 – Pixel Clock (DCLK, RGB I/F) On/Off
'0' = Vertical Sync Bit / Line Off ("Low").
'1' = Vertical Sync Bit / Line On ("High").

Bit D2 – Data Enable (ENABLE, RGB I/F)) On/Off
'0' = Vertical Sync Bit / Line Off ("Low").
'1' = Vertical Sync Bit / Line On ("High").

D1 are D0 - are for future use and are set to '0'.

Restrictions

RCM [1:0]= "0X"(RGB I/F disable), D2,D3,D4,D5 bit = '0'.
RCM [1:0]= "1X"(RGB I/F enable), D6,D7bit = '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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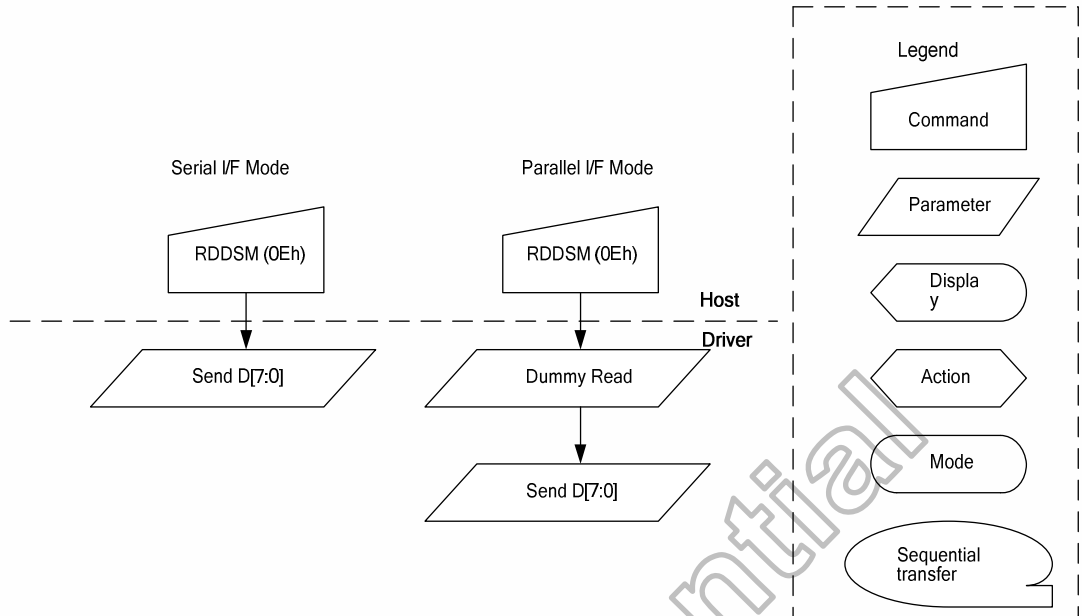
Flow Chart



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6.2.13 Read display self-diagnostic result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	0	0	0	0	-

Description

This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below:

Bit D7 – Register Loading Detection
See section 5.13.1.

Bit D6 – Functionality Detection
See section 5.13.1.

Bit D5 – Chip Attachment Detection
Set bit D5 to '0', if this function is not implemented.

Bit D4 – Display Glass Break Detection
Set bit D4 to '0', if this function is not implemented.

Bits D3, D2, D1 and D0 are for future use and are set to '0'.

Restrictions

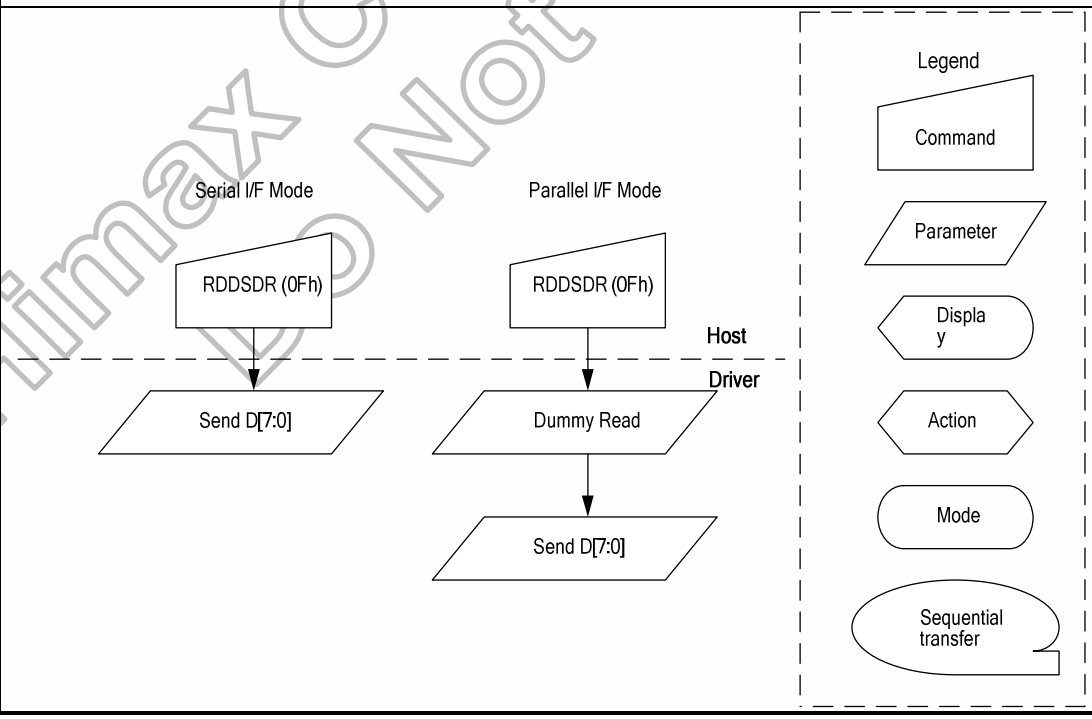
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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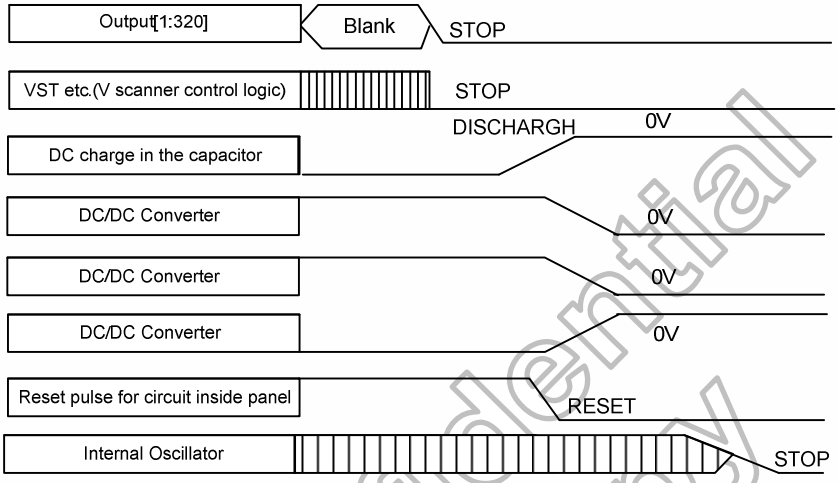
6.2.14 Sleep in (10h)

10 H	SLPIN (Sleep In)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

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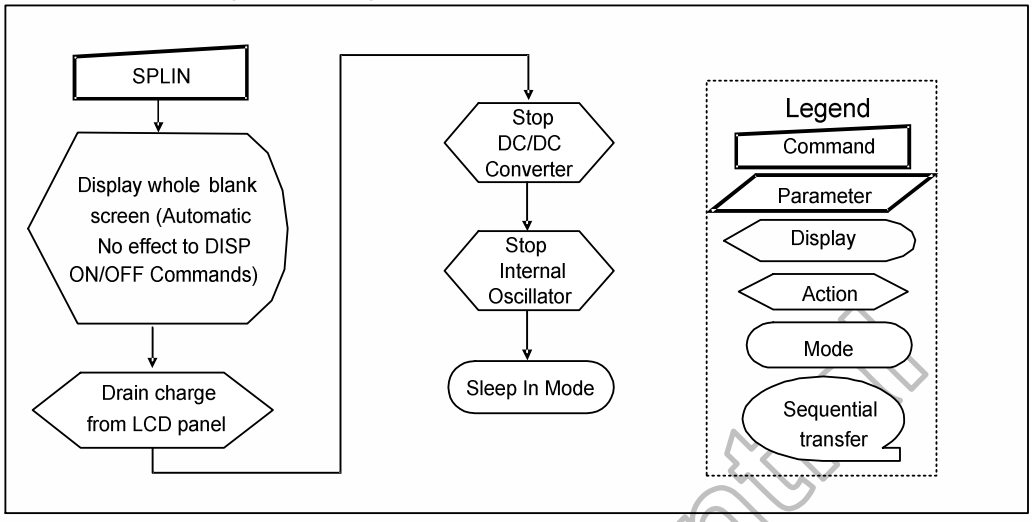
Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



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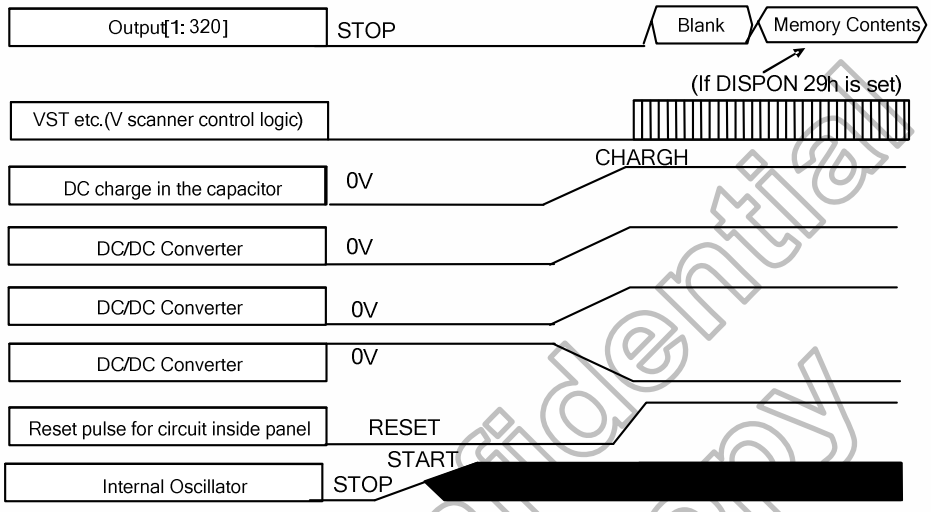
6.2.15 Sleep out (11h)

11 H	SLPOUT (Sleep Out)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

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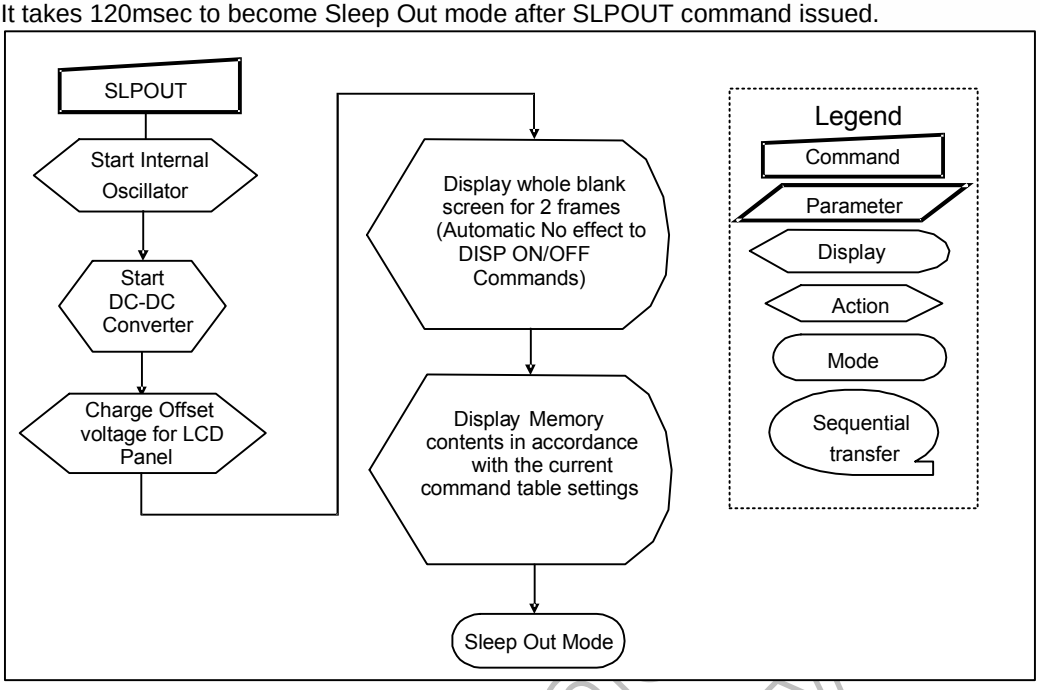
Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



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6.2.16 Partial mode on (12h)

<table>
<tr><td>12 H</td><td colspan="13">PTLON (Partial Mode On)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
See also section 6.3.1</td></tr>
<tr><td>Restrictions</td><td colspan="13">1. RCM [1:0]= “1X” (RGB I/F enable), this command is working as a NOP (00h) command.
2. This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

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6.2.17 Normal display mode on (13h)

13 H	NORON (Normal Display Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. See also section 6.2.1.												
Restriction	1. RCM [1:0]= “1X”(RGB I/F enable), this command is working as a NOP (00h) command. 2. This command has no effect when Normal mode is active.												
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	Status: Default Value Power On Sequence: Normal Display Mode On S/W Reset: Normal Display Mode On H/W Reset: Normal Display Mode On												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

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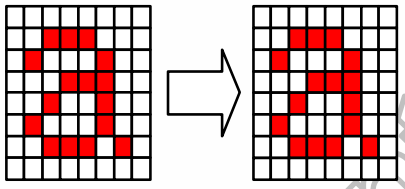
6.2.18 Display inversion off (20h)

20 H	INVOFF (Display Inversion Off)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 												
Restriction	1. RCM [1:0]= “1X”(RGB I/F enable), this command is working as a NOP (00h) command.												

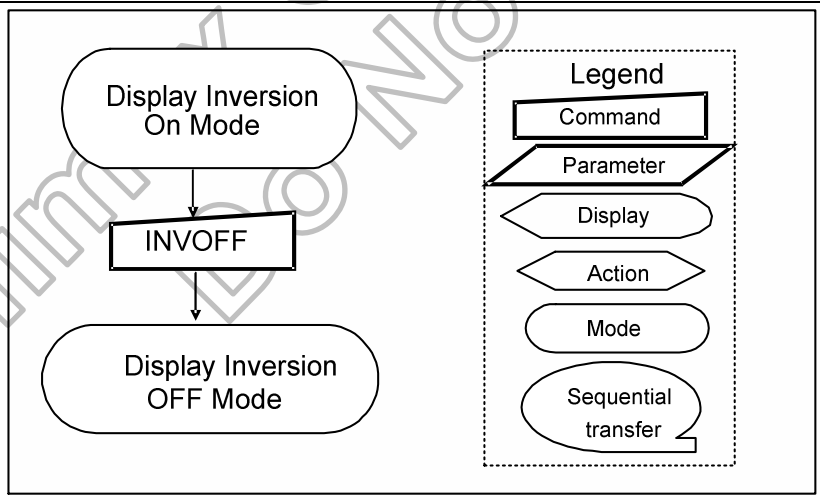
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



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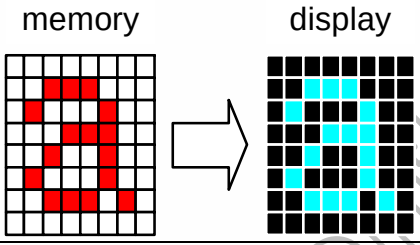
6.2.19 Display inversion on (21h)

21 H	INVON (Display Inversion On)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												

Description

This command is used to enter into display inversion mode.
This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
This command does not change any other status.

(Example)



Restriction

1. RCM [1:0]= “1X”(RGB I/F enable), this command is working as a NOP (00h) command.

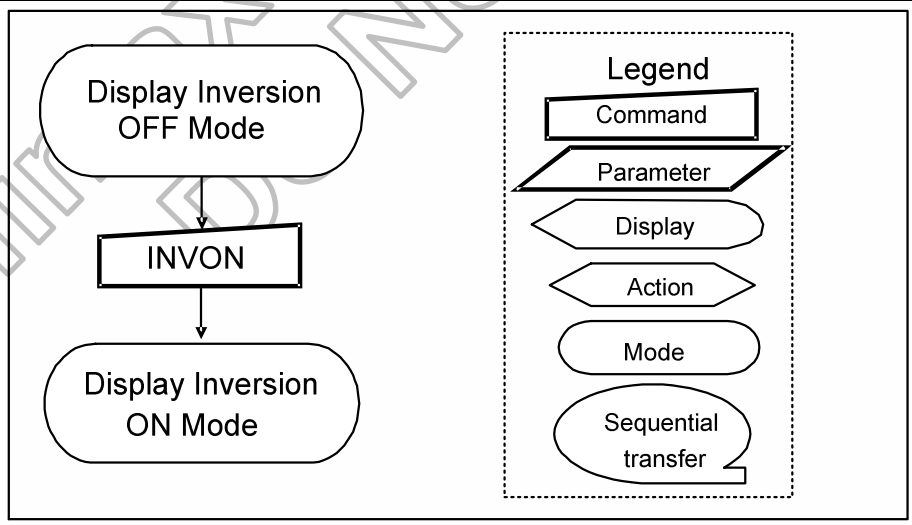
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



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6.2.20 Gamma set (26h)

26 H	GAMSET (Gamma Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	1	1	0	26
Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:

GC[7..0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

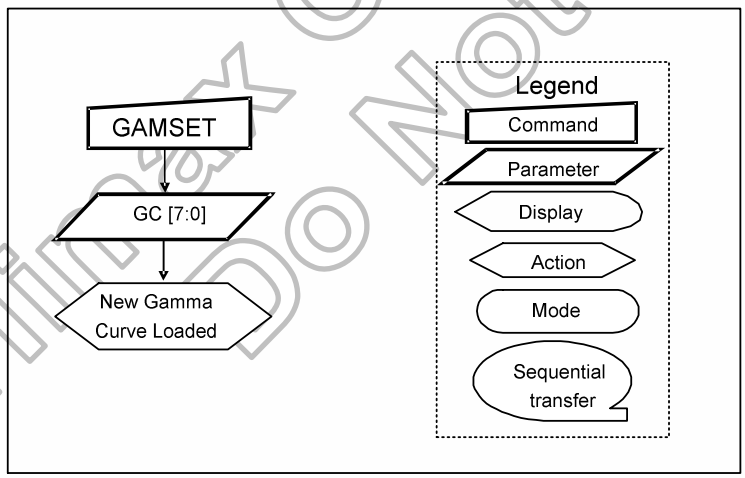
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



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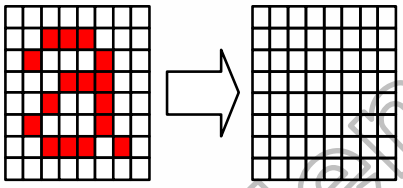
6.2.21 Display off (28h)

28 H	DISPOFF (Display Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) memory display 												
Restriction	This command has no effect when module is already in display off mode.												

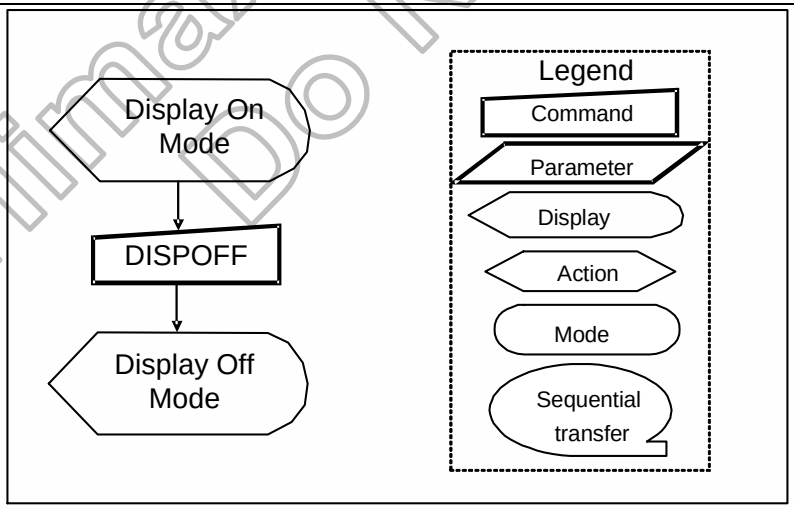
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



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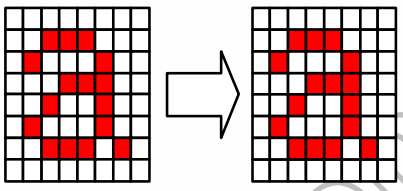
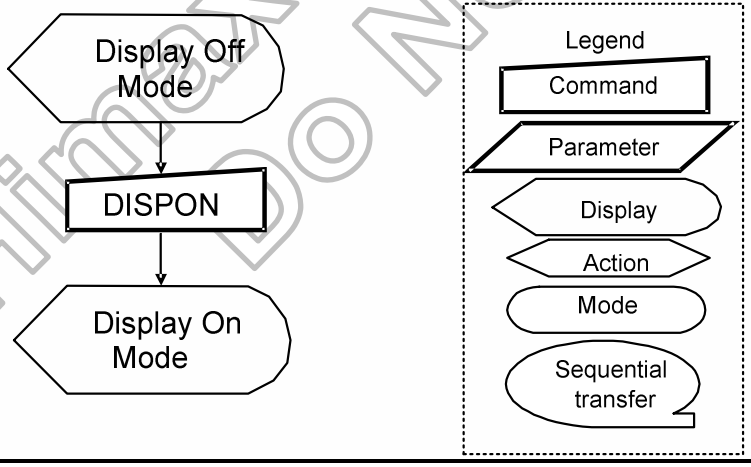
6.2.22 Display on (29h)

<table>
<tr><td>29 H</td><td colspan="13">DISPON (Display On)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)
memory display
  </td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

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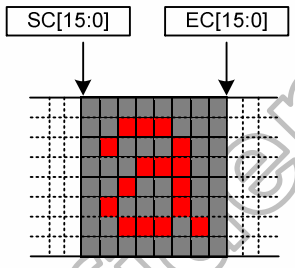
6.2.23 Column address set (2Ah)

2A H	CASET (Column Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	↑	1	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note 1
2nd parameter	1	↑	1	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd parameter	1	↑	1	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note 1
4th parameter	1	↑	1	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

1. SC[15:0] always must be equal to or less than EC[15:0]
Note: When SC[15:0] or EC[15:0] is greater than maximum address like below, data out of range will be ignored
0000h<=SC[15:0]<=EC[15:0] <=00EFh ,when MADCTL's B5=0
0000h<=SC[15:0]<=EC[15:0] <=013Fh ,when MADCTL's B5=1
2. RCM [1:0]= "1X"(RGB I/F enable), this command is working as a NOP (00h) command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh
S/W Reset	When MADCTL's B5=0:	
	SC[15:0]=0000h	EC[15:0]=00EFh
	When MADCTL's B5=1:	
	SC[15:0]=0000h	EC[15:0]=013Fh
H/W Reset	SC[15:0]=0000h	EC[15:0]=00EFh

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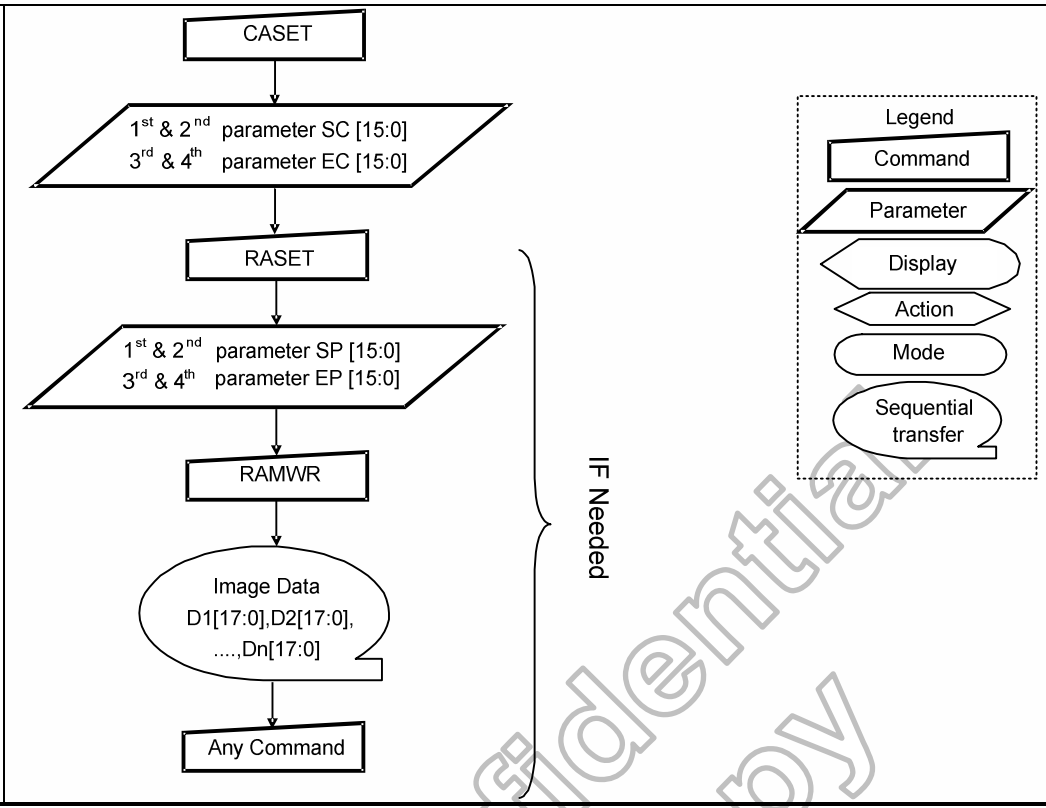
Flow Chart



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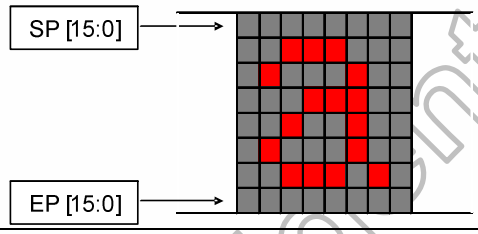
6.2.24 Page address set (2Bh)

2B H	PASET (Page Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	↑	1	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note 1
2nd parameter	1	↑	1	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd parameter	1	↑	1	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note 1
4th parameter	1	↑	1	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

1. SP[15:0] always must be equal to or less than EP[15:0]
Note: When SP[15:0] or EP[15:0] is greater than maximum row address like below, data of out of range will be ignored
0000h<=SP[15:0]<=EP[15:0]<=013Fh (When MADCTL's B5=0)
0000h<=SP[15:0]<=EP[15:0]<=00EFh (When MADCTL's B5=1)
2. RCM [1:0]= "1X"(RGB I/F enable), this command is working as a NOP (00h) command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=013Fh
S/W Reset	When MADCTL's B5=0:	
	SP[15:0]=0000h	EP[15:0]=013Fh
	When MADCTL's B5=1:	
	SP[15:0]=0000h	EP[15:0]=00EFh
H/W Reset	SP[15:0]=0000h	EP[15:0]=013Fh

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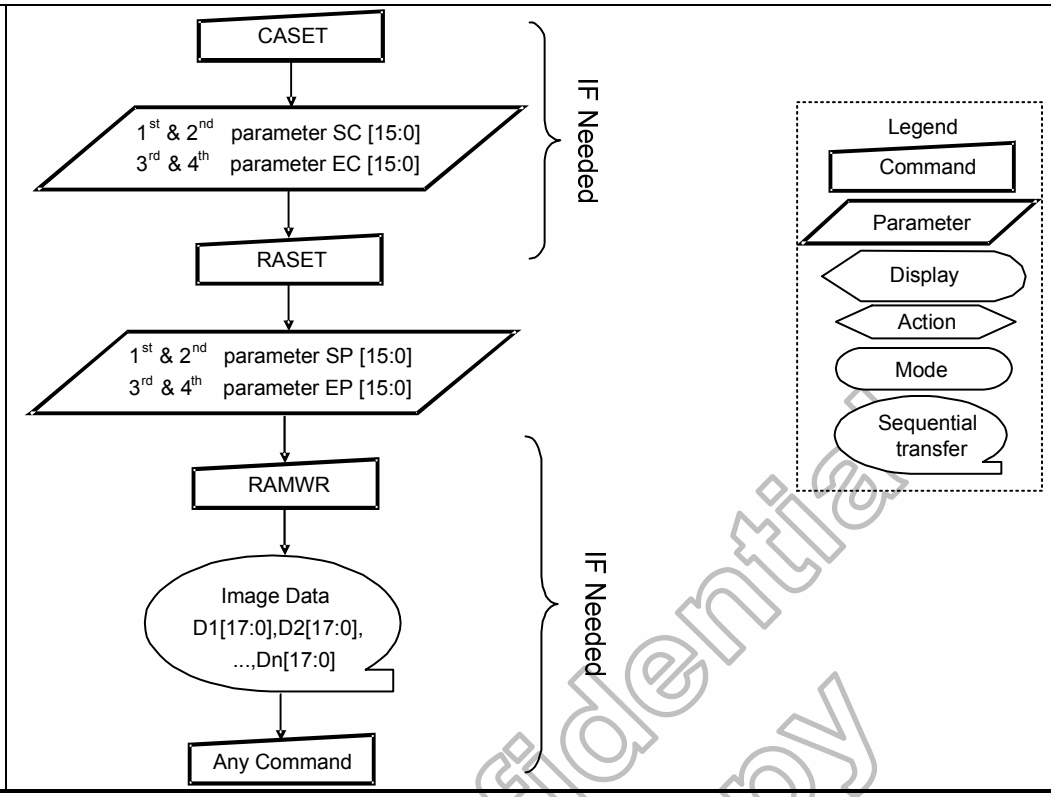
Flow Chart



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6.2.25 Memory write (2Ch)

2C H	RAMWR (Memory Write)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
nth parameter	1	↑	1	Dn[15:0]									00..FF

Description

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2)
Then D[7:0] is stored in frame memory and the column register and the page register incremented.
Sending any other command can stop frame Write.

Restriction

1. In all color modes, there is no restriction on length of parameters.
2. RCM [1:0]= “1X”(RGB I/F enable), this command is working as a NOP (00h) command.

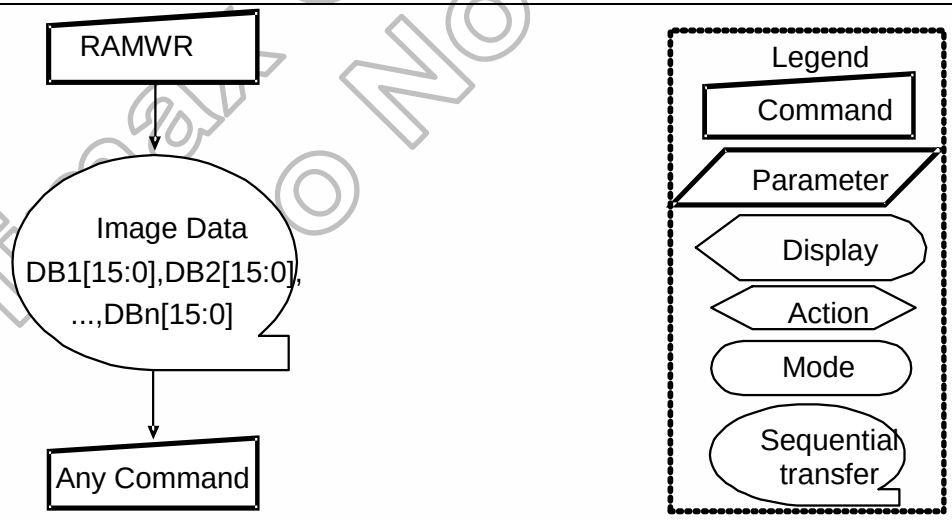
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



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6.2.26 Memory read (2Eh)

2E H	RAMRD (Memory Read)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
(n+1)th parameter	1	↑	1	Dn[15:0]									00..FF
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2) Then D[7:0] is read back from the frame memory and the column register and the page register incremented Frame Read can be stopped by sending any other command.												
Restriction	RGB I/F enable, this command is working as a NOP (00h) command.												

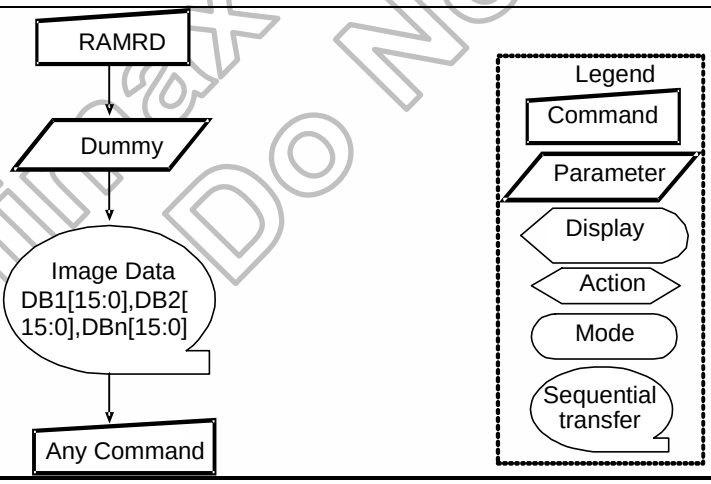
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



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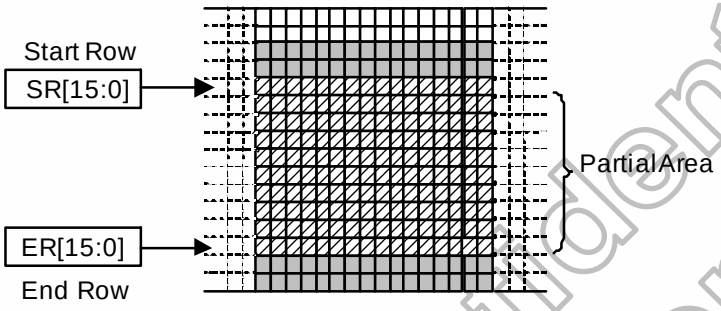
6.2.27 Partial area (30h)

30 H	PLTAR (Partial Area)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30
1st parameter	1	↑	1	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000:
2nd parameter	1	↑	1	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	013F
3rd parameter	1	↑	1	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000:
4th parameter	1	↑	1	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	013F

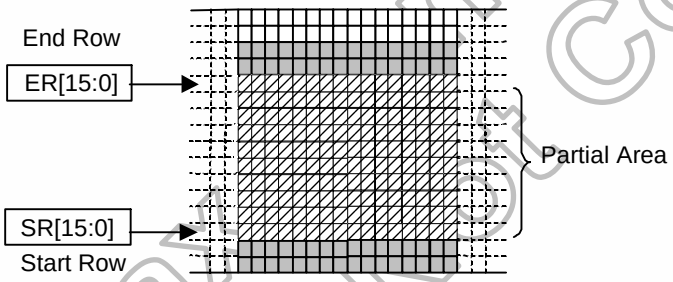
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

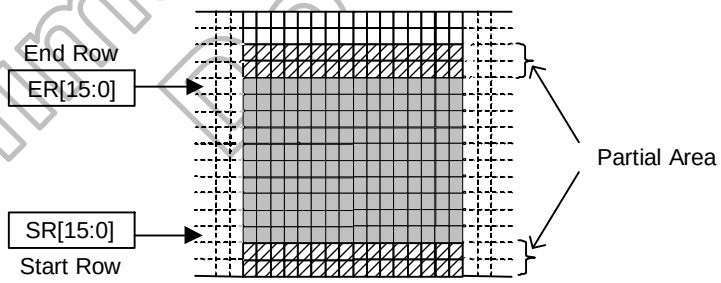
If End Row > Start Row when MADCTL B4(ML) = 0:



If End Row > Start Row when MADCTL B4(ML) = 1:



If End Row<Start Row when MADCTL's B4(ML) = 0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction

1. SR[15:0] and ER[15:0] cannot be exceeding than 013Fh.
2. RGB I/F enable, this command is working as a NOP (00h) command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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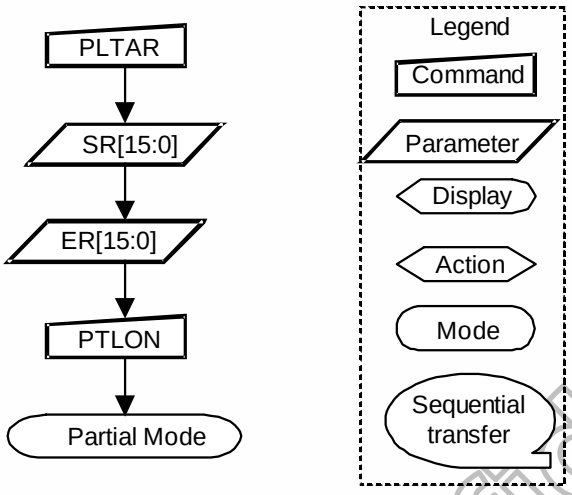
Default

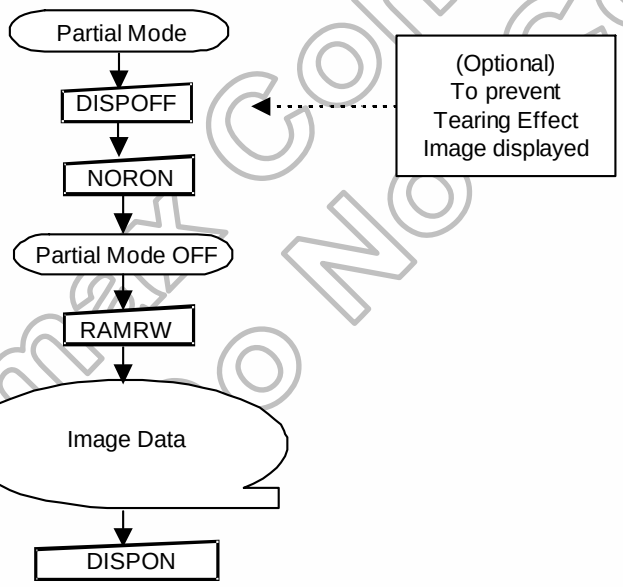
Status	Default Value	
Power On Sequence	SR[15:0]=0000h	ER[15:0]=013Fh
S/W Reset	SR[15:0]=0000h	ER[15:0]=013Fh
H/W Reset	SR[15:0]=0000h	ER[15:0]=013Fh

Flow Chart

1. To Enter Partial Display Mode:



2. To Leave Partial Display Mode



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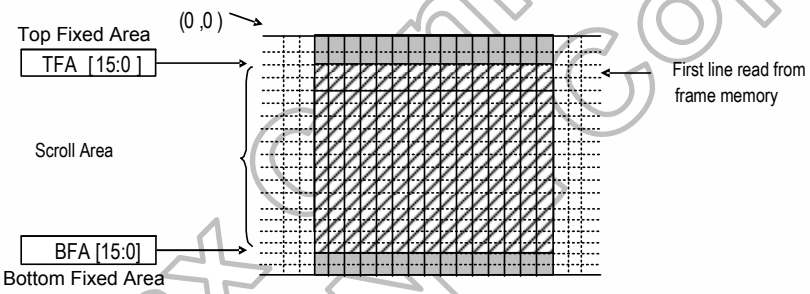
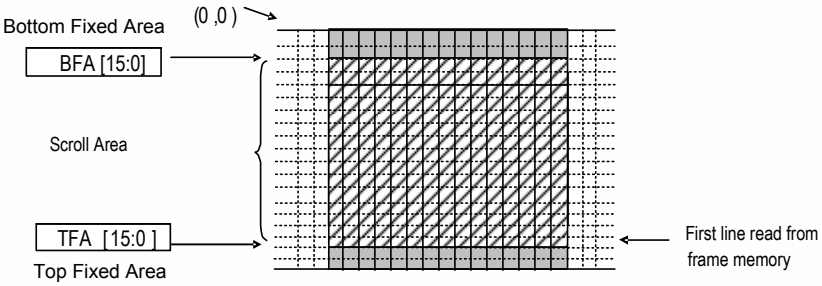
6.2.28 Vertical scrolling definition (33h)

33 H	VSCRDEF (Vertical Scrolling Definition)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1st parameter	1	↑	1	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	0000: 0140
2nd parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	
3rd parameter	1	↑	1	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	0000: 0140
4th parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	
5th parameter	1	↑	1	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	0000: 0140
6th parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.												
Restriction	1.The condition is (TFA+VSA+BFA)=320, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write. 2. RGB I/F enable, this command is working as a NOP (00h) command.												



When MADCTL B4=1

The 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



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Register Availability

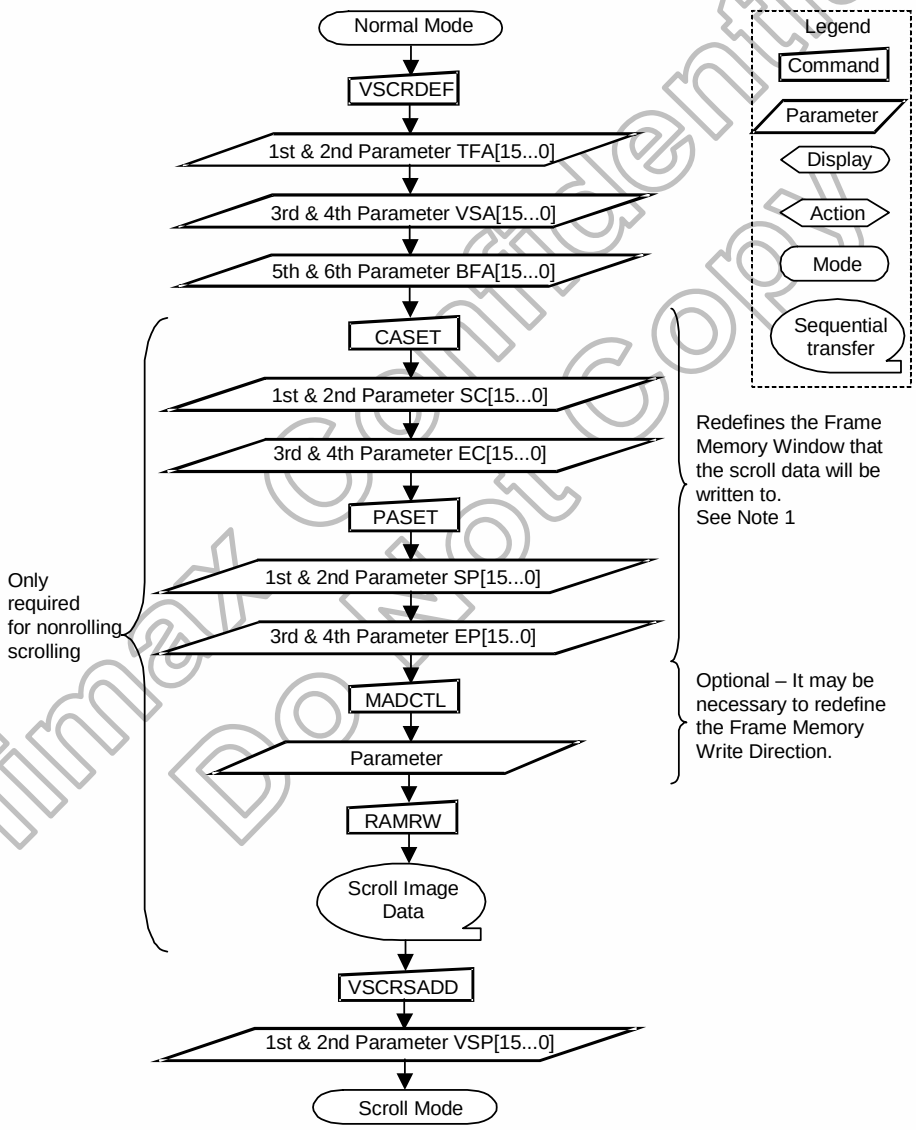
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000	VSA[15:0]=0140h	BFA[15:0]=0000
S/W Reset	TFA[15:0]=0000	VSA[15:0]=0140h	BFA[15:0]=0000
H/W Reset	TFA[15:0]=0000	VSA[15:0]=0140h	BFA[15:0]=0000

Flow Charts

1. To enter Vertical Scroll Mode:



Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

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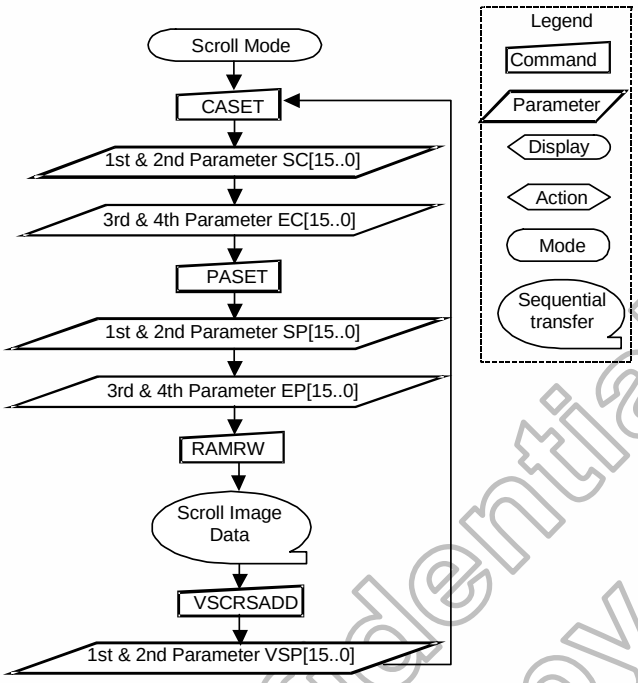
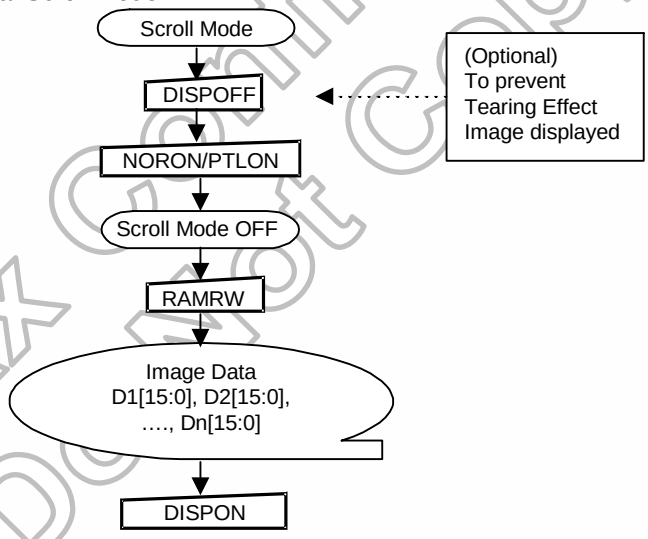
2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

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6.2.29 Tearing effect line off (34h)

34 H	TEOFF (Tearing Effect Line OFF)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												
Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.												
Restriction	1.This command has no effect when Tearing Effect output is already OFF. 2. RGB I/F enable, this command is working as a NOP (00h) command.												

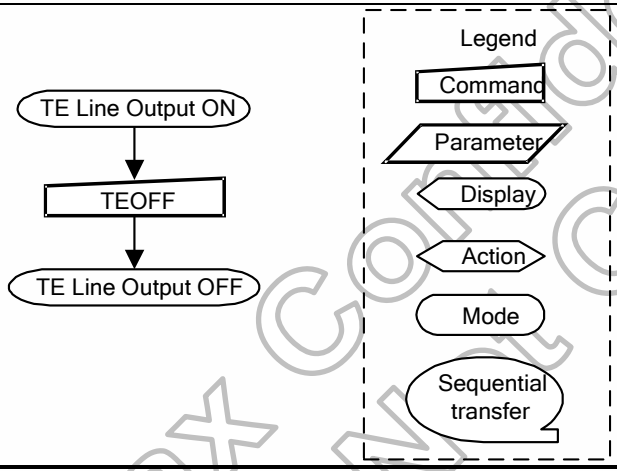
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



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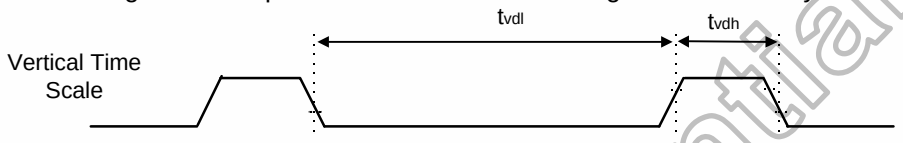
6.2.30 Tearing effect line on (35h)

35 H	TEON (Tearing Effect Line ON)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35
1stparameter	0	↑	1	-	-	-	-	-	-	-	-	TEMODE	-

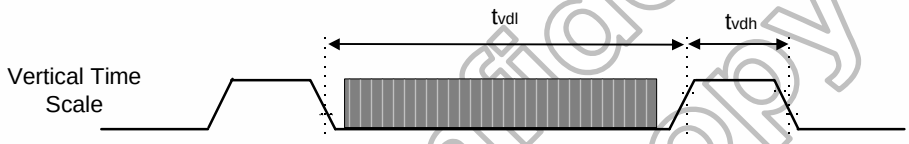
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only:



When TEMODE=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

1.This command has no effect when Tearing Effect output is already ON.
2. RGB I/F enable, this command is working as a NOP (00h) command.

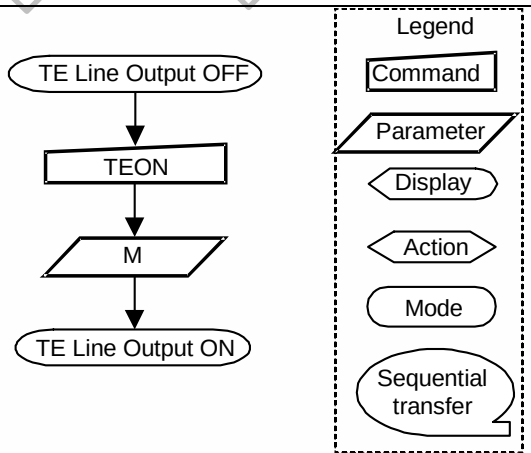
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



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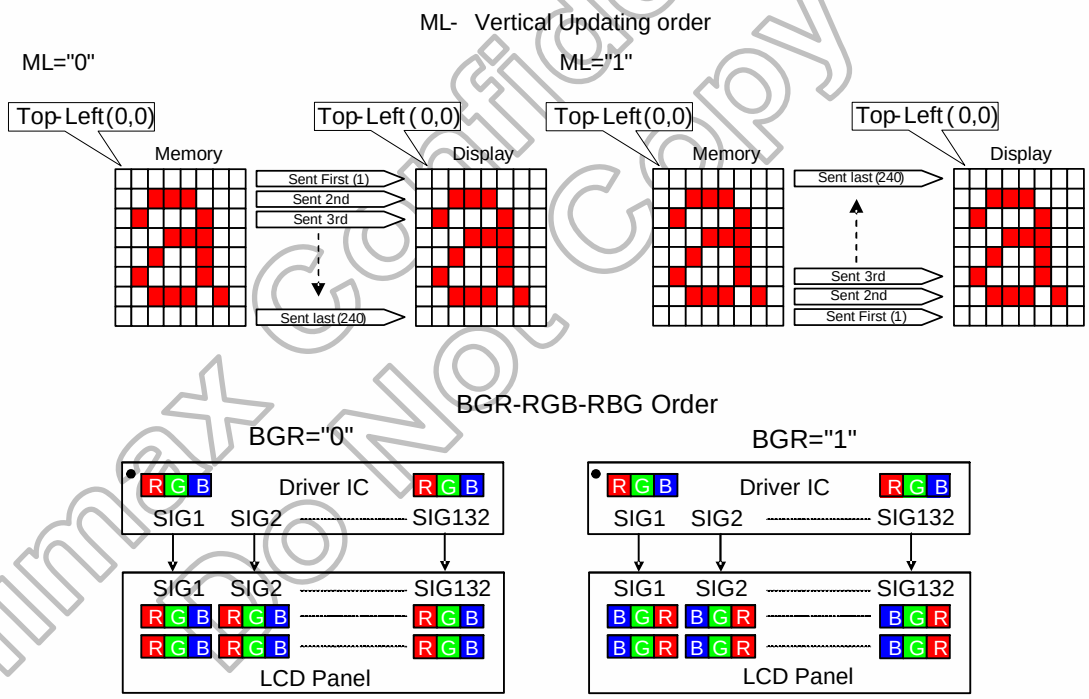
6.2.31 Memory access control (36h)

36 H	MADCTL (Memory Access Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1st parameter	1	↑	1	-	MY	MX	MV	ML	BGR	-	-	-	-

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. See Section 6.2.1 "System interface to GRAM Write Direction"
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



Note: Top-Left (0,0) means a physical memory location.

Restriction

D1 and D0 are set to '00' internally. D2 is implemented if the LCD is updating pixel-by-pixel. D2 is set to '0' internally if the LCD is updating line-by-line.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

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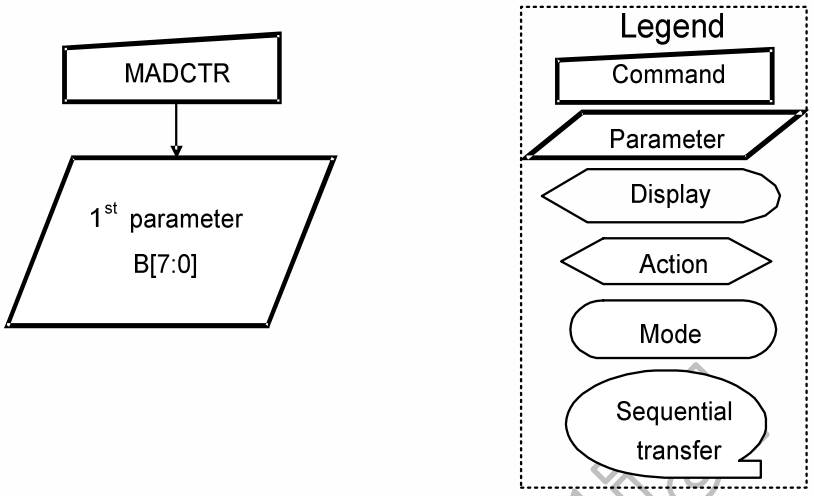
Flow Chart	

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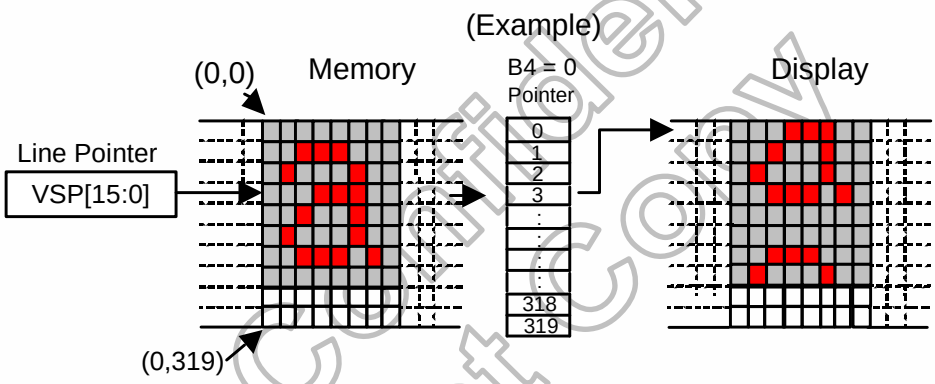
6.2.32 Vertical scrolling start address (37h)

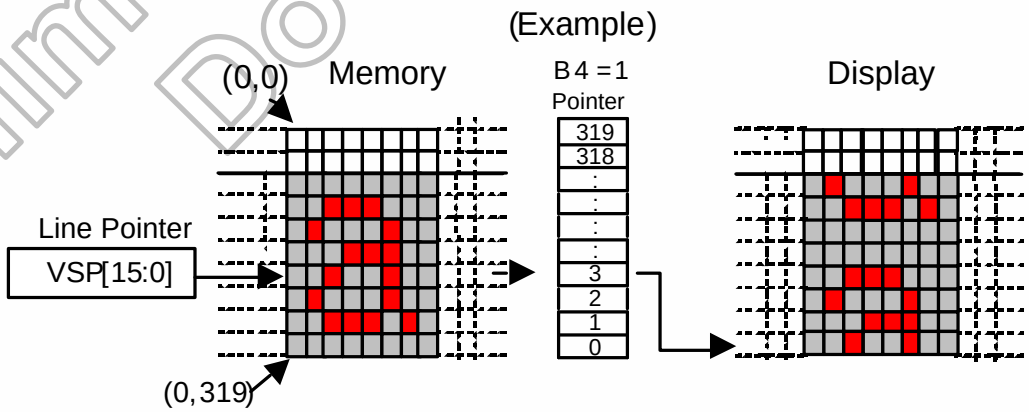
37 H	VSCRSADD (Vertical Scrolling Start Address)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	01. 3F
2nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When MADCTL B4='0'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '318'd' and VSP = '3d'



When MADCTL B4='1'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02d, Vertical Scrolling Area VSA = '318d' and VSP = '3d'



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction	1.Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel. 2. RGB I/F enable, this command is working as a NOP (00h) command.

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

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6.2.33 Idle mode off (38h)

38 H	IDMOFF (Idle Mode Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors.												
Restriction	1. This command has no effect when module is already in idle off mode. 2. RGB I/F enable, this command is working as a NOP (00h) command.												

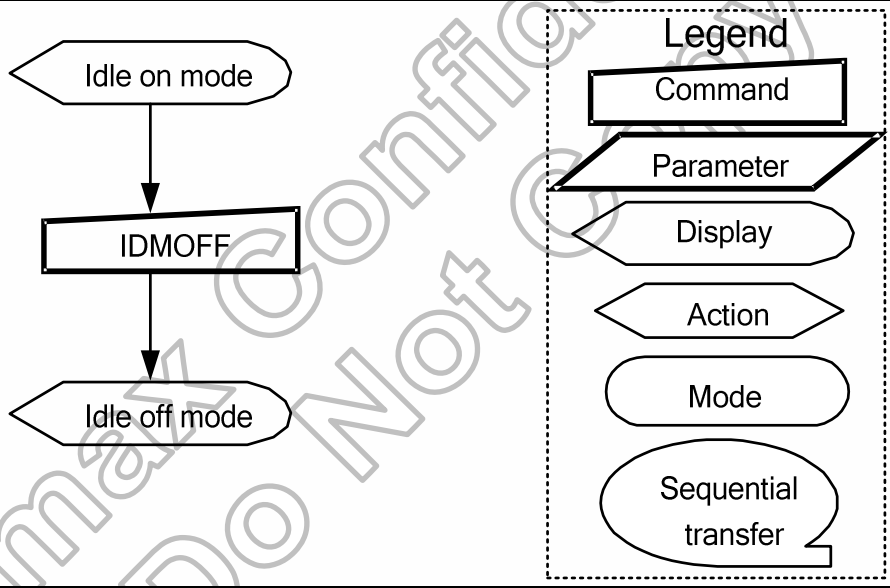
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



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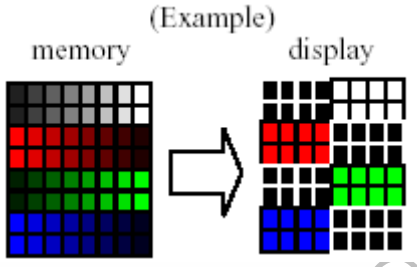
6.2.34 Idle mode on (39h)

39 H	IDMON (Idle Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory contents vs. Display Color			
	$R_5 R_4 R_3 R_2 R_1 R_0$	$G_5 G_4 G_3 G_2 G_1 G_0$	$B_5 B_4 B_3 B_2 B_1 B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

1. This command has no effect when module is already in idle off mode.
2. RGB I/F enable, this command is working as a NOP (00h) command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

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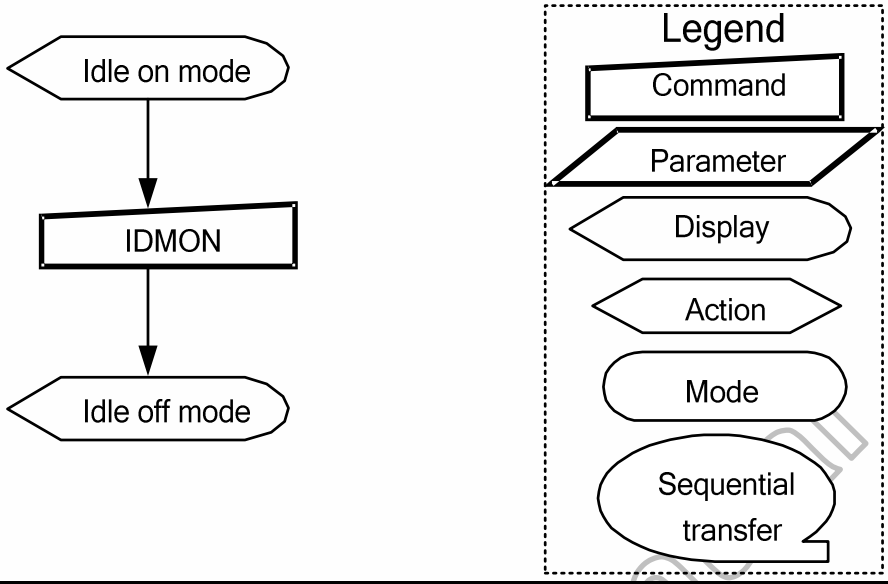
Flow Chart	

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6.2.35 Interface pixel format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	↑	1	-	-	CS EL2	CS EL1	CS EL0	-	D2	D1	D0	011, 101, 110

Description

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface (RCM[1:0]='0x')

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

RGB interface (RCM[1:0]='1x')

Interface Format	CSEL2	CSEL1	CSEL0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

Restriction

Register Availability

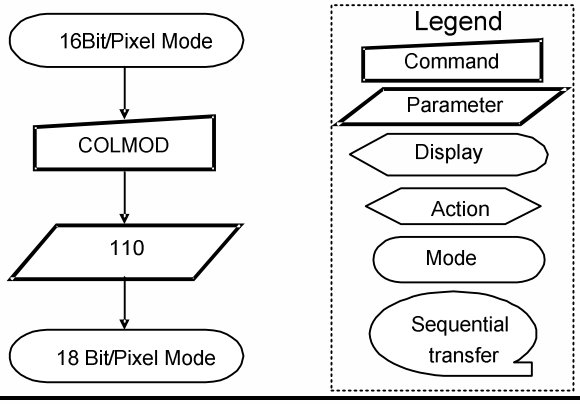
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	No Change
H/W Reset	18-bit/pixel

Flow Chart

Example:



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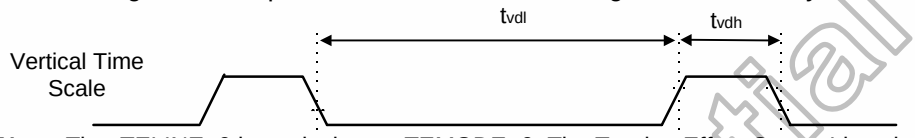
6.2.36 Set tear scan line (44h)

44 H	TESL(Tear Effect Scan Lines)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  **Note:** That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.												
Restriction	The command has no effect when Tearing Effect output is already ON.												

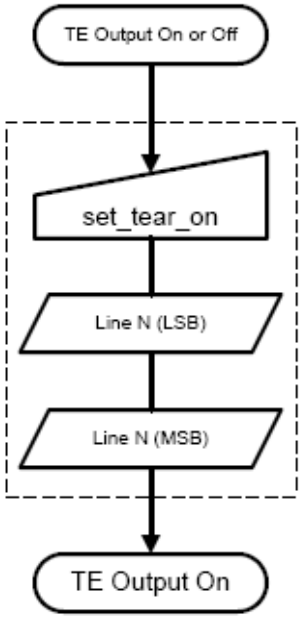
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	TELINE[15:8]=0000h
S/W Reset	TELINE[15:8]=0000h
H/W Reset	TELINE[15:8]=0000h

Flow Chart



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6.2.37 Write display brightness value (51h)

51 H	WRDISBV (Write Display Brightness Value)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	0	1	51
1st parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00..FF

Description

This command is used to adjust the brightness value of the display.
The backlight PWM pulse output duty is equal to DBV[7:0]/255 x CABC_duty.
For details, please refer to chapter "7.4.3 Brightness Control Block".

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.), because this command is only for Nokia.

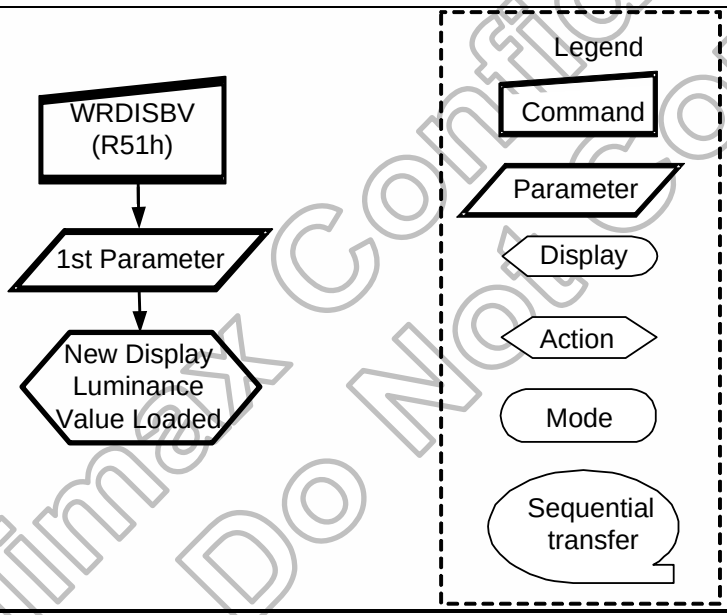
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.38 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	0	52
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	xx

Description

This command returns the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.
DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (R53h)" command is '0'.
DBV[7:0] is manual set brightness specified with "Write CTRL Display (R53h)" command when bit BCTRL is '1'.
When bit BCTRL of "Write CTRL Display (R53h)" command is '1' and bit C1/C0 of "Write Content Adaptive Brightness Control (R55h)" are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (R51h)" command.
For details, please refer to chapter "7.4.3 Brightness Control Block".

Restriction

-

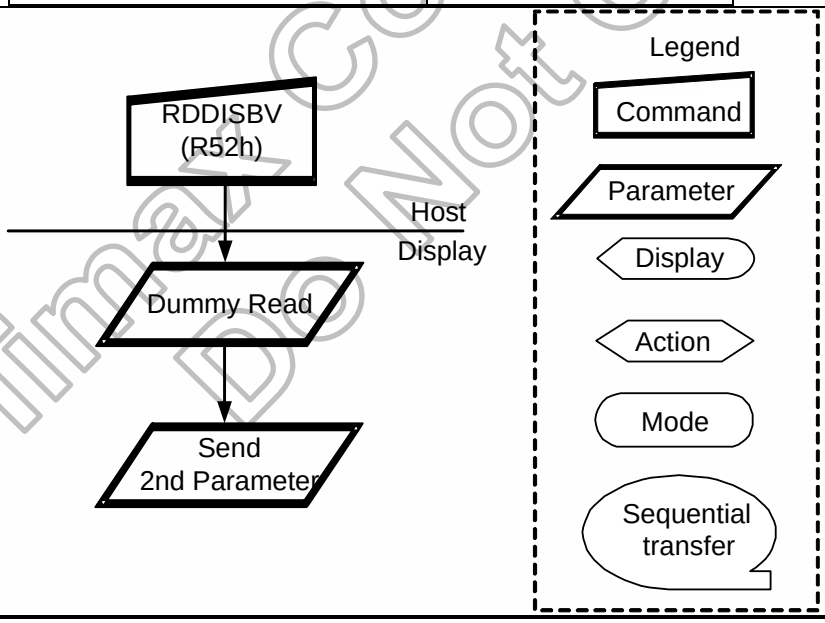
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.39 Write control display (53h)

53H	WRCTRLD (Write Control Display)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	1	53
1st parameter	1	↑	1	-	-	-	BCTRL	-	DD	BL	-	-	00..FF

Description

This command is used to control display brightness.

BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off (Brightness registers are 00h, DBV[7:0] of R52h)
1 = On (Brightness registers are active, according to the other parameters.)

Display Dimming **(DD):** (Only for manual brightness setting)
DD = **0**: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low.)
1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

Restriction

-

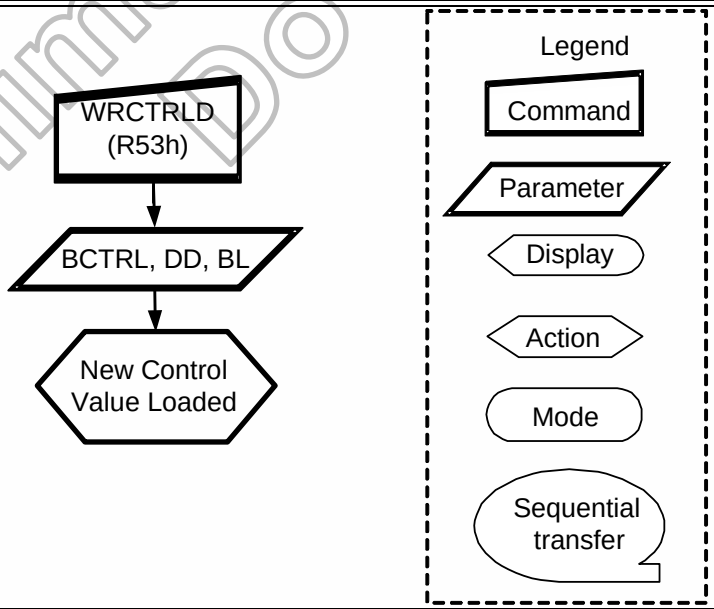
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.40 Read control value display (54h)

54H	RDCTRLD (Read Control Value Display)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	0	54
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	xx

Description

This command returns ambient light and brightness control values, see chapter: "Write CTRL Display (R53h)".

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off
1 = On

Display Dimming (DD):
DD = 0: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off
1 = On

Restriction

-

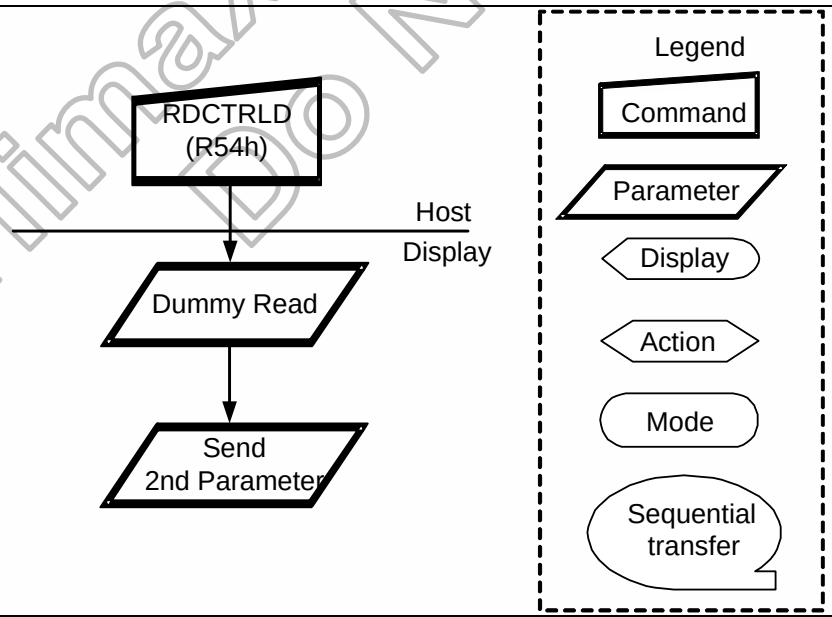
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.41 Write content adaptive brightness control (55h)

55H	WRCABC (Write Content Adaptive Brightness Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	1	55
1st parameter	1	↑	1	-	-	-	-	-	-	-	C1	C0	00..03

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

Restriction

-

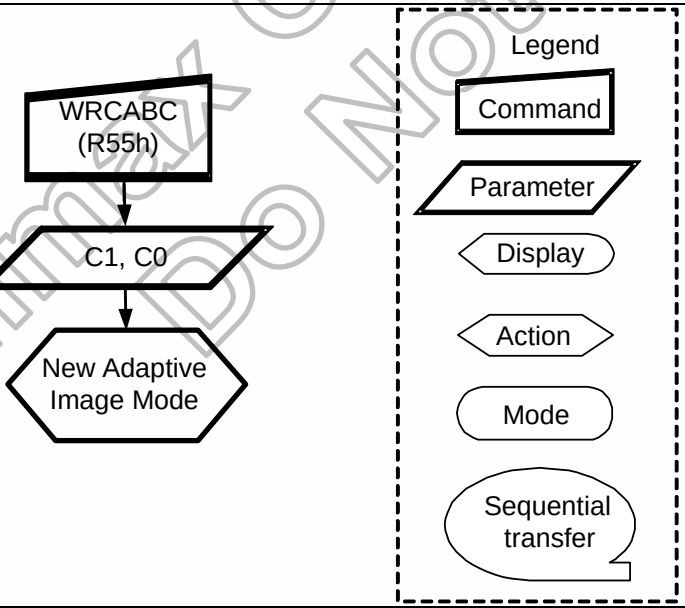
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.42 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	1	0	56
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

Restriction

-

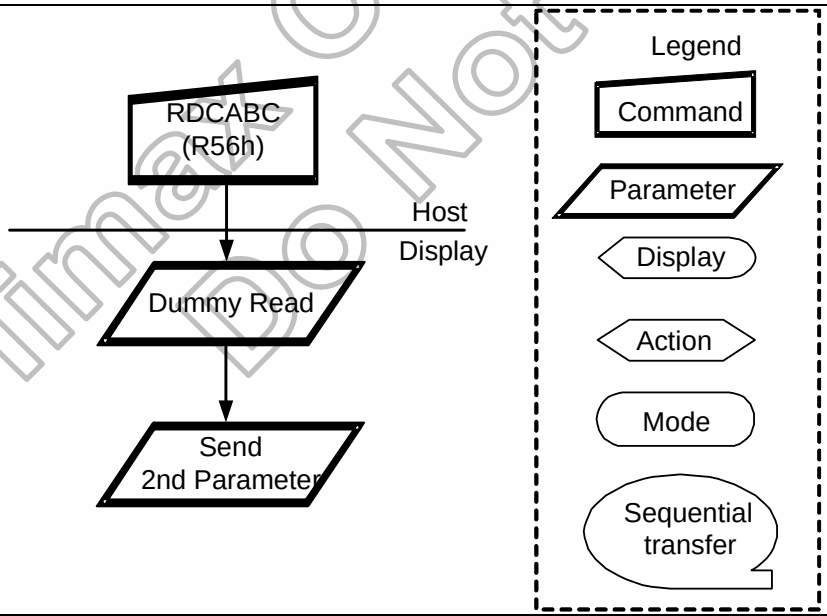
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.43 Write CABC minimum brightness (5Eh)

5EH	WRCABCMB (Write CABC Minimum Brightness)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00..FF

Description

This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
For details, please refer to chapter “5.15.4 Minimum brightness setting of CABC function”.

Restriction

-

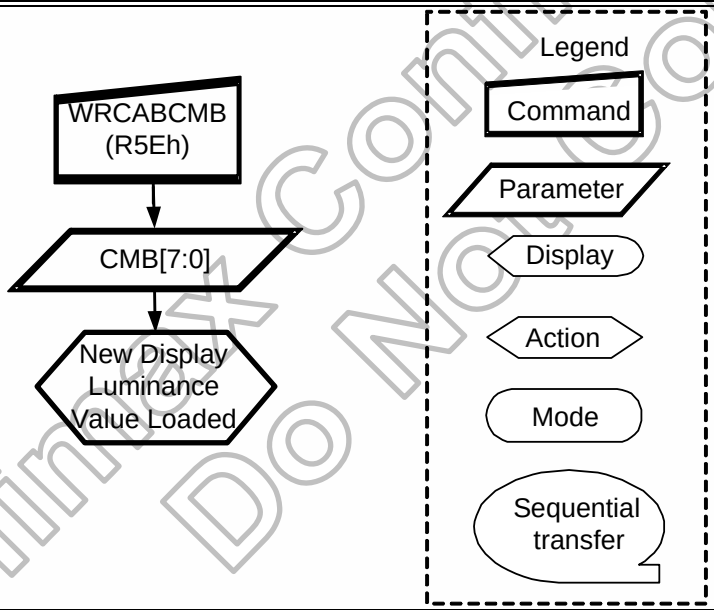
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.44 Read CABC minimum brightness (5Fh)

5FH	RDCABCMB (Read CABC Minimum Brightness)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	xx

Description

This command is used to return the minimum brightness value of CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (R5Eh)” command.

Restriction

-

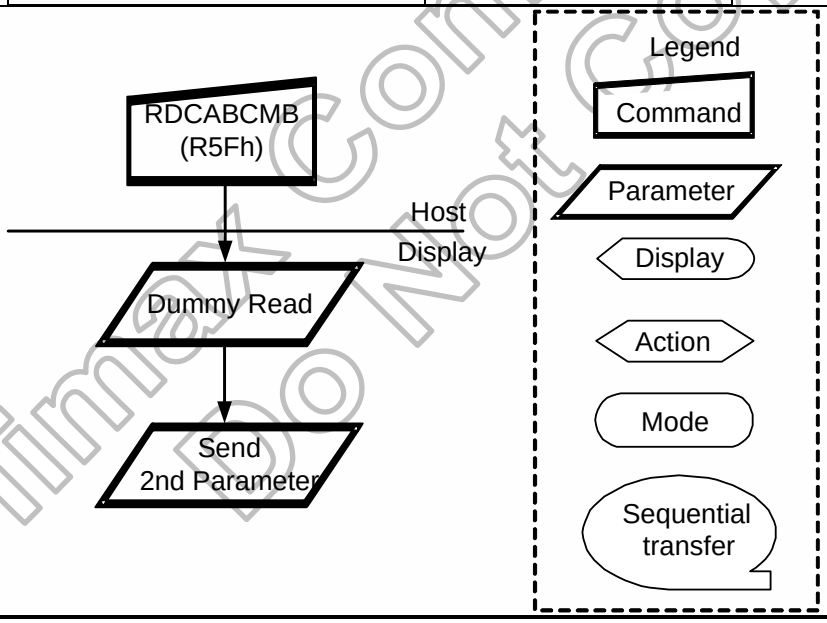
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.45 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	1	0	1	0	0	0	68
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	xx

Description

This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out command as described in the table below.

Bit D7: Register Loading Detection.
See Section "7.4.4.1 Register Loading Detection"

Bit D6: Functionality Detection.
See Section "7.4.4.2 Functionality Detection"

Bit D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'.

Restriction

-

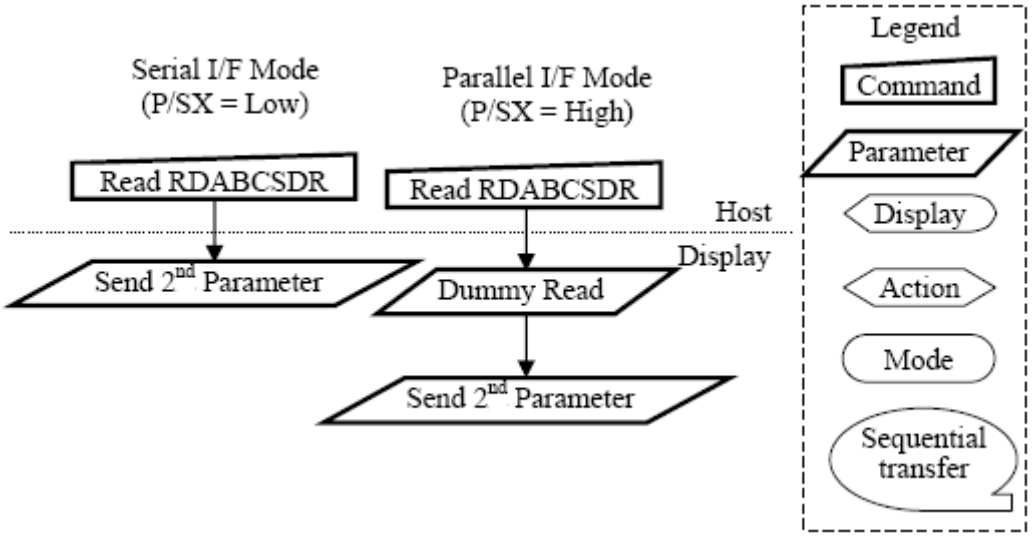
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.2.46 Read ID1 (DAh)

DA H	RDID1 (Read ID1)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	module's manufacturer m[7:0]								-
Description	This read byte identifies the LCD module's manufacturer. It is specified by Nokia and for m[7:0] is defined as xxHEX.												
Restriction	-												

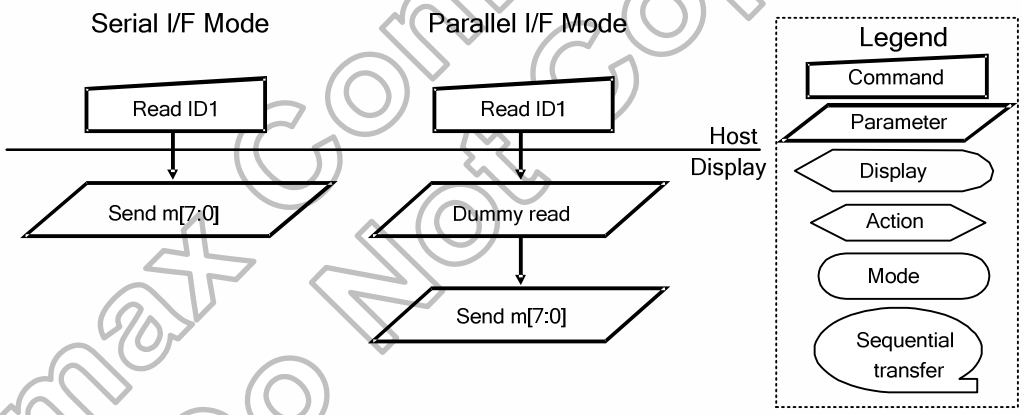
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



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6.2.47 Read ID2 (DBh)

DB H	RDID2 (Read ID2)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	V7	V6	V5	V4	V3	V2	V1	V0	-
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications.												
Restrictions	-												

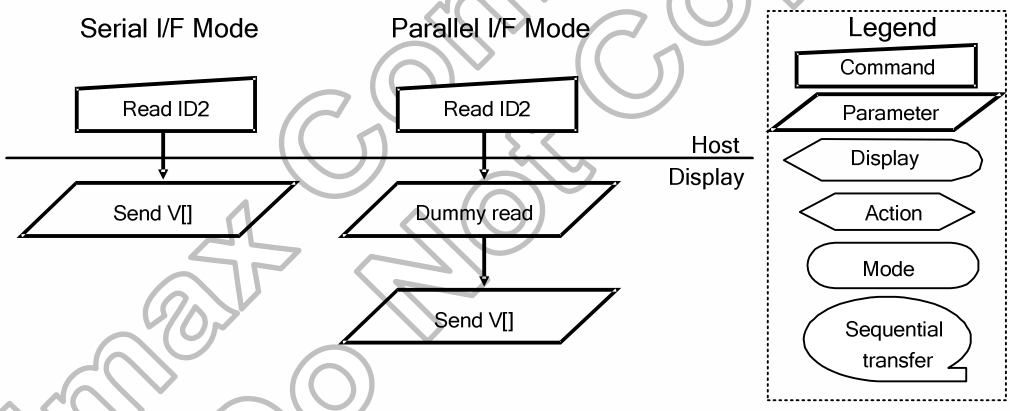
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	See Description
S/W Reset	See Description
H/W Reset	See Description

Flow Chart



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6.2.48 Read ID3 (DCh)

DC H	RDID3 (Read ID3)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	-
Description	This read byte identifies the LCD module/driver. It is specified by Nokia and for this LCD project module is defined as ID.												
Restrictions	-												

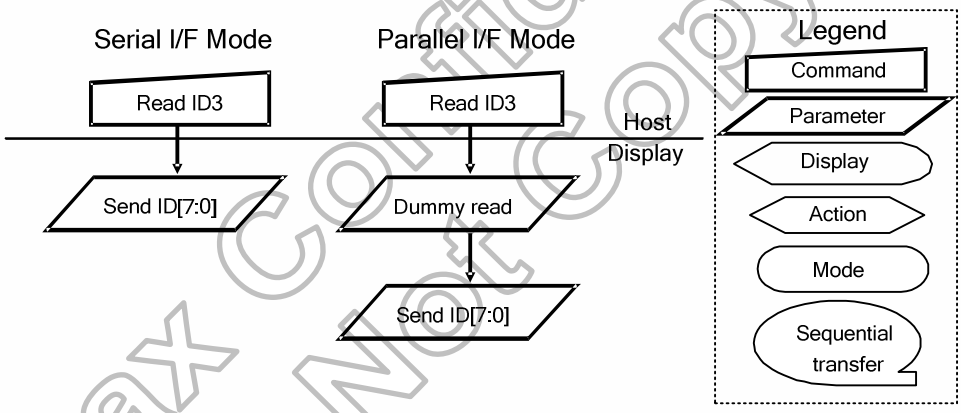
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



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6.2.49 SETOSC: set internal oscillator (B0h)

B0 H	SETOSC(Set Internal Oscillator)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	1	-	I_UADJ[3:0]				N_UADJ[3:0]				66
2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	OSC_EN	00

Description

These command is used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. In RGB interface mode, internal oscillator will be stop to oscillate and OSC_EN bit control is invalid.

N_UADJ[2:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I_UADJ[2:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.
For details, please refer to "7.1 Internal Oscillator" section.

UADJ3	UADJ2	UADJ1	UADJ0	Internal Oscillator Frequency	Display Frame rate
0	0	0	0	3.0 MHz	30Hz
0	0	0	1	3.5 MHz	35Hz
0	0	1	0	4.0 MHz	40Hz
0	0	1	1	4.5 MHz	45Hz
0	1	0	0	5.0 MHz	50Hz
0	1	0	1	5.5 MHz	55Hz
0	1	1	0	6.0 MHz	60Hz
0	1	1	1	6.5 MHz	65Hz
1	0	0	0	7.0 MHz	70Hz
1	0	0	1	7.5 MHz	75Hz
1	0	1	0	8.0 MHz	80Hz
1	0	1	1	8.5 MHz	85Hz
1	1	0	0	9.0 MHz	90Hz
1	1	0	1	9.5 MHz	95Hz
1	1	1	0	10.0 MHz	100Hz
1	1	1	1	10.5 MHz	105Hz

Restrictions

1. Must enable SETEXTC command
2. In RGB interface mode, oscillator will be stop and these bits control are invalid.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	OSC_EN=0, P_UADJ[2:0]=4'b0110, I_UADJ[2:0]=4'b0110.
S/W Reset	OSC_EN=0, P_UADJ[2:0]=4'b0110, I_UADJ[2:0]=4'b0110.
H/W Reset	OSC_EN=0, P_UADJ[2:0]=4'b0110, I_UADJ[2:0]=4'b0110.

Flow Chart -

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6.2.50 SETPWCTR: set power control (B1h)

B1 H	SETPWCTRL (Set power control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	00
2nd parameter	1	↑	1	-	-					BT[2:0]			01
3rd parameter	1	↑	1	-	-	-	VRH[5:0]						1B
4th parameter	1	↑	1	-	-	-	-	-	-	AP[2:0]			03
5th parameter	1	↑	1	-	-	I /IP_FS0[2:0]			-	N/P_FS0[2:0]			44
6th parameter	1	↑	1	-	-	I/IP_FS1[2:0]			-	N/P_FS1[2:0]			44
7th parameter	1	↑	1	-	GASEN	VCO MGG	--	PON	DK	-	-	STB	89

Description

VRH[5:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.VREG1=Decimal(VRH[5:0])x0.05+3.3. The default value is 1Bh(27x0.5+3.3=4.65V)

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	0	0	3.30
0	0	0	0	0	1	3.35
0	0	0	0	1	0	3.40
0	0	0	0	1	1	3.45
0	0	0	1	0	0	3.50
0	0	0	1	0	1	3.55
0	0	0	1	1	0	3.60
0	0	0	1	1	1	3.65
0	0	1	0	0	0	3.70
:	:	:	:	:	:	:
0	1	1	1	0	1	4.75
0	1	1	1	1	0	4.80
0	1	1	1	1	1	STOP
1	0	0	0	0	0	STOP
1	0	0	0	0	1	STOP
:	:	:	:	:	:	:
1	1	0	0	0	0	STOP
1	1	0	0	0	1	STOP
1	1	0	0	1	0	STOP
1	1	0	0	1	1	STOP
1	1	1	0	1	1	STOP
:	:	:	:	:	:	:
1	1	1	1	1	0	STOP
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.

Note: (1) **Internal VREF can be modified by Custom's special request.**
VREG1={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/4.8)**

BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

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BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.0V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	1	5.0V	-VCI	3DDVDH	-2DDVDH
0	1	0	5.0V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	5.0V	-VCI	VCI + 2DDVDH	-VCI-2DDVDH
1	0	0	5.0V	-VCI	VCI + 2DDVDH	-2DDVDH
1	0	1	5.0V	-VCI	VCI + 2DDVDH	VCI-2DDVDH
1	1	0	5.0V	-VCI	2DDVDH	-2DDVDH
1	1	1	5.0V	-VCI	2DDVDH	-VCI-DDVDH

N/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal / Partial mode.
I/PI_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to Internal Oscillator section.

FS02	FS01	FS00	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Small

N/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal / Partial mode.
I/PI_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “Internal Oscillator” section.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency

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1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

STB: When STB = "1", the HX8347-I into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0") ,
b. Start the oscillation

In the standby mode, the GRAM data and register content will be keeping.

GASEN: This stands for abnormal power-off monitor function when the power is off.

DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation. For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

VCOMG: Specify on/off control of step-up circuit 3 for VCL voltage generation. For detail, see the Power Supply Setting Sequence. When VCOMG = '0', VCOML = GND.

VCOMG	Operation of step-up circuit 3
0	OFF
1	ON

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Restrictions: Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DP_STB=1’b0, BT[2:0]=3’b001, VRH[5:0]=6’b011011, AP[2:0]=3’b011, I/PI_FS0[2:0]=3’b100, N/P_FS0[2:0]=3’b100, I/PI_FS1[2:0]=3’b100, N/P_FS1[2:0]=3’b100, GASEN=1’b1, VCOMG=1’b0,PON=1’b0, DK=1’b0, STB=1’b0</td></tr>
<tr><td>S/W Reset</td><td>DP_STB=1’b0, BT[2:0]=3’b001, VRH[5:0]=6’b011011, AP[2:0]=3’b011, I/PI_FS0[2:0]=3’b100, N/P_FS0[2:0]=3’b100, I/PI_FS1[2:0]=3’b100, N/P_FS1[2:0]=3’b100 GASEN=1’b1, VCOMG=1’b0,PON=1’b0, DK=1’b0, STB=1’b0</td></tr>
<tr><td>H/W Reset</td><td>DP_STB=1’b0, BT[2:0]=3’b001, VRH[5:0]=6’b011011, AP[2:0]=3’b011, I/PI_FS0[2:0]=3’b100, N/P_FS0[2:0]=3’b100, I/PI_FS1[2:0]=3’b100, N/P_FS1[2:0]=3’b100 GASEN=1’b1, VCOMG=1’b0,PON=1’b0, DK=1’b0, STB=1’b0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

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6.2.51 SETDISPLAY: set display related register (B2h)

B2H	SETDISCTRL (Set display control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	0	B2
1st parameter	1	↑	1	-	-	-	-	-	ISC3	ISC2	ISC1	ISC0	01
2nd parameter	1	↑	1	-	PT1	PT0	PTV1	PTV0	-	-	PTG	REF	A3
3rd parameter	1	↑	1	-	-	-	NL [5:0]						27
4th parameter	1	↑	1	-	-	SCN[6:0]							00
5th parameter	1	↑	1	-	-	-	GON	DTE	D1	D0	-	-	20

Description

This command is used to set display related register

D[1:0]: When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level.
When D[1:0]= '01', the internal display of the HX8347-I is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
1	0	Fixed to VGL
1	1	Normal Operation (VGH/VGL)

PT[1:0] : Specify the Non-display area source output in partial display mode.

REV_Panel	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
1 (Normally Black Panel)	18'h00000 . 18'h3FFFF	V63P . V0P	V0N . V63N	V63P	V0N	GND	GND	Hi-z	Hi-z
0 (Normally White Panel)	18'h00000 . 18'h3FFFF	V0P . V63P	V63N . V0N	V63P	V0N	GND	GND	Hi-z	Hi-z

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REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	5 frames	83ms
0	0	1	0	9 frames	150ms
0	0	1	1	13 frames	217ms
0	1	0	0	17 frames	283ms
0	1	0	1	21 frames	350ms
0	1	1	0	25 frames	417ms
0	1	1	1	29 frames	483ms
1	0	0	0	33 frames	550ms
1	0	0	1	37 frames	616ms
1	0	1	0	41 frames	683ms
1	0	1	1	45 frames	750ms
1	1	0	0	49 frames	816ms
1	1	0	1	53 frames	883ms
1	1	1	0	57 frames	950ms
1	1	1	1	Setting inhibited	

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PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	--	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	0	0	--	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	1	0	--	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving

NL[5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL5	NL4	NL3	NL2	NL1	NL0	LCD Drive lines
0	0	0	0	0	0	8 lines
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
:	:	:	:	:	:	:
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
other setting						320 lines

SCN[6:0]: Specifies the gate line where the gate driver starts scan.

SCN[6:0]	Scanning start position	
	GS = 0	GS =1
00h ~ 47h	G(1+SCN[6:0]*4)	G(SCN[6:0]*4+(NL[5:0]+1)*8)

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	D1-0=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, PTV[1:0] = 2'b10, ISC[3:0]=4'b001,NL[5:0] = 6'b100111, SCN[6:0]= 7'b0000000.
S/W Reset	D1-0=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, PTV[1:0] = 2'b10, ISC[3:0]=4'b001 ,NL[5:0] = 6'b100111, SCN[6:0]= 7'b0000000.
H/W Reset	D1-0=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, PTV[1:0] = 2'b10, ISC[3:0]=4'b0011 ,NL[5:0] = 6'b100111, SCN[6:0]= 7'b0000000.

Flow Chart

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6.2.52 SETRGB: set RGB interface (B3h)

B3 H	SETRGBIF(Set RGB interface related register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	↑	1	-	-	-	EPF[1:0]				RCM[1:0]		00
2nd parameter	1	↑	1	-			-	-	DPL	HSPL	VSPL	EPL	00
3rd parameter	1	↑	1	-	HBP[7:0]								08
4th parameter	1	↑	1	-	HBP[9:8]		VBP[5:0]						04

Description

This command is used to set RGB interface related register

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	Display image	Operation
0	High	Enable	Write data to D17-0
0	Low	Disable	Disable
1	High	Disable	Disable
1	Low	Enable	Write data to D17-0

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

HBP[9:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2

HBP[9:0]	No. of clock cycle of DOTCLK
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
1021d	1021
1022d	1022
1023d	Setting Inhibited

VBP[6:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2

VBP[6:0]	No. of clock cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
125d	125
126d	126
127d	Setting Inhibited

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<table>
<tr><td></td><td>
RCM[1:0]: RGB and MCU interface select.
<table>
<tr><th>RCM1</th><th>RCM0</th><th>Interface Select</th></tr>
<tr><td>0</td><td>x</td><td>System Interface (1)</td></tr>
<tr><td>1</td><td>0</td><td>RGB Interface (1) (VS+HS+DE)</td></tr>
<tr><td>1</td><td>1</td><td>RGB Interface (2) (VS+HS)</td></tr>
</table>
EPF[1:0]: 65k colours mapping
<table>
<tr><th>EPF1</th><th>EPF0</th><th>Mapping</th></tr>
<tr><td colspan="2">Other setting</td><td>No mapping</td></tr>
<tr><td>1</td><td>1</td><td>If R[4:0] = B[4:0],
R[5:0] = {R[4:0],G[0]}, B[5:0] = {B[4:0],G[0]}</td></tr>
</table>
</td></tr>
<tr><td>Restrictions</td><td>Must enable SETEXTC command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DPL=1’b0, HSPL=1’b0, VSPL=1’b0, EPL=1’b0, RCM[1:0]=2’b00, HBP[9:0]=10’b0000001000, VBP[5:0]=6’b000100, EPF[1:0] = 2’b00</td></tr>
<tr><td>S/W Reset</td><td>DPL=1’b0, HSPL=1’b0, VSPL=1’b0, EPL=1’b0, RCM[1:0]=2’b00, HBP[9:0]=10’b0000001000, VBP[5:0]=6’b000100, EPF[1:0] = 2’b00</td></tr>
<tr><td>H/W Reset</td><td>DPL=1’b0, HSPL=1’b0, VSPL=1’b0, EPL=1’b0, RCM[1:0]=2’b00, HBP[9:0]=10’b0000001000, VBP[5:0]=6’b000100, EPF[1:0] = 2’b00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

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6.2.53 SETCYC: set display cycle register (B4h)

B4 H	SETCYC (Set display cycle)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	0	0	B4
1st parameter	1	↑	1	-	-	I/IP_NW[2:0]			-	N/P_NW[2:0]			11
2nd parameter	1	↑	1	-	I/PI_RTN[3:0]				N/P_RTN[3:0]				88
3rd parameter	1	↑	1	-	-	-	I/PI_DIV[1:0]		-	-	N/P_DIV[1:0]		00
4th parameter	1	↑	1	-	N/P_DUM[7:0]								32
5th parameter	1	↑	1	-	I/IP_DUM[7:0]								32
6th parameter	1	↑	1	-	GDON[7:0]								0D
7tp parameter	1	↑	1	-	GDOF[7:0]								78

Description

This command is used to set display related register

N/P_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I/PI_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD driving Inversion Type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

N/P_DIV[1:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **N/P_RTN[3:0]** bits (1H period clock cycle), **N/P_DIV[1:0**], and **N/P_DUM[7:0]** bits.

I/PI_DIV[1:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **I/PI_RTN[3:0]** bits(1H period clock cycle), **I/PI_DIV[1:0**], and **I/PI_DUM[7:0]** bits.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

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N/P_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation.
I/PI_ RTN[3:0]: Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[3:0]	Clock number per Line	RTN[3:0]	Clock number per Line
4'b0000	127	4'b1000	135
4'b0001	128	4'b1001	136
4'b0010	129	4'b1010	137
4'b0011	130	4'b1011	138
4'b0100	131	4'b1100	139
4'b0101	132	4'b1101	140
4'b0110	133	4'b1110	141
4'b0111	134	4'b1111	142

N/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
I/PI_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4
:	:
190d	190
others	Setting Inhibited

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (320+DUM)) [Hz]
fosc: RC oscillation frequency

GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting "00h", "01h", "02h" is inhibited)**.**

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).

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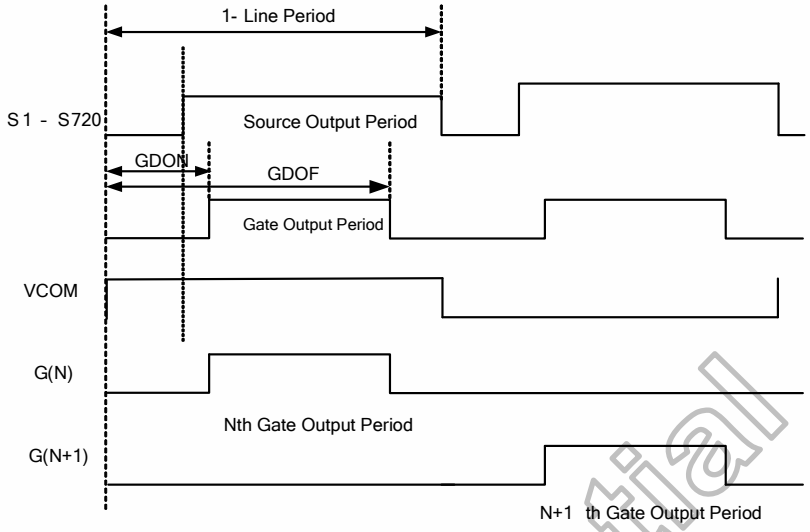

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	I/PI_NW[2:0]=3'b001, N/P_NW[2:0]=3'b001, N/P_DIV[1:0]=2'b00, I/PI_DIV[1:0]=2'b00, N/P_RTN[3:0]=4'b1000, I/PI_ RTN[3:0]=4'b1000, N/P_DUM[7:0]=8'b00110010, I/PI_ DUM[7:0]=8'b00110010. GDON7:0]=8'h0D, GDOF[7:0]=8'h78
S/W Reset	I/PI_NW[2:0]=3'b001, N/P_NW[2:0]=3'b001, N/P_DIV[1:0]=2'b00, I/PI_DIV[1:0]=2'b00, N/P_RTN[3:0]=4'b100, I/PI_ RTN[3:0]=4'b1000, N/P_DUM[7:0]=8'b00110010, I/PI_ DUM[7:0]=8'b00110010. GDON7:0]=8'h0D, GDOF[7:0]=8'h78
H/W Reset	I/PI_NW[2:0]=3'b001, N/P_NW[2:0]=3'b001, N/P_DIV[1:0]=2'b00, I/PI_DIV[1:0]=2'b00, N/P_RTN[3:0]=4'b1000, I/PI_ RTN[3:0]=4'b1000, N/P_DUM[7:0]=8'b00110010, I/PI_ DUM[7:0]=8'b00110010. GDON7:0]=8'h0D, GDOF[7:0]=8'h78

Flow Chart

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6.2.54 SETCOM: set VCOM voltage related register (B6h)

B6 H	SETCOM (Set VCOM Voltage)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	1	0	B6
1st parameter	1	↑	1	-	VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	2F
2nd parameter	1	↑	1	-	VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	57

Description

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

VMH[7:0]: Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5. The default value is 2Fh (47x0.025+2.5=3.205V)

VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	VCOMH
0	0	0	0	0	0	0	0	2.500
0	0	0	0	0	0	0	1	2.515
0	0	0	0	0	0	1	0	2.530
0	0	0	0	0	0	1	1	2.545
0	0	0	0	0	1	0	0	2.560
0	0	0	0	0	1	0	1	2.575
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	1	0	0	1	1	4.705
1	0	0	1	0	1	0	0	4.720
1	0	0	1	0	1	0	1	4.735
1	0	0	1	0	1	1	0	4.750
1	0	0	1	0	1	1	1	4.765
1	0	0	1	1	0	0	0	4.780
1	0	0	1	1	0	0	1	4.795
1	0	0	1	1	0	1	0	4.800
1	0	0	1	1	0	1	1	4.800
1	0	0	1	1	1	0	0	4.800
1	0	0	1	1	1	0	1	4.800
:	:	:	:	:	:	:	:	4.800
1	1	0	0	1	0	0	0	4.800
:	:	:	:	:	:	:	:	4.800
1	1	1	1	1	1	1	0	4.800
1	1	1	1	1	1	1	1	Setting inhibited

Note: Internal VREF can be modified by customer's request. default VREF=4.8

VCOMH= {Decimal(VMH[7:0])x0.015+2.5 **}*(VREF/4.8)**

VML[7:0]: Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5. The default value is 2Fh(47x0.015-2.5=-1.795V)

VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	0	1	-2.485
0	0	0	0	0	0	1	0	-2.470
0	0	0	0	0	1	0	1	-2.455
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	-0.055
1	0	1	0	0	1	0	0	-0.040
1	0	1	0	0	1	0	1	-0.025
1	0	1	0	0	1	1	0	-0.010
1	0	1	0	0	1	1	1	VSS
	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	VSS

Note: Internal VREF can be modified by customer's request. default VREF=4.8

VCOML= { Decimal(VML[7:0])x0.015-2.5 **}*(VREF/4.8)**

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<table>
<tr><td></td><td></td></tr>
<tr><td>Restrictions</td><td>Must enable SETEXTC command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>VMH[7:0]=8’h2F,VML[7:0]=8’h57</td></tr>
<tr><td>S/W Reset</td><td>VMH[7:0]=8’h2F,VML[7:0]=8’h57</td></tr>
<tr><td>H/W Reset</td><td>VMH[7:0]=8’h2F,VML[7:0]=8’h57</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

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6.2.55 SETOTP: set EFUSE setting (B7h)

B7 H	SETOTP (Set OTP related setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	0	1	1	1	B7
1st parameter	1	↑	1	-	PTM[1:0]		VRADJ[1:0]		OTP_POR	OTP_OTPEN	OTP_PPROG	OTP_PWE	00
2nd parameter	1	↑	1	-	-	-	-	-	-	OTP_YA[2:0]			00
3rd parameter	1	↑	1	-	-	-	-	OTP_XA[4:0]					0F
4th parameter	1	1	↑	-	OTPDATA[7:0]								00
Description	This command is used to set the OTP related setting. **OTP_POR**: for OTP read/write timing control **OTP_OTPEN**: 1'b1 to select 6.5V for OTP write operation. **OTP_PPROG** : 1'b1 to turn on OTP write mode. **OTP_PWE** : 1'b1 to write OTP. **OTP_XA[4:0]: OTP_YA[2:0] :** Select OTP write address **PTM[1:0]** : OTP Test mode register, In-house use. **VRADJ[1:0]** : OTP VPP2 adjusts register, In-house use. **OTPDATA[7:0]:** Read OTP data. When user want read OTP data, must set OTP index first and then set OTP_POR=1. After this user can get OTP data from OTPDATA[7:0]												
Restrictions	Must enable SETEXTC command												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											
Default	Status	Default Value											
	Power On Sequence	POR= 1'b0, OTPEN= 1'b0, PPROG= 1'b0, PWE=1'b0 OTP_XA[4:0]=5'b01111, OTP_YA[2:0]=3'b000 VRADJ[1:0]=2'b00 , PTM[1:0]=2'b00 OTPDATA[7:0]=8'h00											
	S/W Reset	POR= 1'b0, OTPEN= 1'b0, PPROG= 1'b0, PWE=1'b0 OTP_XA[4:0]=5'b01111, OTP_YA[2:0]=3'b000 VRADJ[1:0]=2'b00 , PTM[1:0]=2'b00 OTPDATA[7:0]=8'h00											
	H/W Reset	POR= 1'b0, OTPEN= 1'b0, PPROG= 1'b0, PWE=1'b0 OTP_XA[4:0]=5'b01111, OTP_YA[2:0]=3'b000 VRADJ[1:0]=2'b00 , PTM[1:0]=2'b00 OTPDATA[7:0]=8'h00											
Flow Chart	-												

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6.2.56 SETEXTC: enable extention command (B9h)

<table>
<tr><td>B9 H</td><td colspan="13">SETEXTC (Set extended command set)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>B9</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FF</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>83</td></tr>
<tr><td>3rd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>47</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set extended command set access enable.

<table><tr><td>Extend cmd</td><td>Command description</td></tr><tr><td>Enable</td><td>Must write 3 parameters (ffh,83h,47h) by order</td></tr><tr><td>Disable(default)</td><td>Write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (ffh,83h,47h)</td></tr></table></td></tr>
<tr><td>Restrictions</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
</table>

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6.2.57 SETID: set ID (C4h)

C4 H	SETID (Set ID)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	1	0	0	C4
1st parameter	1	↑	1	-	ID1[7:0]								00
2nd parameter	1	↑	1	-	ID2[7:0]								00
3rd parameter	1	↑	1	-	ID3[7:0]								00
4th parameter	1	1	↑	-	-	-	-	-	-	ID_OTP_TIMES[2:0]			00

Description

This command is used to set ID.

ID_OTP_TIMES[2:0]: Read ID OTP programmed times.

ID_OTP_TIMES[2:0]	ID OTP programmed times
3'b000	Not programmed
3'b001	1 time
3'b010	2 times
3'b011	3 times
3'b100	4 times

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	ID1[7:0]=8'h00, ID2[7:0]=8'h00, ID3[7:0]=8'h00, ID_OTP_TIMES[2:0]=3'b000
S/W Reset	No change
H/W Reset	OTP value

Flow Chart

-

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6.2.58 SETCABC: set CABC related setting (C9h)

C9H	SETCABC(Set CABC Related Setting)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	0	0	1	C9
1st parameter	1	↑	1	-	BC_CTL	PWMDIV[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY	0F
2nd parameter	1	↑	1	-	PWM_PERIOD[7:0]								23

Description

This command is used to set CABC parameter

BC_CTL: The control reigister for LED driver when IC needs enable signal.
'0': BC_CTRL pin='L'
'1': BC_CTRL pin='H'

SEL_BLDUTY : The backlight PWM output duty on/off control when CABC operated.
'0', The backlight PWM output duty is 100%.
'1', The backlight PWM output duty is calculated from CABC operation.

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

SEL_GAIN[1:0]: CABC gain select. **(Not Open)**
00: use 1.00 as CABC calculate gain
01: use 0.5x CABC calculate gain
10: use 0.75x CABC calculate gain
11: use CABC calculate gain

PWMDIV[2:0]: Internal PWM_CLK divider for CABC clock.

PWMDIV[2:0]			Brightness Control Clock
0	0	0	PWM_CLK / 1
0	0	1	PWM_CLK / 2
0	1	0	PWM_CLK / 4
0	1	1	PWM_CLK / 8
1	0	0	PWM_CLK / 16
1	0	1	PWM_CLK / 32
1	1	0	PWM_CLK / 64
1	1	1	PWM_CLK / 128

PWM_PERIOD[7:0]: The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV)) x (256x(PWM_PERIOD[7:0]+1)).
For details, please refer to chapter "5.15.2 CABC Block".

Restrictions: Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>PWMDIV[2:0]= 3’h00, SEL_GAIN[1:0]= 2’b11, INVPULS=1,
SEL_BLDUTY= 1, PWM_PERIOD[7:0]=8h’23, BC_CTL = 1’b0</td></tr>
<tr><td>S/W Reset</td><td>PWMDIV[2:0]= 3’h00, SEL_GAIN[1:0]= 2’b11, INVPULS=1,
SEL_BLDUTY= 1, PWM_PERIOD[7:0]=8h’23, BC_CTL = 1’b0</td></tr>
<tr><td>H/W Reset</td><td>PWMDIV[2:0]= 3’h00, SEL_GAIN[1:0]= 2’b11, INVPULS=1,
SEL_BLDUTY= 1, PWM_PERIOD[7:0]=8h’23, BC_CTL = 1’b0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

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6.2.59 SETPanel: set panel characteristic (CCh)

CCH	SETPANEL(Set Panel characteristic register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	1	0	0	CC
1st parameter	1	↑	1	-	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00
Description	This command is used to set Panel characteristic related register **REV_PANEL:** The source output data polarity selected. '0': normally white panel. '1': normally black panel. **BGR_PANEL:** The color filter order direction selected. '0': S1:S2:S3='R':'G':'B' '1': S1:S2:S3='B':'G':'R' **GS_PANEL:** The gate driver output shift direction selected. '0': G1→G320 '1': G320→G1 **SS_PANEL:** The source driver output shift direction selected. '0': S720→S1 '1': S1→S720												
Restrictions	Must enable SETEXTC command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	SS_PANEL=1'b0, GS_PANEL=1'b0, REV_PANEL=1'b0, BGR_PANEL=1'b0
S/W Reset	SS_PANEL=1'b0, GS_PANEL=1'b0, REV_PANEL=1'b0, BGR_PANEL=1'b0
H/W Reset	SS_PANEL=1'b0, GS_PANEL=1'b0, REV_PANEL=1'b0, BGR_PANEL=1'b0

Flow Chart: -

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6.2.60 SETGamma: set gamma curve (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	↑	1	-	-	-	VRP0[5:0]						01
2nd parameter	1	↑	1	-	-	-	VRP1[5:0]						02
3rd parameter	1	↑	1	-	-	-	VRP2[5:0]						00
4th parameter	1	↑	1	-	-	-	VRP3[5:0]						13
5th parameter	1	↑	1	-	-	-	VRP4[5:0]						12
6th parameter	1	↑	1	-	-	-	VRP5[5:0]						24
7th parameter	1	↑	1	-	-	PRP0[6:0]							08
8th parameter	1	↑	1	-	-	PRP1[6:0]							55
9th parameter	1	↑	1	-	-	-	-	PKP0[4:0]					02
10th parameter	1	↑	1	-	-	-	-	PKP1[4:0]					14
11th parameter	1	↑	1	-	-	-	-	PKP2[4:0]					1A
12th parameter	1	↑	1	-	-	-	-	PKP3[4:0]					19
13th parameter	1	↑	1	-	-	-	-	PKP4[4:0]					16
14th parameter	1	↑	1	-	-	-	VRN0[5:0]						1B
15th parameter	1	↑	1	-	-	-	VRN1[5:0]						2D
16th parameter	1	↑	1	-	-	-	VRN2[5:0]						2C
17th parameter	1	↑	1	-	-	-	VRN3[5:0]						3F
18th parameter	1	↑	1	-	-	-	VRN4[5:0]						3D
19th parameter	1	↑	1	-	-	-	VRN5[5:0]						3E
20th parameter	1	↑	1	-	-	PRN0[6:0]							2A
21th parameter	1	↑	1	-	-	PRN1[6:0]							77
22th parameter	1	↑	1	-	-	-	-	PKN0[4:0]					09
23th parameter	1	↑	1	-	-	-	-	PKN1[4:0]					06
24th parameter	1	↑	1	-	-	-	-	PKN2[4:0]					05
25th parameter	1	↑	1	-	-	-	-	PKN3[4:0]					0B
26th parameter	1	↑	1	-	-	-	-	PKN4[4:0]					1D
27th parameter	1	↑	1	-	CGMN1[1:0]		CGMN0[1:0]		CGMP1[1:0]		CGMP0[1:0]		CC
Description	This command is used for Gamma Curve related Setting. For details, please refer to Gamma resister stream and 8 to 1 Selector.												
Restrictions	Must enable SETEXTC command												
Register Availability	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
	Sleep In or Booster Off							Yes					
Flow Chart	-												

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6.2.61 SetCE: set color Enhancement (E5h)

E5H	SETCE(Set Color Enhance)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	0	0	1	0	1	E5
1st parameter	1	↑	1	-	-								00
2nd parameter	1	↑	1	-				-					00
3rd parameter	1	↑	1	-				-					06
4th parameter	1	↑	1	-				-					04
5th parameter	1	↑	1	-				-					02
6th parameter	1	↑	1	-				-					00
7th parameter	1	↑	1	-								CE_EN	00
Description	This command is used to set setting of color enhancement function. CE_EN : 1: Enable Color Enhancement, 0: Diable Color Enhancement. Under Patial/Idel Mode, CE_EN setting with no effect.												
Restrictions	Must enable SETEXTC command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	CE_EN= 1'b0
S/W Reset	CE_EN= 1'b0
H/W Reset	CE_EN= 1'b0

Flow Chart -

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6.2.62 SetVMF: set VMF(FDh)

FDH	SETVMF(Set VCOM Offset)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	1	1	1	0	1	FD
1st parameter	1	↑	1	-	VMF[7:0]								80
2nd parameter	1	↑	1	-						VCOM_OTP_TIMES[2:0]			00

Description

VMF[7:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

VMF[7:0]	VCOMH	VCOML
0	"VMH" – 128d	"VMH" – 128d
1	"VMH" – 127d	"VMH" – 127d
2	"VMH" – 126d	"VMH" – 126d
3	"VMH" – 125d	"VMH" – 125d
:	:	:
126	"VMH" – 2d	"VMH" – 2d
127	"VMH" – 1d	"VMH" – 1d
128	"VMH"	"VML"
129	"VMH" + 1d	"VMH" + 1d
130	"VMH" + 2d	"VMH" + 2d
:	:	:
254	"VMH" + 126d	"VMH" + 126d
255	"VMH" + 127d	"VMH" + 127d

Note: VMH[7:0]-128+VMF[7:0]>=0 and VML[7:0]-128+VMF[7:0]>=0

Restrictions: Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	VMF[7 :0]= 8'h80, VCOM_OTP_TIMES[2 :0] = 3'b000
S/W Reset	VMF[7 :0]= OTP_Value, VCOM_OTP_TIMES[2 :0] = 3'b000
H/W Reset	VMF[7 :0]= OTP_Value, VCOM_OTP_TIMES[2 :0] = 3'b000

Flow Chart: -

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7.Layout Recommendation

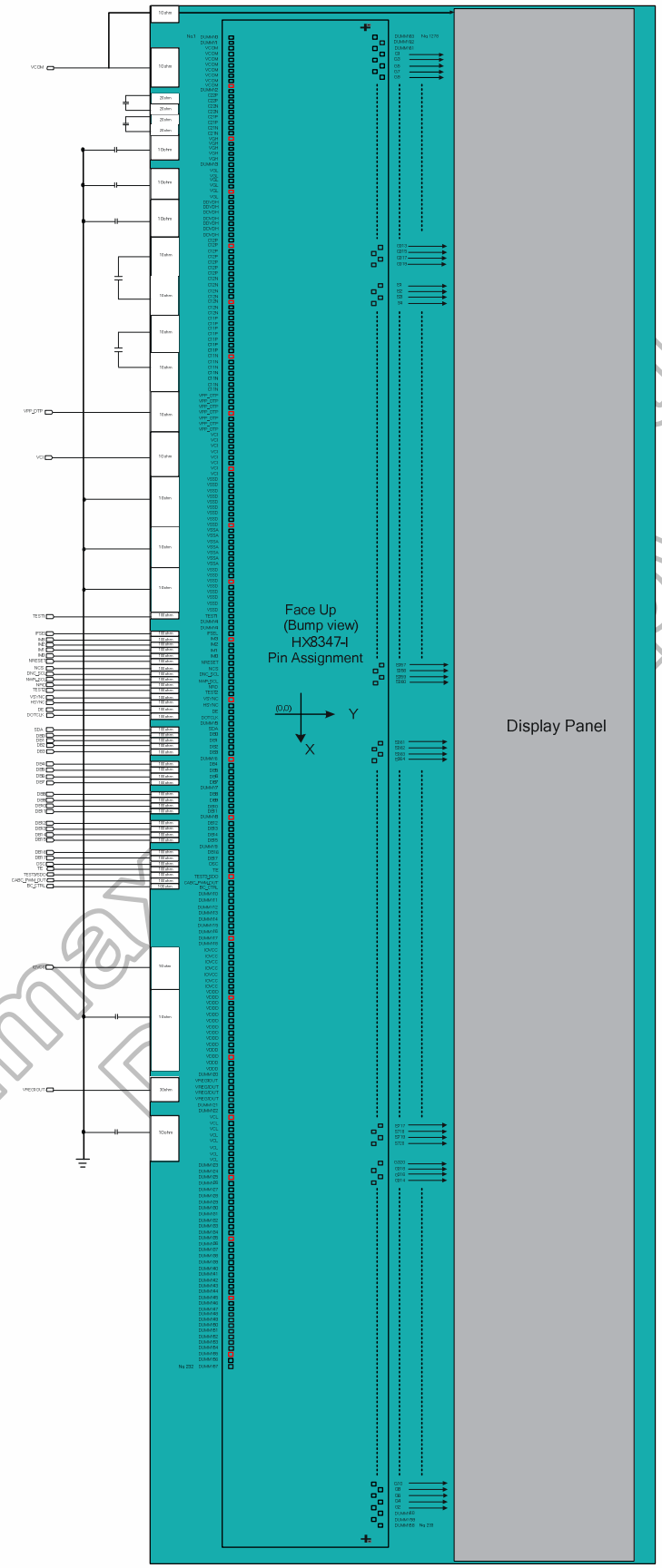

Figure 7-1: Layout recommendation of HX8347-I mode

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7.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA,VSSC	Power supply	10	Ω
VSSD	Power supply	10	Ω
VPP_OTP	Power supply	10	Ω
OSC	Input	100	Ω
IM[3:0], IFSEL	Input	100	Ω
NRD, NWR_SCL, DNC_SCL, NCS, SDA	Input	100	Ω
NRESET	Input	100	Ω
TE, CABC_PWM_OUT,BC_CTRL	Output	100	Ω
DB[17:0],	I/O	100	Ω
DOTCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	50	Ω
C11P, C11N, C12P, C12N	Capacitor connection	10	Ω
C21P, C21N	Capacitor connection	15	Ω
C22P, C22N	Capacitor connection	15	Ω
TEST[2:1]	Input	100	Ω
DUMMY	Dummy	100	Ω

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7.2 External components connection

Capacitor	Recommended voltage	Capacity
C1 (C11P/N)	6V	1µF (B characteristics)
C2 (C12P/N)	6V	1µF (B characteristics)
C3 (DDVDH)	10V	1µF (B characteristics)
C4 (C21P/N)	10V	1µF (B characteristics)
C5 (C22P/N)	10V	1µF (B characteristics)
C6 (VGH)	25V	1µF (B characteristics)
C7 (VGL)	16V	1µF (B characteristics)
C9 (VCL)	6V	1µF (B characteristics)
C10(VDDD)	6V	1µF (B characteristics)

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8. Electrical Characteristic

8.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.			Note
			Min.	Typ.	Max.	
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3	-	+4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+4.6	Note(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3	-	+6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3	-	+4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3	-	+9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3	-	+18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	-16.5	-	0	Note(8)
Logic Input Voltage	V_{IN}	V	-0.3	-	IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3	-	IOVCC+0.5	-
Operating Temperature	Topr	℃	-40	-	+85	Note(9),(10)
Storage Temperature	Tstg	℃	-55	-	+110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

Table 8-1: Absolute maximum ratings

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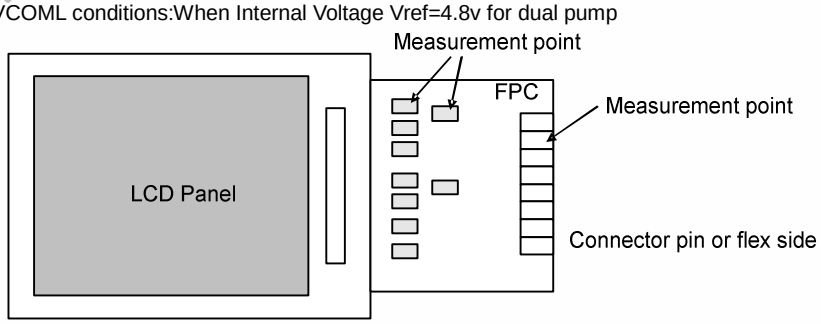
8.2 DC characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.3	2.8	3.3	
	VREG1	Dual Pump	3.3	4.05	4.8	
Gate Drive High Voltage	VGH	IVGH=100uA (Typ:BT=001) VCI=2.8 Dual Pump	9.5	14.25	-	
Gate Drive Low Voltage	VGL	IVGL=100uA (Typ:BT=001) VCI=2.8 Dual Pump	-6.85	-9.5		
Drive Supply Voltage	|VGH-VGL|	-	-	-	30	
Input / Output						
High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
Oscillator frequency	fOSC	Frame rate at 65hz,default Vs and Hs setting Ta=25℃	5.7	6	6.3	MHz
Booster(VCI=2.8V)						
DDVDH boost voltage1	DDVDH	Dual Pump IDDVDH=1mA	4.8	5.0	5.2	V
VCL boost voltage	VCL	ICL=-300uA	-2.5	-2.65	2.75	
VCOM Generator(VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	2.5	4.4	7.3	V
VCOM high level	VCOMH	No load Dual Pump	2.5	3.205	4.8	V
VCOM low level	VCOML	No load	-2.5	-1.195	VSSD	V
Source Driver(Typ:Ta=25℃ VCI=2.8v)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VREG1-1.0	-	+/- 10	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	+/- 30	+/- 50	mV
Output voltage range	VOS	-	0.1	-	DDVDH-0.1	V
Output offset voltage	Voff	-		+/-30	+/-50	mV

*Vreg1/VCOMH/VCOML conditions:When Internal Voltage Vref=4.8v for dual pump



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8.3 AC characteristics

8.3.1 Parallel interface characteristics (8080-series MPU)

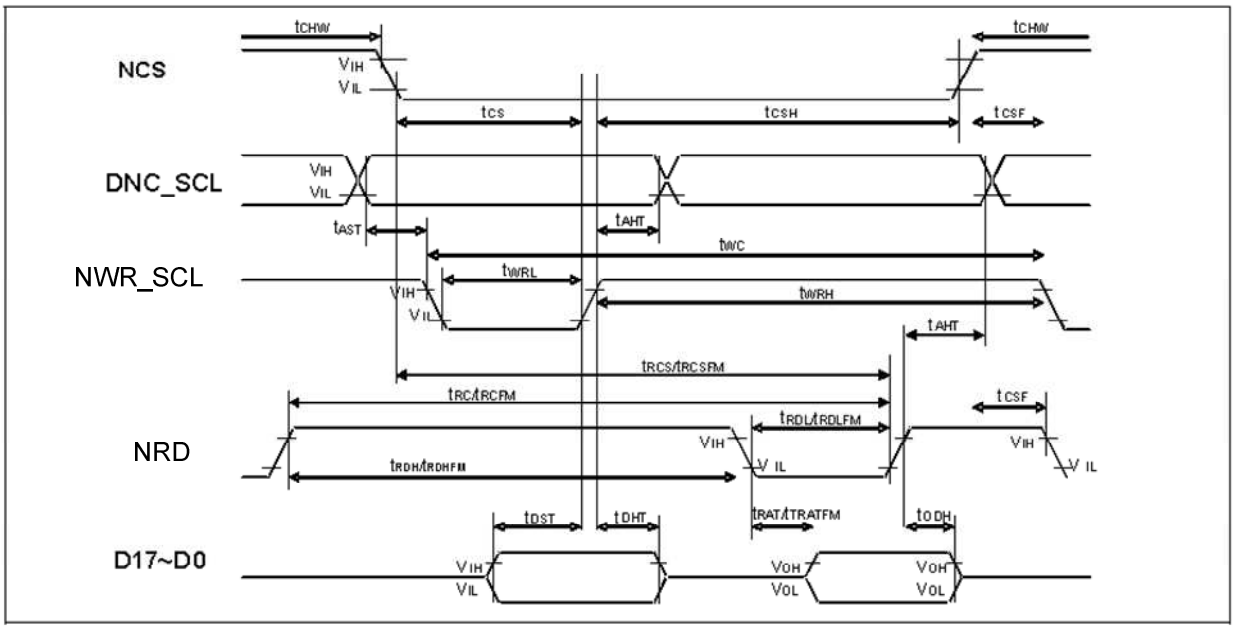

Figure 8-1: Parallel interface characteristics (8080-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70℃)

Signal	Symbol	Parameter	Spec.			Unit	Description
			Min	Typ	Max		
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	0 10	- -	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 15 45 355 10 10	- - - - - -	- - - - - -	ns	-
NWR_SCL	t_{WC} t_{WC} t_{WRH} t_{WRL}	Write cycle(1pixel for one write) Write cycle (1 pixel for 2 or 3 write) Control pulse “H” duration Control pulse “L” duration	100 50 15 15	- - - -	- - - -	ns	-
NRD (ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse “H” duration (ID) Control pulse “L” duration (ID)	160 90 45	- - -	- - -	ns	When read ID data
NRD (FM)	t_{RCFM} t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) (1pixel for one write) Read cycle (FM) (1 pixel for 2 or 3 write) Control pulse “H” duration (FM) Control pulse “L” duration (FM)	600 400 90 355	- - - -	- - - -	ns	When read from frame memory
D15 to D0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - - - -	- - 40 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

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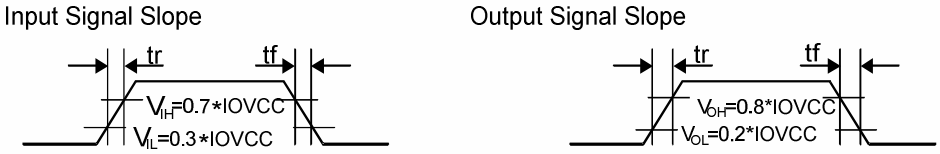

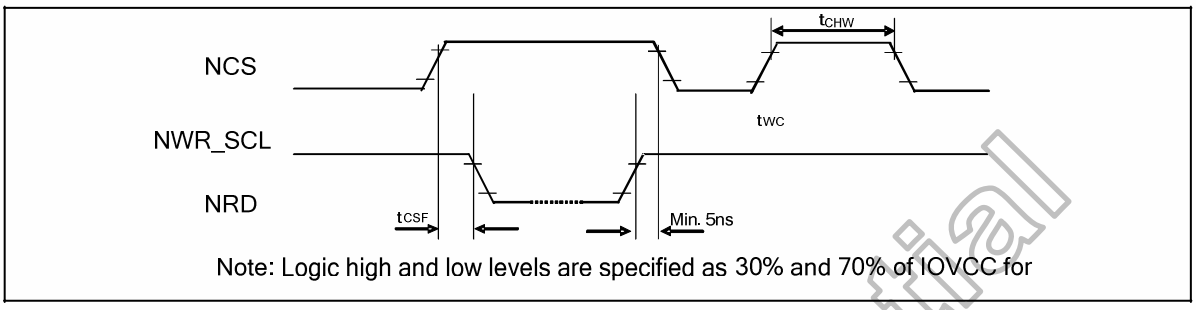

Figure 8-2: Chip select timing

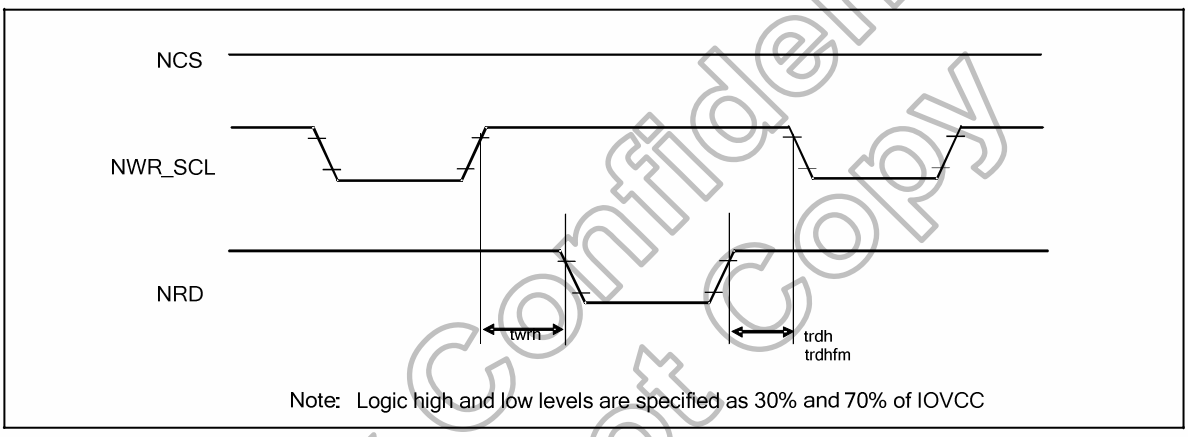

Figure 8-3: Write to read and read to write timing

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8.3.2 Serial interface characteristics

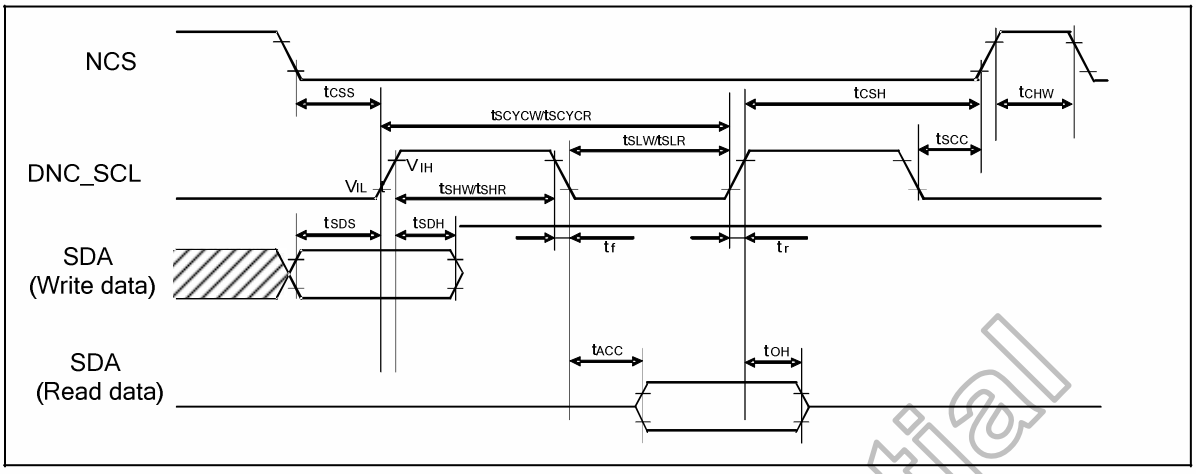
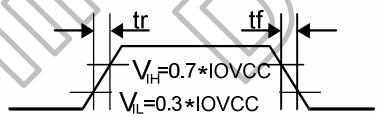


Figure 8-4: Serial interface characteristics

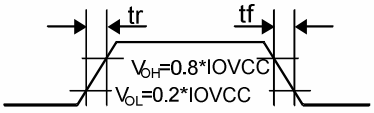
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Serial clock cycle (Write) DNC_SCL "H" pulse width (Write) DNC_SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	DNC_SCL	14 6 6	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDA	6 6	- -	- -	ns
Serial clock cycle (Read) DNC_SCL "H" pulse width (Read) DNC_SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	DNC_SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDI for maximum C_L=30pF For minimum C_L=8pF	10	-	50	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	50	ns
DNC_SCL to Chip select	t_{SCC}	DNC_SCL, NCS	20	-		ns
NCS "H" pulse width	t_{CHW}	NCS	40	-		ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 65	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



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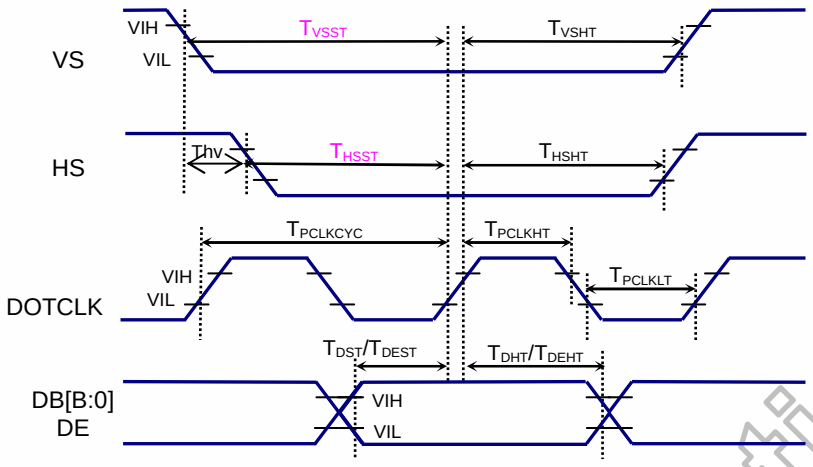
8.3.3 RGB interface characteristics

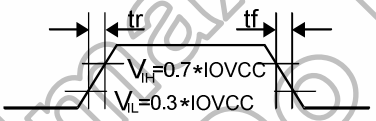


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,T_A = -30 to 70℃)

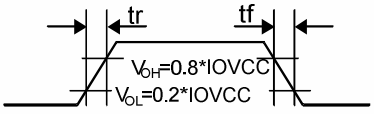
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	T_{CLKLT}		15	-	-	ns
Pixel high pulse width	T_{CLKHT}		15	-	-	ns
Vertical Sync. set-up time	T_{VSST}		15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}		15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}		15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}		15	-	-	ns
Data Enable set-up time	T_{DEST}		15	-	-	ns
Data Enable hold time	T_{DEHT}		15	-	-	ns
Data set-up time	T_{DST}		15	-	-	ns
Data hold time	T_{DHT}		15	-	-	ns
Phase difference of sync signal falling edge	Thv		0	-	240	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



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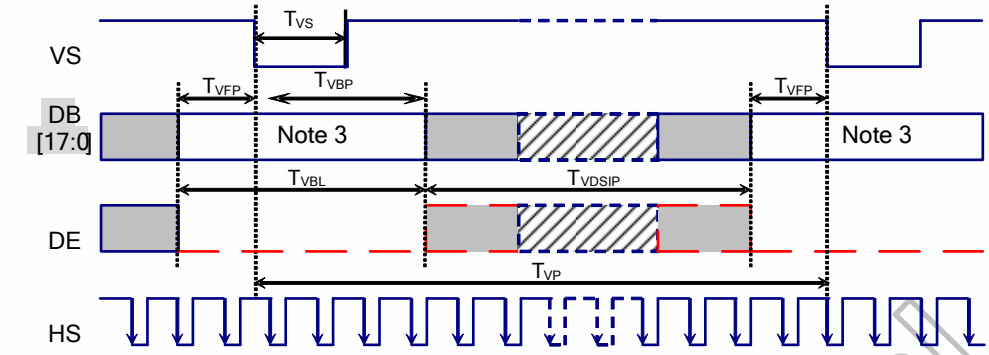
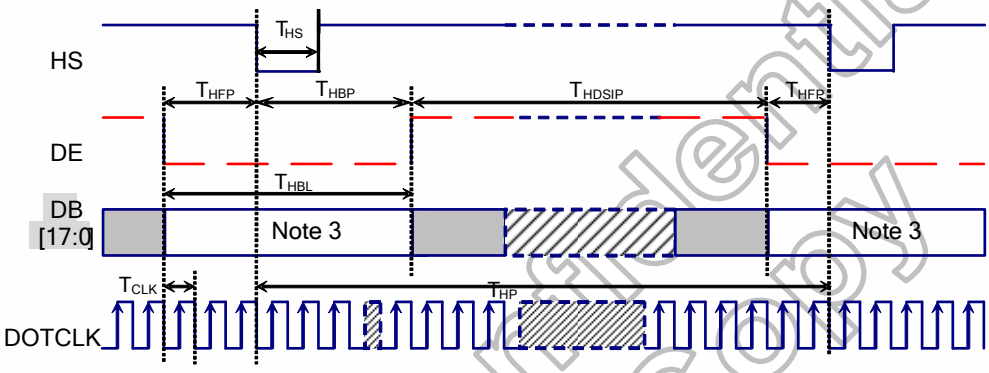
Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical Timing						
Vertical cycle period	T_{VP}		324	-	452	HS
Vertical low pulse width	T_{VS}		2	2	-	HS
Vertical front porch	T_{VFP}		2	2	6	HS
Vertical back porch	T_{VBP}		2	6	126	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	8	132	HS
Vertical active area	T_{VDISP}		-	320	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}		244		1008	DOTCLK
Horizontal low pulse width	T_{HS}		2	2	256	DOTCLK
Horizontal front porch	T_{HFP}		2	2	256	DOTCLK
Horizontal back porch	T_{HBP}		2	6	256	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	4	8	768	DOTCLK
Horizontal active area	T_{HDISP}		-	240	-	DOTCLK
Pixel clock cycle	f_{CLKCYC}		3.9		16.6	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, T_A=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of DOTCLK.
(4)16.6MHz is using at below condition: 324(Hs)x1008(DOTCLK)x50(Hz)

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8.3.4 Reset input timing

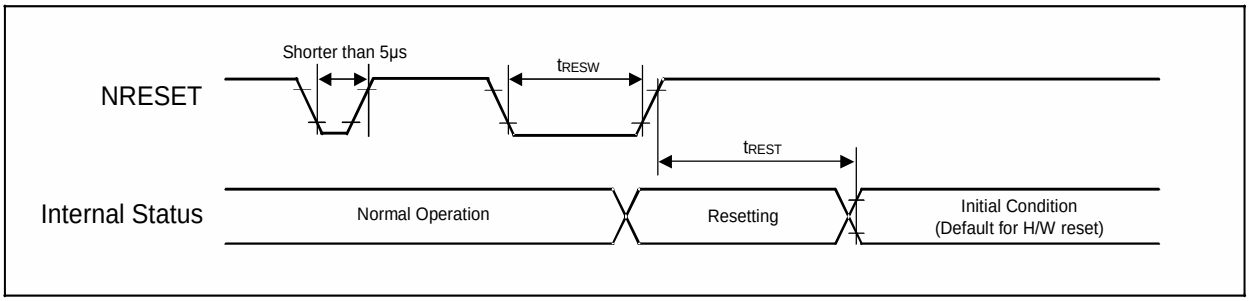


Figure 8-5: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	5	-	-	When reset applied during SLPOUT mode	ms
		-	120	-	-	When reset applied during SLPIN mode	ms

Table 8-2: Reset input timing

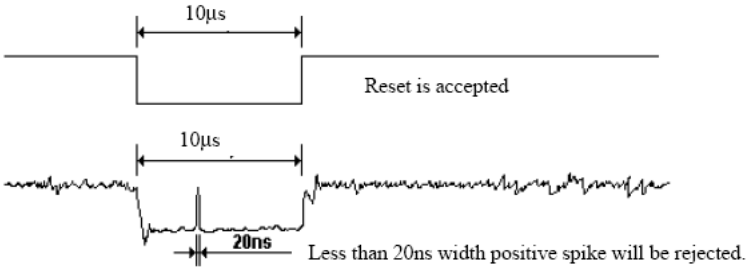
Note: (1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

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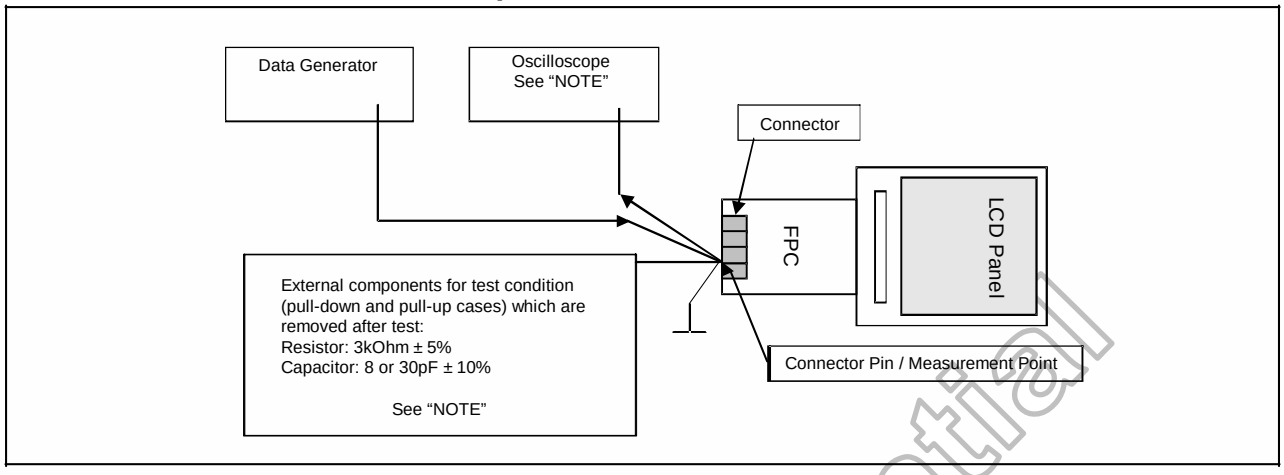
tACC, tOH measurement condition

Measurement condition set-up



Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Figure 8-6: tACC and tOH measurement condition set-up

Minimum value measurement

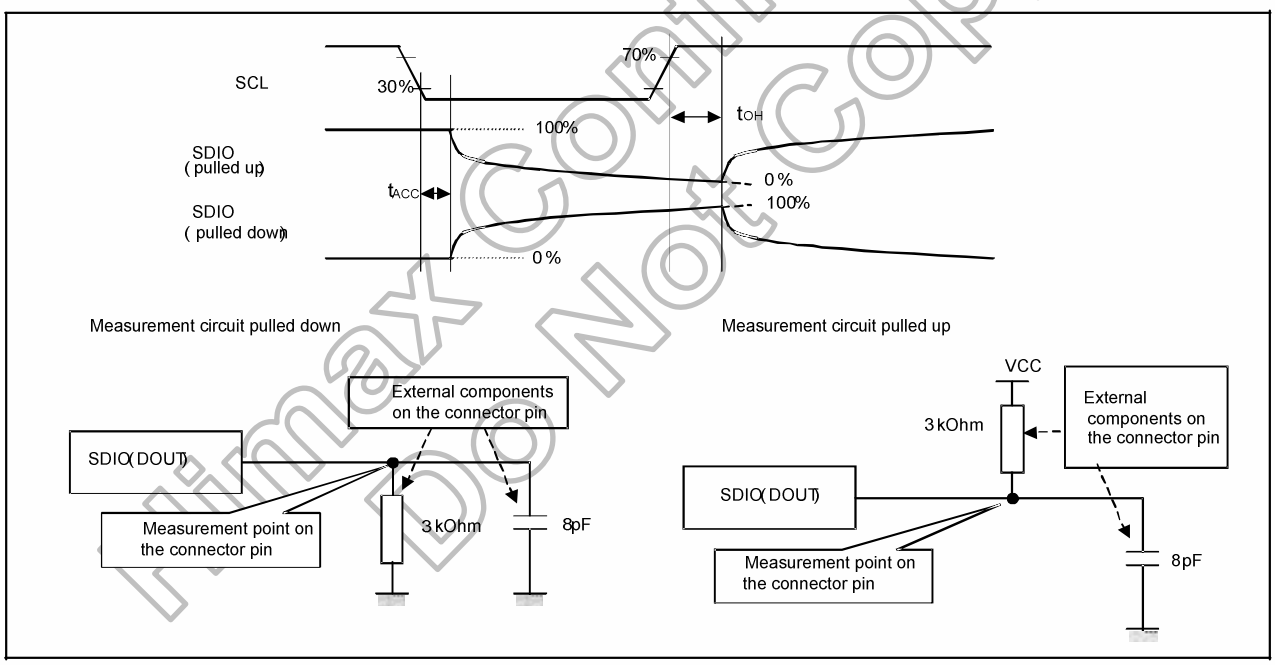


Figure 8-7: tACC and tOH minimum condition set-up

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Maximum value measurement

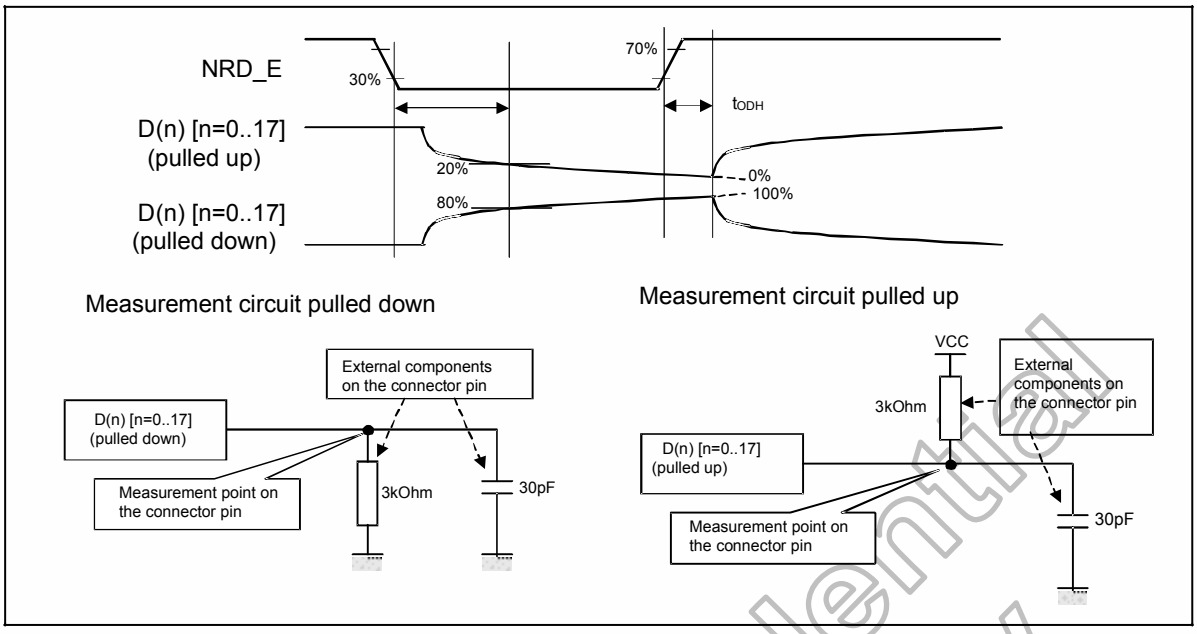

Figure 8-8: tACC and tOH maximum value measurement

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9.Ordering Information

Part No.	Package
HX8347-I000 PDxxx	PD : mean COG xxx : mean chip thickness (µm), (default: 250 µm)

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